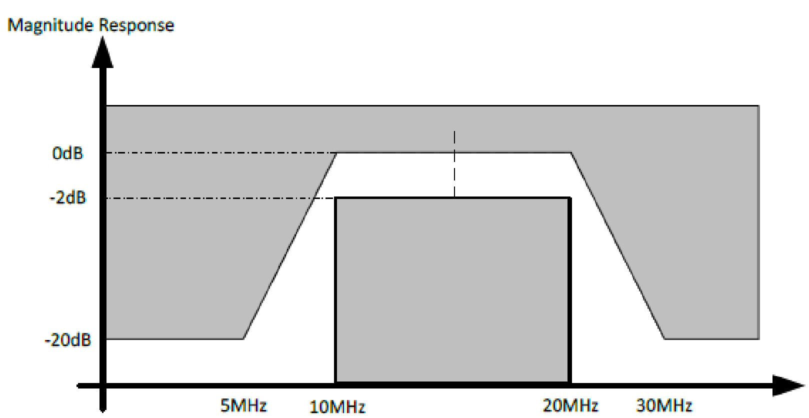
Mini Project #2: Design an Opamp-RC Bandpass Filter

This project can be done in groups of **4 students (or less).**
Project grade will be based on the submitted report; any copied reports will be given **ZERO**.
You should provide the required simulations using **CADENCE**.
All the equations derivations should be written in **WORD.**
Project submission will be an email containing a **PDF** as an attachment to
elc3010.analog.assignments@gmail.com
The cover page must contain the group names in **Arabic** and their **ID's**.
All graphs and figures should be clear with readable axes and traces.
If the students participating in the project ID's are: 9202293, 9202162, 9202038 & 9202125
then the report name should be "9202293 & 9202162 & 9202038 & 9202125".
The project is due on **Saturday April 29th, 2023 at 23:59**.

Design Specifications:

The Filter response should be within the white area of the figure below.



The design should consist of **three phases**:

1. **Find the transfer function** that satisfies the specifications showing the location of poles and zeros (if any).
2. **Design the circuit** that synthesizes the transfer function obtained in part 1. For the design, choose any suitable **cascade** Opamp-RC architecture. Design all component values such that the total capacitance does not exceed 100pF.
3. **Simulate your design and verify it** using **Cadence**, you can use ideal Op-amps (voltage controlled voltage source with a gain of 10,000 and $\mathbf{V_{max}=1V}$ & $\mathbf{V_{min}=-1V}$).

<u>Report Requirements</u>

- Write down a complete analysis of **part 1**, showing how you did obtain the transfer function (**order**, etc.)
- Draw the complete schematic of the circuit you chose to implement the filter's transfer function in **part 2 showing the values of the components**.
- Write down your design equations and show how you reached the component values.
- Show the simulation results indicating the filter **specifications** on the response (In Cadence: ac analysis). Plot both magnitude and phase.
- Find the **poles and zeros** locations of the filter (In Cadence: pz analysis).
- Show the **output referred noise** of the filter from **DC-100MHz** (In Cadence: noise analysis).
- For this simulation only: **Reduce** all resistors by factor **2**, keep the same transfer function, and simulate the noise again. What is your **estimate** of the area and power increase?
- Plot the **transient response** of the outputs of **all biquadratic stages** for a sine-wave input of $1V_{pp}$ at 15MHz. Plot discrete Fourier transform (**in dB**) and hence calculate third harmonic distortion (**HD_3**) at **V_{out}** (In Cadence: transient analysis and **DFT** in calculator).
- Simulate and **tabulate the effect** on poles and zeros, maximum passband ripples, and minimum stopband attenuation for the following cases:
    - Varying all capacitators by ±15%.
    - Varying capacitors in 1^{st} section by ±2% relative to other capacitors of other stages.
    - Vary the gain of the Op-amps to 1000 and 100.
    - Add a BW limitation for the Op-amps. Set the gain at 1000 and **vary BW** to 10MHz and 1MHz.
      Hint: Use voltage controlled voltage source followed by an RC section to set BW $(BW = \frac{1}{2\pi RC})$ followed by an ideal gain of 1 as a buffer.
    - **For each** of the above cases, plot **3 curves in the same figure** (ideal magnitude response and magnitude response for the required variations).
- **Discussion on your results.**
- **Make sure that the figures, with its markers, and captions, are clear and visible.**
- **Be concise and limit the number of pages to 10 without the cover.**
- **Any missing item from the items above will be penalized in the report grading.**