Monil Shah

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Education

University of California San Diego *GPA 4.0/4.0*

M.S. Computer Engineering *Sep 2021 - Present*

Birla Institute of Technology and Science, Pilani *CGPA - 8.74/10*

B.E.(Hons.) in Electrical and Electronics Engineering *Aug 2014 - May 2018*

Projects

Graduate Student Researcher *University of California San Diego*

Mentor: Prof. Tajana Simunic Rosing *Sep 2021 - present*

- Responsible for designing, verifying and synthesizing CNN hardware accelerator for tapeout
- Using GEM5 to collect statistics for PPA prediction

Parallel Computing *University of California San Diego*

Mentor: Prof. Bryan Chin *Apr 2022 - Jun 2022*

- Accelerated matrix multiplication in C using blocking and vectorization on Intel AVX2
- Accelerated matrix multiplication in CUDA using blocking and shared memory on K80 and T4

Advanced microarchitecture *University of California San Diego*

Mentor: Prof. Samira Mirbagher *Jan 2022 - Mar 2022*

- Performed workload analysis and design space exploration for prefetcher and cache replacement on champsim simulator.
- Explored microarchitectural optimizations to create gadgets similar to spectre and meltdown for security attacks.

CUDA Programming *University of California San Diego*

Mentor: Prof. An Cheolhong *Jan 2022 - Mar 2022*

- Used reinforcement learning to implement mine-sweeper game using multithreaded programming model
- Implemented seed table construction on GPU for finding arbitrary length kmer in a string of DNA sequence

Modelling Branch Predictor and L1 Cache *University of Califonia San Diego*

Mentor: Prof. Jishen Zhao *Sep 2021 - Dec 2021*

- Modelled various branch predictors like Gshare, Tournament, Perceptron, TAGE and L1 Cache structure with FIFO replacement in C.

Mapping of VGGnet Convolution Layer on 8*8 Systolic Array *University of Califonia San Diego*

Mentor: Prof. Mingu Kang *Sep 2021 - Dec 2021*

- Mapped layers of VGGnet by tiling on a 8*8 2D systolic array designed in Verilog. Performed optimizations like quantization and pruning to implement clock gating and reduce dynamic power

Fault Tolerant Network-on-Chips *BITS Pilani*

Mentor: Dr. Soumya J. *Aug 2017 - Dec 2017*

- Devised and modelled static scheduling algorithm to support packet routing on a Mesh-of-Tree Topology based NoC under router faults ensuring scalability in topology size

Professional Experience

NVIDIA Graphics India Pvt. Ltd. *Bangalore, India*

ASIC Design & Verification Engineer, PCIe *Jul 2018 - Aug 2021*

- Designed PCIe specification defined features like Error Detection and Reporting, Port Containment for Root Port IP
- Responsible for timing, clock gating fixes, integration of internal DFT Plugins, Infrastructure Improvements, Code Coverage analysis, Flow Automation
- Worked on various aspects of verification methodology like Testplanning, micro-architecture discussions, infrastructure setup, Functional Coverage
- Extended UVM based infrastructure in system verilog for verifying PCIe Transaction Layer features like ResetWidth checks, MSI Ordering Checks, Address Blocker IP, Error Detection and Reporting(AER) , Register Access Security, RAS Error Injection

NVIDIA Graphics India Pvt. Ltd. *Bangalore, India*

Verification Intern, PCIe *Jul 2017 - Dec 2017*

- Responsible for automation of test and coverage flows specific to the team
- Assisted in Bug fixes and verification closure

Publications

- *PatterNet: Explore and Exploit Filter Patterns for Efficient Deep Neural Networks*, B. Khaleghi, U. Mallappa, D. Yaldiz, H. Yang, M. Shah, J. Kang, T. Rosing, DAC 2022
- *Multi-application Based Network-on-Chip Design for Mesh-of-Tree Topology Using Global Mapping and Reconfigurable Architecture*, Mohit Upadhyay, **Monil Shah**, P Veda Bhanu, J Soumya, Linga Reddy Cenkeramaddi, 32nd International Conference on VLSI Design, VLSID 2019
- *A Novel Fault-Tolerant Routing Technique for Mesh-of-Tree based Network-on-Chip Design*, Mohit Upadhyay, **Monil Shah**, P Veda Bhanu, J Soumya, Linga Reddy Cenkeramaddi, Henning Idsøe, IEEE TENCON 2018

Teaching Experience

CSE 140 (Winter 22), 140L (Spring 22) - Digital Design Systems *University of California San Diego*

Mentor : Prof. Rosing (Winter), Prof. Chin (Spring). *Jan 2022 - Present*

- Responsible for designing HW, Exam questions and solving them (CSE 140), designing Verilgo based labs (CSE 140L)
- Responsible for answering on Q/A forum, holding discussion sessions, office hours and grading for a class of 200-260 undergraduate students

Microprocessors and Interfacing *BITS Pilani*

Mentor : DR. SOUMYA J. *Jan 2018 - May 2018*

- One of the Teaching Assistant for Course on Microprocessors with a strength of around 400 Students.
- Responsible for Labwork supervision and mentoring and assisted in End-Semester Grading

Relevant Courses

M.S. Courses: Paralle Computing (CSE 260), Parallel computer architecture (CSE 240B), Advanced microrchitecture, (CSE 240C), GPU Programming (ECE 277), Principles in Computer Architecture (CSE 240A), Hardware implementation of Machine Learning Algorithm (ECE 284), VLSI Digital System (ECE 260A), Operating systems (CSE 120)

B.E. Courses: Introduction to Operating Systems, FPGA Systems Design , Computer Architecture, Analog and Digital VLSI Design, Microprocessors and Interfacing, Embedded System Design, Digital Design

Technical Strengths

Programming Languages:: C++, Verilog, System Verilog, Bash, Perl, Pytorch, Python

Tools & Simulators:: Champsim, Verdi, dc_shell, lc_shell, Vivado, Quartus, Modelsim, gem5

Responsibilities

2016 **Head of Dept of Technical Arts**: Managed department of over 60 students with focus on design Creatives, Website development and Application development for College Fest. We helped achieve a footfall over 10,000 and Social Outreach of 100,000 *BITS Pilani*

2014 **Head Boy, Student's Council**: As Head Boy and part of Student Representative Council for the academic year 2013-14, I was the point of contact of students to administration and worked closely with teachers and students for coordinating curricular and extracurricular activities. *DPS Surat*