Monil Shah

+1-(858)-308-6607 | m3shah@ucsd.edu | mnlshah

Education

University of California San Diego *GPA 4.0/4.0*

M.S. Computer Engineering *Sep 2021 - Present*

Birla Institute of Technology and Science, Pilani *CGPA - 8.74/10*

B.E.(Hons.) in Electrical and Electronics Engineering *Aug 2014 - May 2018*

Professional Experience

NVIDIA Graphics India Pvt. Ltd. *Bangalore, India*

ASIC Verification Engineer, PCIe *Jul 2018 - Aug 2021*

- Worked on various aspects of verification methodology like Testplanning, micro-architecture discussions, infrastructure setup, Functional Coverage
- Responsible for ISO26262 - Industry automotive safety standard- Verification closure of PCIe IP within GPU
- Extended UVM based infrastructure in system verilog for verifying PCIe Transaction Layer features like ResetWidth checks, MSI Ordering Checks, Address Blocker IP, Error Detection and Reporting(AER) , Register Access Security, RAS Error Injection

NVIDIA Graphics India Pvt. Ltd. *Bangalore, India*

ASIC Design Engineer, PCIe *Mar 2020 - Apr-2021*

- Designed PCIe specification defined features like Error Detection and Reporting, Port Containment for Root Port IP
- Responsible for Timing, Clock Gating and Power Improvements
- Delivered integration of internal DFT Plugins
- Assisted in Infrastructure Improvements, Code Coverage analysis, Flow Automation

NVIDIA Graphics India Pvt. Ltd. *Bangalore, India*

Verification Intern, PCIe *Jul 2017 - Dec 2017*

- Responsible for automation of test and coverage flows specific to the team
- Assisted in Bug fixes and verification closure

Publications

- *Multi-application Based Network-on-Chip Design for Mesh-of-Tree Topology Using Global Mapping and Reconfigurable Architecture*, Mohit Upadhyay, **Monil Shah**, P Veda Bhanu, J Soumya, Linga Reddy Cenkeramaddi, 32nd International Conference on VLSI Design, VLSID 2019
- *A Novel Fault-Tolerant Routing Technique for Mesh-of-Tree based Network-on-Chip Design*, Mohit Upadhyay, **Monil Shah**, P Veda Bhanu, J Soumya, Linga Reddy Cenkeramaddi, Henning Idsøe, IEEE TENCON 2018
- *Fault Tolerant Routing Methodology for Mesh-of-Tree based Network-on-Chips using Local Reconfiguration*, Mohit Upadhyay, **Monil Shah**, P Veda Bhanu, J Soumya, Linga Reddy Cenkeramaddi, International Conference on High Performance Computing and Simulation, HPCS 2018
- *A Novel Fault-Tolerant Routing Algorithm for Mesh-of-Tree Based Network-on-Chips*, **Monil Shah**, Mohit Upadhyay, P Veda Bhanu, J Soumya, Linga Reddy Cenkeramaddi, 22nd International Symposium on VLSI Design and Test, VDAT 2018

Teaching Experience

CSE 140 - Components and Design Techniques for Digital Systems *University of California San Diego*

Mentor : Prof. Tajana Simunic Rosing. *Jan 2022 - Present*

- Responsible for designing HW and Exam questions and solving them
- Responsible for answering on piazza, holding discussion sessions, office hours and grading for a class of 260 undergraduate students

Microprocessors and Interfacing *BITS Pilani*

Mentor : Dr. Soumya J. *Jan 2018 - May 2018*

- One of the Teaching Assistant for Course on Microprocessors with a strength of around 400 Students.
- Responsible for Labwork supervision and mentoring and assisted in End-Semester Grading

Projects

Modelling Branch Predictor and L1 Cache *University of Califonia San Diego*

Mentor: Prof. Jishen Zhao. *Sep 2021 - Dec 2021*

- Modelled various branch predictors like Gshare, Tournament, Perceptron, Gselect, Yeh-Patt, TAGE in C
- Modelled L1 Cache structure with FiFo Replacement policy in C.

Mapping of VGGnet Convolution Layer on 8*8 Systolic Array *University of Califonia San Diego*

Mentor: Prof. Mingu Kang. *Sep 2021 - Dec 2021*

- Implemented and mapped multiple layers of VGGnet neural network by tiling on a 8*8 2D systolic array designed in Verilog.
- Optimized the Inference portion by applying Quantization and Pruned the weights to implement clock gating and reduce overall dynamic power consumption

Fault Tolerant Network-on-Chips *BITS Pilani*

Mentor: Dr. Soumya J. *Aug 2017 - Dec 2017*

- Devised and modelled static scheduling algorithm to support packet routing on a Mesh-of-Tree Topology based NoC under Router faults ensuring scalability in topology size.
- By modelling a two-phase approach of mapping and reconfiguration using additional hardware, the distance between communicating cores was reduced thereby reducing intercommunication latency.

Pipelined Processor Design *BITS Pilani*

Mentor: Dr. Chetan Kumar V. *Jan 2017 - May 2017*

- Designed a 5-stage Pipelined MIPS Processor in Verilog supporting limited instructions and logic to counter Control/Data Hazards arising due to dependencies

Relevant Courses

M.S. Courses: Advanced Computer Architecture, GPU Programming using CUDA, Principles in Computer Architecture (CSE 240A), Low Power VLSI implementation of Machine Learning Algorithm (ECE 284), VLSI Digital System Algorithm and Architecture (ECE 260A)

B.E. Courses: Introduction to Operating Systems, FPGA Systems Design , Computer Architecture, Analog and Digital VLSI Design, Microprocessors and Interfacing, Embedded System Design, Digital Design

Technical Strengths

Programming Languages:: C/C++, Shell, Perl, Verilog, System Verilog

Tools & Simulators:: Xilinx Vivado, Synopsys Design Compiler, Arduino, Modelsim, Quartus Prime

Responsibilities

Head of Dept of Technical Arts: Managed department of over 60 students with focus on design Creatives, Website development and Application development for College Fest. We helped achieve a footfall over 10,000 and Social Outreach of 100,000 *BITS Pilani*

2014 **Head Boy, Student's Council**: As Head Boy and part of Student Representative Council for the academic year 2013-14, I was the point of contact of students to administration and worked closely with teachers and students for coordinating curricular and extracurricular activities. *DPS Surat*