1. Programs that translate symbolic notation to binary is called…… [0.5]
   Ans: Assembler

2. Sign extension is a step in [0.5]
   A) floating point multiplication B) Signed 16 bit integer addition
   B) Arithmetic left shift C) Converting a signed integer from one size to another

3. If hexadecimal representation of a MIPS instruction is $(02324020)_{16}$. Give the actual MIPS instruction. [1]
   Ans: Add $to,$S1, $S2

4. Suppose we have a 32 bit quantity written as A3BC12CD. CD is stored in the smallest addrss. And A3 is stored in the largest address. This alignment restriction is called…….. [1]
   Ans: Little Endian

5. The 16-bit 2's complement representation of an integer is 1111 1111 1111 0101.
   Its decimal representation is…….. [1]

   Ans: -11.0

6. When a program tries to access a page that is mapped in address space but not loaded in physical memory, then
   A) segmentation fault occurs B) fatal error occurs [1]
   C) page fault occurs D) no error occurs

7. ……...algorithm chooses the page that has not been used for the longest period of time whenever the page required to be replaced. [1]
   Ans: Least recently used

8. Working set model for page replacement is based on the assumption of…….. [1]
   A)Modularity B) Locality C) Globalization D) random access

9. Performance of a pipelined processor suffers if [1]
   A) The pipeline stages have different delays. B) Consecutive instructions are dependent on each other.
   C) The pipeline stages share hardware resources. D) All of the above

10. For the following combination of instruction, identify whether any hazard(s) exist. I f there is a hazard, write the hazard name, number of stall cycles for, with and without data forwarding . Justify your answer.

A) lw $S1,16($S2)

addi $S3, $S1, 4

i) <u>without data forwarding:</u> [1]

State whether hazard exist or not: **yes** If yes give the hazard name: DATA HAZARD Number of stall cycles:2

Justification with pipeline stages:

IF ID EX MEM WB

IF ID EX MEM WB

ii) <u>with data forwarding:</u> [1]

State whether hazard exist or not: **No** If yes give the hazard name: DATA HAZARD Number of stall cycles:1

Justification with pipeline stages:

IF ID EX MEM WB

IF ID EX MEM WB

B) addi $S0, $S0, 5

beq $S0, $S1, L1

i) without data forwarding: [1]

State whether hazard exist or not: **YES** If yes give the hazard name: DATA HAZARD Number of stall cycles: 2

Justification with pipeline stages:

IF ID EX MEM WB

IF ID EX MEM WB

ii) with data forwarding: [1]

State whether hazard exist or not: **No** If yes give the hazard name: Number of stall cycles: 0

Justification with pipeline stages:

IF ID EX MEM WB

IF ID EX MEM WB

11. Consider two different implementations, M1 and M2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. M1 has a clock rate of 80 MHz and M2 has a clock rate of 100 MHz. The average number of cycles for each instruction class and their frequencies (for a typical program) are as follows:

Instruction Class	Machine M1 – Cycles/Instruction Class	Machine M2 – Cycles/Instruction Class	Frequency
A	1	2	60%
B	2	3	30%
C	4	4	10%

(a) Calculate the average CPI for each machine, M1, and M2. [1]

For Machine M1:

Clocks per Instruction = (60/100)* 1 + (30/100)*2 + (10/100)*4 = 1.6

For Machine M2:

Clocks per Instruction = (60/100)*2 + (30/100)*3 + (10/100)*4 = 2.5

(b) Calculate the average MIPS ratings for each machine, M1 and M2. [1]

For Machine M1:

Average MIPS rating = Clock Rate/(CPI * 106)= (80 * 106) / (1.6*106)= 50.0

For Machine M2:

Average MIPS rating = Clock Rate/(CPI * 106)= (100 * 106) / (2.5*106)= 40.0

(c) Which machine has a smaller MIPS rating? Which individual instruction class CPI do you need to change, and by how much, to have this machine have the same or better performance as the machine with the higher MIPS rating (you can only change the CPI for one of the instruction classes on the slower machine)? [1]

Machine M2 has a smaller MIPS rating. If we change the CPI of instruction class A for Machine M2 to 1, we can have a better MIPS rating than M1 as follows:

Clocks per Instruction = (60/100)*1 + (30/100)*3 + (10/100)*4= 1.9Average MIPS rating

= Clock Rate/(CPI * 106

= (100 * 106) / (1.9*106)

= 52.6

12. In the IEEE floating point representation the hexadecimal value 0x000000000 corresponds to…… [1.5]

C) The normalized value 2^{-127} B) The normalized value 2^{-126}

D) The normalized value +0 D) The special value +0

Justify your answer

S	BE	M	Value
0/1	All 0's	All 0's	0
0	All 1's	All 0's	+∞
1	All 1's	All 0's	-∞
0/1	All 1's	Non zero	NaN

13. If a computer B runs a program in 8 seconds and computer A runs a program in 16 seconds. How much faster is B than A? [1.5]

Pb/ Pa=16/8=2; Pb=2 Pa

14. Assume that the variables i, and j are assigned to registers $s0, and $s1 respectively. For the C statement below, give the corresponding MIPS assembly code . [2]

```
if ( i == j )
 i++ ;
else
  j-- ;
j += i ;
```

Ans:
```
bne  $r1, $r2, ELSE   # branch if ! ( i == j )
addi $r1, $r1, 1      # i++
 j L1                 # jump over else  (ADD THIS!!!)
ELSE: addi $r2, $r2, -1     # j--
L1:   add $r2, $r2, $r1     # j += i
```

15. Find the average memory access time for a processor with a 2ns clock cycle time , a miss penalty of 40 clock cycles, a miss rate of 0.05 misses per instruction, and a cache access time (including hit detection) of 2 clock cycle. Assume that the read and write miss penalties are same and ignore other write stalls. [2]

Answer with necessary steps:

AmAT= time for hit+ miss rate *miss penality

=2+0.05*40

= 4

16. The decimal value 0.5 in IEEE single precision floating point representation has……. [2]

(A) fractional bits of 000…000 and exponent value of 0

(B) fractional bits of 000…000 and exponent value of −1

(C) fractional bits of 100…000 and exponent value of 0

(D) no exact representation

Justify your answer:

17. In a paged memory hit ratio is 70% and it takes 30 ns to search in TLB and 100 ns to access memory. Effective memory access time is…….. [2.5]

Justify your answer:

EMA= hit ratio* (TLB access time + memory access time)+ miss ratio * (TLB access time +2* memory access time)

=0.7(30+100)+0.3(30+2*100)

=91+69=**160ns**

18. The value of a float type variable is represented using the single-precision 32-bit floating point format of IEEE-754 standard that uses 1 bit for sign, 8 bits for biased exponent and 23 bits for mantissa. A float type variable X is assigned the decimal value of −14.25. The representation of X in hexadecimal notation is……

Ans: **C1640000**

Justify your answer : [2.5]

Since No is negative S bit will be 1
Convert 14.25 into binary 1110.01
Normalize it : 1.11001 X 2 ^ 3
Biased Exponent (Add 127) : 3 + 127 = 130 (In binary 10000010)
Mantissa : 110010.....0 (Total 23 bits)
Num represented in IEEE 754 single precision format :
1 10000010 11001000000000000000000

19. Suppose we have two implementations of the same instruction set architecture. Computer A has a clock cycle time of 250 ps and a CPI of 2.0 for some program, and computer B has a clock cycle time of 500 ps and a CPI of 1.2 for the same program. Which computer is faster for this program, and by how much? [2.5]

I = no. of instructions for the program

CPU clock cycles$_A$ = I × 2.0 ; CPU clock cycles$_B$ = I × 1.2

Now we can compute CPU time for each computer.

CPU time$_A$ = CPU clock cycles$_A$ × clock cycle time

I × 2.0 × 250 ps = 500 × I ps

Likewise for B,

I × 1.2 × 500 ps = 600 × I ps

Clearly A is faster. The amount faster is given by ratio of execution times.

CPU performance$_A$ / CPU performance$_B$ = Execution time$_B$ / Execution time$_A$ = (600 × I ps) / (500 × I ps) = 1.2

A is 1.2 times faster than B.

20. Assume an instruction cache miss rate for a program is 2% and a data cache miss rate is 4%. If a processor has a CPI of 2 without any memory stalls and the miss penalty is 100 cycles for all misses, determine how much faster a processor would run with a perfect cache that never missed. Assume the frequency of all loads and stores is 36% [2.5]

Justify your answer:

Instruction cache miss rate = 2%; Data cache miss rate = 4% ; Processor cycles per instruction(CPI) = 2 (without memory stalls) ; Miss penalty = 100 cycles, ; 36% of instructions are loads and stores

How much faster would the processor run if the cache never missed?

Assume I = total instruction count

Instruction miss cycles = I * 2% * 100 = 2*I

Data miss rate - What programs?

Specint2000 benchmark (36% instructions are loads/stores)

Data miss = I* 36% * 4% *100 = 1.44*I

Memory stall cycles = 1.44*I + 2*I = 3.44*I

CPU execution time per inst = 3.44 + 2 = 5.44, vs. 2 for perfect cache

Performance = 5.44/2 = **2.72** faster for a system with a perfect cache

21. A 4-way set-associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. The number of bits for the TAG field is _____ [2.5]

A) 5 B)15 C)20 D)25

Justify your answer:

In a k-way set associate mapping, cache memory is divided into sets, each of size k blocks.
Size of Cache memory = 16 KB; As it is 4-way set associative,K = 4
Block size B = 8 words; The word length is 32 bits.
size of Physical address space = 4 GB.

No of blocks in Cache Memory(N) = (size of cache memory / size of a block)

= (16*1024 bytes / 8*4 bytes) = 512 (as 1 word = 4 bytes)

No of sets(S) = (No of blocks in cache memory/ no of blocks in a set)

= N/K = 512/4 = 128

Now,size of physical address = 4GB = 4*(2^30) Bytes = 2^32 Bytes

These physical adresses are divided equally among the sets.

Hence, each set can access ((2^32)/128) bytes = 2^25 bytes = 2^23 words = 2^20 blocks

So, each set can access total of 2^20 blocks. So to identify these 2^20 blocks, each set needs TAG bits of length 20 bits.

22. Calculate the total execution time by drawing the pipeline diagram for the code below,if it runs on a five stage pipelined processor with data forwarding circuitry. [2.5]

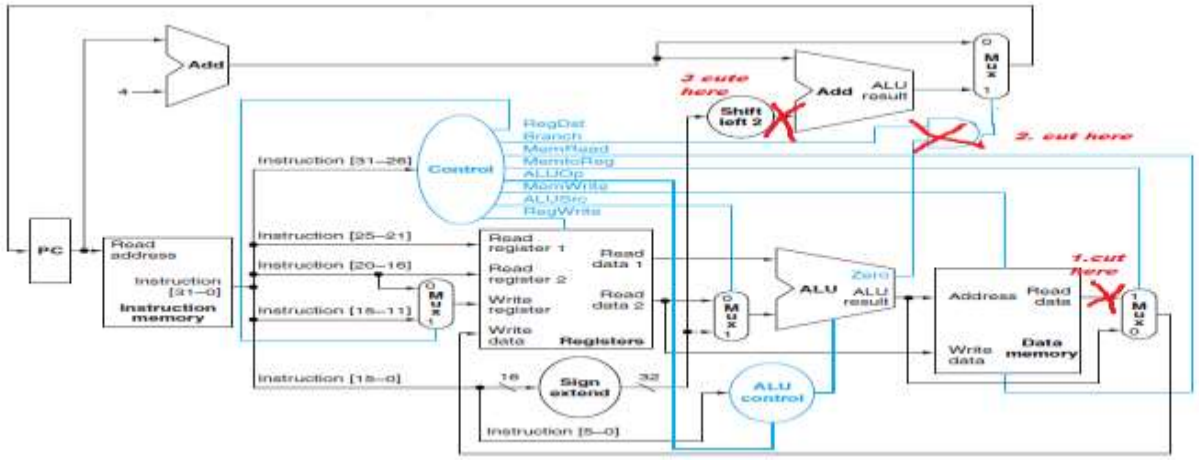
```
add $S1, $S2, $S3
sw  $S1, 0($S2)
add $S2, $S2, $S3
```

Total execution time in number of clock cycles neded: 7

Justify your answer

```
IF  ID EX MEM WB
    IF  ID EX MEM WB
        IF  ID EX MEM WB
```

23. For the MIPS datapath shown below, several lines are marked with “X”.



A) **Cut1** **[3]**

Describe in words the negative consequence of cutting this line relative to the working,

Cannot write to register file. This means that R-type and any instruction with write back to register file will fail.

Provide a snippet of code that will fail

add $s1, $s2, $s3

Provide a snippet of code that will still work

sw $s1, 0($s2)

B) **Cut2** **[2]**

Describe in words the negative consequence of cutting this line relative to the working,

C) **Cut3** **[3]**

Describe in words the negative consequence of cutting this line relative to the working,

Jumping to a branch target does not work.

Provide a snippet of code that will fail

addi $s1, $zero, 2

addi $s2, $zero, 2

beq $s1, $s2, exit

Provide a snippet of code that will still work

addi $s1, $zero, 10

addi $s2, $zero, 20

beq $s1, $s2, exit

24. In a paged memory if the page hit ratio is 0.35. The time required to access a page from secondary memory is 100ns. The time required to access a page from primary memory is 10ns. The average time required to access a page is…… [3]

Justify your answer:

EMA=Hit ratio*primary memory aceess time+ miss ratio* seconddary memory access time

= 0.35*10+0.65*100=**68.5ns**