Name:_____ **Roll No. :**_____ **Sl No. :**____

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY, CALICUT

CSCS2004 : Computer Organization – End Semester Examination (Winter 2016-'17)

Time: 3hr ***Max Marks: 50***

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1. Programs that translate symbolic notation to binary is called_____ [0.5]

2. Sign extension is a step in [0.5]

   ☐ Floating point multiplication ☐ Arithmetic left shift

   ☐ Signed 16 bit integer addition ☐ Converting a signed integer from one size to another

3. If hexadecimal representation of a MIPS instruction is $(02324020)_{16}$. Give the actual MIPS instruction. [1]

   Ans:

4. Suppose we have a 32 bit quantity written as A3BC12CD. CD is stored in the smallest address. And A3 is stored in the largest address. This alignment restriction is called _____ [1]

5. The 16-bit 2s complement representation of an integer is 1111 1111 1111 0101. Its decimal representation is

   _____ [1]

6. When a program tries to access a page, mapped in address space but not loaded in physical memory,then [1]

   ☐ Segmentation fault occurs. ☐ Page fault occurs.

   ☐ Fatal error occurs. ☐ No error occurs.

7. _____ algorithm chooses the page that has not been used for the longest period of time whenever the page required to be replaced. [1]

8. Working set model for page replacement is based on the assumption of _____ [1]

   ☐ Modularity. ☐ Globalization.

   ☐ Locality. ☐ Random access.

9. Performance of a pipelined processor suffers if [1]

   ☐ The pipeline stages have different delays. ☐ Consecutive instructions are dependent on each other.

   ☐ The pipeline stages share hardware resources. ☐ All of the above

10. For the following combination of instruction, identify whether any hazard(s) exist. I f there is a hazard, write the hazard name, number of stall cycles for, with and without data forwarding . Justify your answer.

    A)
    ```
    lw   $S1,16($S2)
    addi $S3, $S1,4
    ```

    (a) Without data forwarding: [1]
    Whether hazard exist or not:____ If yes, hazard name : _____ No.of stall cycles:____
    Justification with pipeline stages:

(b) With data forwarding: [1]
Whether hazard exist or not:_____ If yes, hazard name : _____ No.of stall cycles:_____
Justification with pipeline stages:

B)
```
addi $S0, $S0, 5
beq  $S0, $S1, L1
```

(a) Without data forwarding: [1]
Whether hazard exist or not:_____ If yes, hazard name : _____ No.of stall cycles:_____
Justification with pipeline stages:

(b) With data forwarding: [1]
Whether hazard exist or not:_____ If yes, hazard name : _____ No.of stall cycles:_____
Justification with pipeline stages:

11. Consider two different implementations, M1 and M2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. M1 has a clock rate of 80 MHz and M2 has a clock rate of 100 MHz. The average number of cycles for each instruction class and their frequencies (for a typical program) are as follows:

Instruction Class	Machine M1 Cycles/Instruction Class	Machine M2 Cycles/Instruction Class	Frequency
A	1	2	60%
B	2	3	30%
C	4	4	10%

(a) Calculate the average CPI for each machine, M1, and M2. [1]
For Machine1 :

For Machine2 :

(b) Calculate the average MIPS ratings for each machine, M1 and M2. [1]
For Machine1 :

For Machine2 :

(c) Which machine has a smaller MIPS rating? Which individual instruction class CPI do you need to change, and by how much, to have this machine have the same or better performance as the machine with the higher MIPS rating (you can only change the CPI for one of the instruction classes on the slower machine)? [1]

12. In the IEEE floating point representation the hexadecimal value 0x000000000 corresponds to_____ [1.5]

- ☐ The normalized value 2^{-127}
- ☐ The normalized value +0
- ☐ The normalized value 2^{-126}
- ☐ The special value +0

Justify your answer

13. If a computer B runs a program in 8 seconds and computer A runs a program in 16 seconds. How much faster is B than A? [1.5]

14. Assume that the variables i, and j are assigned to registers $s0, and $s1 respectively. For the C statement below, give the corresponding MIPS assembly code . [2]

C Code	Equivalent MIPS Instruction

`if(i==j)`
`  i++;`
`else`
`  j--;`
`j+= i ;`	

15. Find the average memory access time for a processor with a 2ns clock cycle time , a miss penalty of 40 clock cycles, a miss rate of 0.05 misses per instruction, and a cache access time (including hit detection) of 2 clock cycle. Assume that the read and write miss penalties are same and ignore other write stalls. Answer with necessary steps: [2]

16. The decimal value 0.5 in IEEE single precision floating point representation has_____ [2]

- ☐ fraction bits of 00..00 and exponent value of 0
- ☐ fraction bits of 10..00 and exponent value of 0
- ☐ fraction bits of 00..00and exponent value of -1
- ☐ no exact representation

Justify your answer:

17. In a paged memory hit ratio is 70% and it takes 30 ns to search in TLB and 100 ns to access memory. Effective memory access time is_____. Justify your answer: [2.5]

18. The value of a float type variable is represented using the single-precision 32-bit floating point format of IEEE-754 standard that uses 1 bit for sign, 8 bits for biased exponent and 23 bits for mantissa. A float type variable X is assigned the decimal value of -14.25. The representation of X in hexadecimal notation is_____ ? Justify your answer [2.5]

19. Suppose we have two implementations of the same instruction set architecture. Computer A has a clock cycle time of 250 ps and a CPI of 2.0 for some program, and computer B has a clock cycle time of 500 ps and a CPI of 1.2 for the same program. Which computer is faster for this program, and by how much? [2.5]

20. Assume an instruction cache miss rate for a program is 2% and a data cache miss rate is 4%. If a processor has a CPI of 2 without any memory stalls and the miss penalty is 100 cycles for all misses, determine how much faster a processor would run with a perfect cache that never missed. (Assume the frequency of all loads and stores is 36%) Justify your answer: [2.5]

21. A 4-way set-associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. The number of bits for the TAG field is [2.5]

☐ 5 ☐ 15 ☐ 20 ☐ 25

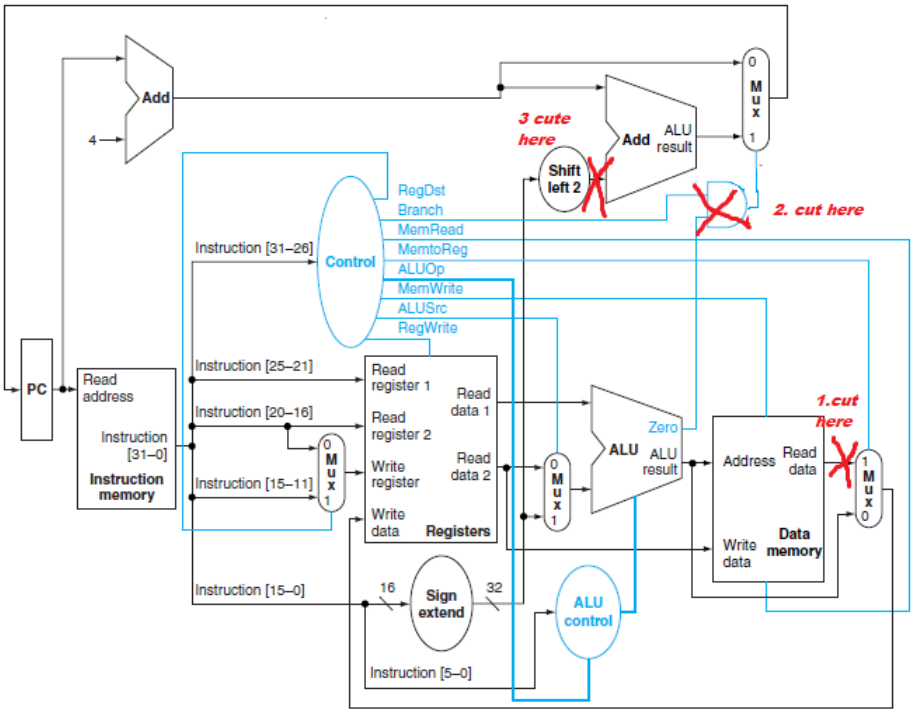
Justify your answer:

22. Calculate the total execution time by drawing the pipeline diagram for the code below,if it runs on a five stage pipelined processor with data forwarding circuitry. [2.5]

```
add  $S1 , $S2 , $S3
sw   $S1 , 0($S2)
add  $S2 , $S2 , $S3
```

Total execution time in number of clock cycles neded:_____
Justify your answer

23. For the MIPS datapath shown below, several lines are marked with X.



A) **Cut1** [3]
Describe in words the negative consequence of cutting this line relative to the working.

Provide a snippet of code that will fail

Provide a snippet of code that will still work

B) **Cut2** [2]
Describe in words the negative consequence of cutting this line relative to the working.

C) **Cut3** [3]
Describe in words the negative consequence of cutting this line relative to the working.

Provide a snippet of code that will fail.

Provide a snippet of code that will still work.

24. In a paged memory if the page hit ratio is 0.35. The time required to access a page from secondary memory is 100ns. The time required to access a page from primary memory is 10ns. The average time required to access a page is_____. Justify your answer: [3]