

COMPUTER ORGANIZATION AND DESIGN



The Hardware/Software Interface

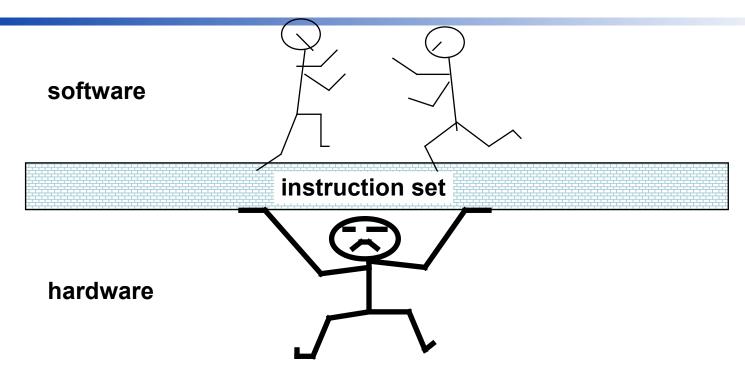
Chapter 2

Instructions: Language of the Computer

Instruction Set

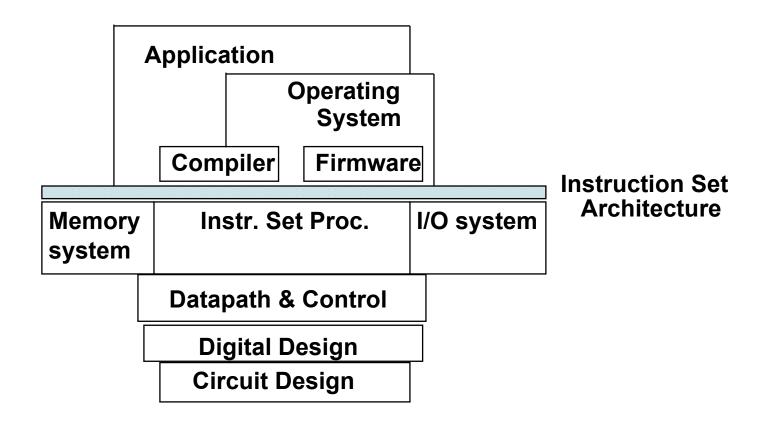
- The repertoire of instructions of a computer
- Different computers have different instruction sets
 - But with many aspects in common
- Early computers had very simple instruction sets
 - Simplified implementation
- Many modern computers also have simple instruction sets

Instruction Set Architecture



- One of the most important abstractions is ISA
 - A critical interface between HW and SW
 - Example: MIPS

How does the pieces fit together



The MIPS Instruction Set

- Used as the example throughout the book
- Stanford MIPS commercialized by MIPS Technologies (www.mips.com)
- Large share of embedded core market
 - Applications in consumer electronics, network/storage equipment, cameras, printers, ...
- Typical of many modern ISAs
 - See MIPS Reference Data tear-out card, and Appendixes B and E

Arithmetic Operations

- Add and subtract, three operands
 - Two sources and one destination
 - add a, b, c # a gets b + c
- All arithmetic operations have this form

Arithmetic Example

C code:

```
f = (g + h) - (i + j);
```

Compiled MIPS code:

```
add t0, g, h # temp t0 = g + h add t1, i, j # temp t1 = i + j sub f, t0, t1 # f = t0 - t1
```

Register Operands

- Arithmetic instructions use register operands
- MIPS has a 32 × 32-bit register file
 - Use for frequently accessed data
 - Numbered 0 to 31
 - 32-bit data called a "word"
- Assembler names
 - \$t0, \$t1, ..., \$t9 for temporary values
 - \$s0, \$s1, ..., \$s7 for saved variables

Name	Register number	Usage		
\$zero	0	the constant value 0		
\$v0-\$v1	2-3	values for results and expression evaluation		
\$a0-\$a3	4-7	arguments		
\$t0-\$t7	8-15	temporaries		
\$s0-\$s7	16-23	saved		
\$t8-\$t9	24-25	more temporaries		
\$gp	28	global pointer		
\$sp	29	stack pointer		
\$fp	30	frame pointer		
\$ra	31	return address		

Register 1 (\$at) reserved for assembler, Registers 26-27 for operating system

Register Operand Example

C code:

```
f = (g + h) - (i + j);

• f, ..., j in $s0, ..., $s4
```

Compiled MIPS code:

```
add $t0, $s1, $s2
add $t1, $s3, $s4
sub $s0, $t0, $t1
```

C code: A = B + C + D; E = F - A;MIPS code: add \$t0, \$s1, \$s2 add \$s0, \$t0, \$s3 sub \$s4, \$s5, \$s0

What about programs with lots of variables?

Memory Organization

- Viewed as a large, single-dimension array, with an address.
- A memory address is an index into the array

"Byte addressing" means that the index

points to a byte of memory.

1,	GCA
)	8 bits of data
	8 bits of data
2	8 bits of data
3	8 bits of data
1	8 bits of data
5	8 bits of data
6	8 bits of data

...

Memory Operands

- Main memory used for composite data
 - Arrays, structures, dynamic data
- To apply arithmetic operations
 - Load values from memory into registers
 - Store result from register to memory
- Memory is byte addressed
 - Each address identifies an 8-bit byte
- Words are aligned in memory
 - Address must be a multiple of 4
- MIPS is Big Endian
 - Most-significant byte at least address of a word
 - c.f. Little Endian: least-significant byte at least address

Memory Operand Example 1

C code:

```
g = h + A[8];
```

- g in \$s1, h in \$s2, base address of A in \$s3
- Compiled MIPS code:
 - Index 8 requires offset of 32
 - 4 bytes per word

Memory Operand Example 2

C code:

```
A[12] = h + A[8];
```

- h in \$s2, base address of A in \$s3
- Compiled MIPS code:
 - Index 8 requires offset of 32

```
lw $t0, 32($s3)  # load word
add $t0, $s2, $t0
sw $t0, 48($s3)  # store word
```

Registers vs. Memory

- Registers are faster to access than memory
- Operating on memory data requires loads and stores
 - More instructions to be executed
- Compiler must use registers for variables as much as possible
 - Only spill to memory for less frequently used variables
 - Register optimization is important!

Immediate Operands

- Constant data specified in an instruction addi \$s3, \$s3, 4
- No subtract immediate instruction
 - Just use a negative constant addi \$s2, \$s1, -1
- Design Principle : Make the common case fast
 - Small constants are common
 - Immediate operand avoids a load instruction

The Constant Zero

- MIPS register 0 (\$zero) is the constant 0
 - Cannot be overwritten
- Useful for common operations
 - E.g., move between registers add \$t2, \$s1, \$zero

MIPS R-format Instructions

ор	rs	rt	rd	shamt	funct
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits

- Instruction fields
 - op: operation code (opcode)
 - rs: first source register number
 - rt: second source register number
 - rd: destination register number
 - shamt: shift amount (00000 for now)
 - funct: function code (extends opcode)

R-format Example

ор	rs	rt	rd	shamt	funct
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits

add \$t0, \$s1, \$s2

special	\$s1	\$s2	\$t0	0	add
0	17	18	8	0	32
000000	10001	10010	01000	00000	100000

 $00000100011001001001000000100000_2 = 02324020_{16}$

MIPS I-format Instructions

ор	rs	rt	constant or address
6 bits	5 bits	5 bits	16 bits

- Immediate arithmetic and load/store instructions
 - rt: destination or source register number
 - Constant: -2¹⁵ to +2¹⁵ 1
 - Address: offset added to base address in rs
 - Different formats complicate decoding, but allow 32-bit instructions uniformly
 - Keep formats as similar as possible
 - Iw \$t0,32(\$s3) |35|19|8|32|

So far we've learned: (p.59)

MIPS

- loading words but addressing bytes
- arithmetic on registers only

Instruction

add \$s1, \$s2, \$s3 sub \$s1, \$s2, \$s3 addi \$s1, \$s2,100 lw \$s1, 100(\$s2) sw \$s1, 100(\$s2)

Meaning

```
$s1 = $s2 + $s3

$s1 = $s2 - $s3

$s1 = $s2 + 100

$s1 = Memory[$s2+100]

Memory[$s2+100] = $s1
```

MIPS instruction encoding

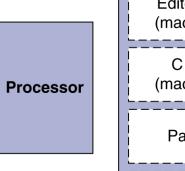
Instruction	Format	ор	rs	rt	rd	shamt	funct	address
add	R	0	reg	reg	reg	0	32 _{ten}	n.a.
sub (subtract)	R	0	reg	reg	reg	0	34 _{ten}	n.a.
add immediate	I	8 _{ten}	reg	reg	n.a.	n.a.	n.a.	constant
ไพ (load word)	I	35 _{ten}	reg	reg	n.a.	n.a.	n.a.	address
sw (store word)	I	43 _{ten}	reg	reg	n.a.	n.a.	n.a.	address

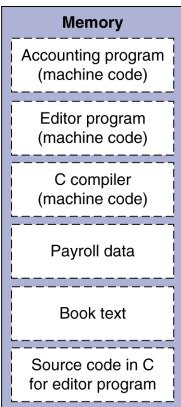
- A[300] = h + A[300];
 - is compiled to
- Iw \$t0,1200(\$t1)
- add \$t0,\$s2,\$t0
- sw \$t0,1200(\$t1)

ор	rs	rt	rd	address/ shamt	funct
35	9	8		1200	
0	18	8	8	0	32
43	9	8		1200	

Stored Program Computers

The BIG Picture





- Instructions represented in binary, just like data
- Instructions and data stored in memory
- Programs can operate on programs
 - e.g., compilers, linkers, ...
- Binary compatibility allows compiled programs to work on different computers
 - Standardized ISAs

Stored Program Concept

- Instructions are bits
- Programs are stored in memory
 - to be read or written just like data
- Fetch & Execute Cycle
 - Instructions are fetched and put into a special register
 - Bits in the register "control" the subsequent actions
 - Fetch the "next" instruction and continue

Logical Operations

Instructions for bitwise manipulation

Operation	С	Java	MIPS
Shift left	<<	<<	s11
Shift right	>>	>>>	srl
Bitwise AND	&	&	and, andi
Bitwise OR			or, ori
Bitwise NOT	~	~	nor

Useful for extracting and inserting groups of bits in a word

- 0000 0000 00000 000 0000 0000 1001two= 9_{ten}
- 9<<4
- 0000 0000 0000 0000 0000 1001 0000two= 144_{ten}
- sll \$t2,\$s0,4

shamt: how many positions to shift

Shift Operations

ор	rs	rt	rd	shamt	funct
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits

- Shift left logical
 - Shift left and fill with 0 bits
 - s11 by i bits multiplies by 2i
- Shift right logical
 - Shift right and fill with 0 bits
 - srl by i bits divides by 2i (unsigned only)

op	rs	rt	rd	shamt	funct	
0	0	16	10	4	0	

AND Operations

- Useful to mask bits in a word
 - Select some bits, clear others to 0

```
and $t0, $t1, $t2
```

```
$t2 | 0000 0000 0000 0000 00<mark>00 11</mark>01 1100 0000
```

\$t0 | 0000 0000 0000 0000 1100 0000 0000

OR Operations

- Useful to include bits in a word
 - Set some bits to 1, leave others unchanged

```
or $t0, $t1, $t2
```

NOT Operations

- Useful to invert bits in a word
 - Change 0 to 1, and 1 to 0
- MIPS has NOR 3-operand instruction
 - a NOR b == NOT (a OR b)

```
nor $t0, $t1, $zero ←
```

Register 0: always read as zero

```
$t1 | 0000 0000 0000 0001 1100 0000 0000
```

\$t0 | 1111 1111 1111 1100 0011 1111 1111

MIPS operands

Name	Example	Comments
32	\$s0,\$s1,,\$s7	Fast locations for data. In MIPS, data must be in registers to perform arithmetic.
registers	\$t0,\$t1,,\$t7	Registers \$s0-\$s7 map to 16–23 and \$t0-\$t7 map to 8–15.
2 ³⁰	Memory[0],	Accessed only by data transfer instructions. MIPS uses byte addresses, so
memory	Memory[4], ,	sequential word addresses differ by 4. Memory holds data structures, arrays, and
words	Memory[4294967292]	spilled registers.

MIPS assembly language

Category	Instruction	Example		Meaning	Comments
Arithmetic	add	add	\$s1,\$s2,\$s3	\$s1 = \$s2 + \$s3	Three operands; overflow detected
	subtract	sub	\$s1,\$s2,\$s3	\$s1 = \$s2 - \$s3	Three operands; overflow detected
	add immediate	addi	\$s1,\$s2,100	\$s1 = \$s2 + 100	+ constant; overflow detected
	and	and	\$s1,\$s2,\$s3	\$s1 = \$s2 & \$s3	Three reg. operands; bit-by-bit AND
	or	or	\$s1,\$s2,\$s3	\$s1 = \$s2 \$s3	Three reg. operands; bit-by-bit OR
	nor	nor	\$s1,\$s2,\$s3	\$s1 = ~ (\$s2 \$s3)	Three reg. operands; bit-by-bit NOR
Logical	and immediate	andi	\$s1,\$s2,100	\$s1 = \$s2 & 100	Bit-by-bit AND reg with constant
	or immediate	ori	\$s1,\$s2,100	\$s1 = \$s2 100	Bit-by-bit OR reg with constant
	shift left logical	sll	\$s1,\$s2,10	\$s1 = \$s2 << 10	Shift left by constant
	shift right logical	srl	\$\$s1,\$s2,10	\$s1 = \$s2 >> 10	Shift right by constant
Data	load word	1w	\$s1,100(\$s2)	\$s1 = Memory[\$s2 + 100]	Word from memory to register
transfer	store word	SW	\$s1,100(\$s2)	Memory[\$s2 + 100] = \$s1	Word from register to memory

MIPS machine language

WIPS macnine language

Name	Format			Comments				
add	R	0	18	19	17	0	32	add \$s1,\$s2,\$s3
sub	R	0	18	19	17	0	34	sub \$s1,\$s2,\$s3
1w	I	35	18	17	100			lw \$s1,100(\$s2)
SW	I	43	18	17	100			sw \$s1,100(\$s2)
and	R	0	18	19	17	0	36	and \$s1,\$s2,\$s3
or	R	0	18	19	17	0	37	or \$s1,\$s2,\$s3
nor	R	0	18	19	17	0	39	nor \$s1,\$s2,\$s3
andi	I	12	18	17	100			andi \$s1,\$s2,100
ori	I	13	18	17	100			ori \$s1,\$s2,100
s11	R	0	0	18	17	10	0	sll \$s1,\$s2,10
srl	R	0	0	18	17	10	2	srl \$s1,\$s2,10
beq	T I	4	17	18	25			beq \$s1,\$s2,100
bne	T.	5	17	18	25			bne \$s1,\$s2,100
slt	R	0	18	19	17	0	42	slt \$s1,\$s2,\$s3
j	J	2			j 10000 (see Section 2.9)			

Conditional Operations

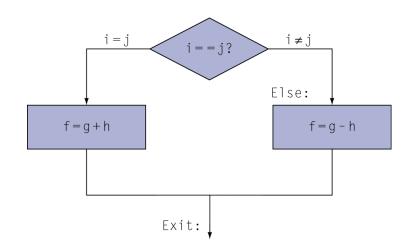
- Branch to a labeled instruction if a condition is true
 - Otherwise, continue sequentially
- beq rs, rt, L1
 - if (rs == rt) branch to instruction labeled L1;
- ullet bne rs, rt, L1
 - if (rs != rt) branch to instruction labeled L1;
- j L1
 - unconditional jump to instruction labeled L1

Compiling If Statements

C code:

Exit: *...

- f, g, ... in \$s0, \$s1, ...
- Compiled MIPS code:



```
bne $s3, $s4, Else
    add $s0, $s1, $s2
    j Exit
Else: sub $s0, $s1, $s2
```

Assembler calculates addresses

Compiling Loop Statements

C code:

```
while (save[i] == k) i += 1;
```

- i in \$s3, k in \$s5, address of save in \$s6
- Compiled MIPS code: ???

Compiling Loop Statements

C code:

```
while (save[i] == k) i += 1;
```

- i in \$s3, k in \$s5, address of save in \$s6
- Compiled MIPS code:

```
Loop: sll $t1, $s3, 2
add $t1, $t1, $s6
lw $t0, 0($t1)
bne $t0, $s5, Exit
addi $s3, $s3, 1
j Loop
```

More Conditional Operations

- Set result to 1 if a condition is true
 - Otherwise, set to 0
- slt rd, rs, rt
 - if (rs < rt) rd = 1; else rd = 0;</pre>
- slti rt, rs, constant
 - if (rs < constant) rt = 1; else rt = 0;</p>
- Use in combination with beq, bne

```
slt $t0, $s1, $s2 # if ($s1 < $s2)
bne $t0, $zero, L # branch to L</pre>
```

Branch Instruction Design

- Why not blt, bge, etc?
- Hardware for <, ≥, ... slower than =, ≠</p>
 - Combining with branch involves more work per instruction, requiring a slower clock
 - All instructions penalized!
- beq and bne are the common case
- This is a good design compromise

Signed vs. Unsigned

- Signed comparison: s1t
- Unsigned comparison: s1tu
- Example

 - slt \$t0, \$s0, \$s1 # signed
 ????
 - sltu \$t0, \$s0, \$s1 # unsigned
 ????

Signed vs. Unsigned

- Signed comparison: s1t
- Unsigned comparison: s1tu
- Example

 - slt \$t0, \$s0, \$s1 # signed
 - $-1 < +1 \Rightarrow $t0 = 1$
 - sltu \$t0, \$s0, \$s1 # unsigned
 - $+4,294,967,295 > +1 \Rightarrow $t0 = 0$

Opcode for instructions

MIPS machine language

mir o macinile ranguage								
Name	Format	Example			Comments			
add	R	0	18	19	17	0	32	add \$s1,\$s2,\$s3
sub	R	0	18	19	17	0	34	sub \$s1,\$s2,\$s3
1w	I	35	18	17		100		lw \$s1,100(\$s2)
SW	I	43	18	17		100		sw \$s1,100(\$s2)
and	R	0	18	19	17	0	36	and \$s1,\$s2,\$s3
or	R	0	18	19	17	0	37	or \$s1,\$s2,\$s3
nor	R	0	18	19	17	0	39	nor \$s1,\$s2,\$s3
andi	I	12	18	17		100		andi \$s1,\$s2,100
ori	I	13	18	17		100		ori \$s1,\$s2,100
s11	R	0	0	18	17	10	0	sll \$s1,\$s2,10
srl	R	0	0	18	17	10	2	srl \$s1,\$s2,10
beq	I	4	17	18		25		beq \$s1,\$s2,100
bne	I	5	17	18		25		bne \$s1,\$s2,100
s1t	R	0	18	19	17	0	42	slt \$s1,\$s2,\$s3
j	J	2		2500 j 10000 (see Section 2.9)				
Field size		6 bits	5 bits	5 bits	5 bits	5 bits	6 bits	All MIPS instructions 32 bits
R-format	R	ор	rs	rt	rd	shamt	funct	Arithmetic instruction format
I-format	I	ор	rs	rt		address	•	Data transfer, branch format

Procedures

- A stored sub-program that performs a specific task based on the parameters with which it is provided
 - It makes the code understandable and allowed the code to be reused.
 - The coder can concentrate on just one portion of task at time, with parameters acting as a barrier
 - Passed values and return values

Procedure Calling

In the execution of the procedure, the program must follow these six steps

- Place parameters in registers
- 2. Transfer control to procedure
- **Acquire storage for procedure**
- 4. Perform procedure's operations
- Place result in register for caller
- Return to place of call

Register Usage

- \$a0 \$a3: arguments (reg's 4 7)
- \$v0, \$v1: result values (reg's 2 and 3)
- \$t0 \$t9: temporaries
 - Can be overwritten by callee
- \$s0 \$s7: saved
 - Must be saved/restored by callee
- \$gp: global pointer for static data (reg 28)
- \$sp: stack pointer (reg 29)
- \$fp: frame pointer (reg 30)
- \$ra: return address (reg 31)

Procedure Call Instructions

- Procedure call: jump and link jal ProcedureLabel
 - Address of following instruction put in \$ra
 - Jumps to target address
- Procedure return: jump register jr \$ra
 - Copies \$ra to program counter
 - Can also be used for computed jumps
 - e.g., for case/switch statements

Leaf Procedure Example

C code:

```
int leaf_example (int g, h, i, j)
{ int f;
    f = (g + h) - (i + j);
    return f;
}
```

- Arguments g, ..., j in \$a0, ..., \$a3
- f in \$s0 (hence, need to save \$s0 on stack)
- Result in \$v0

Leaf Procedure Example

MIPS code:

<pre>leaf_example:</pre>				
addi	\$sp,	\$sp,	-4	
SW	\$s0,	0(\$sp	o)	
add	\$t0,	\$a0,	\$a1	
add	\$t1,	\$a2,	\$a3	
sub	\$s0,	\$t0,	\$t1	
add	\$v0,	\$s0,	\$zero	
٦w	\$s0,	0(\$sp	o)	
addi	\$sp,	\$sp,	4	
jr	\$ra			

Save \$s0 on stack

Procedure body

Result

Restore \$s0

Return

Non-Leaf Procedures

- Procedures that call other procedures
- For nested call, caller needs to save on the stack:
 - Its return address
 - Any arguments and temporaries needed after the call
- Restore from the stack after the call

Non-Leaf Procedure Example

C code:

```
int fact (int n)
{
  if (n < 1) return 1;
  else return n * fact(n - 1);
}</pre>
```

- Argument n in \$a0
- Result in \$v0

Non-Leaf Procedure Example

MIPS code:

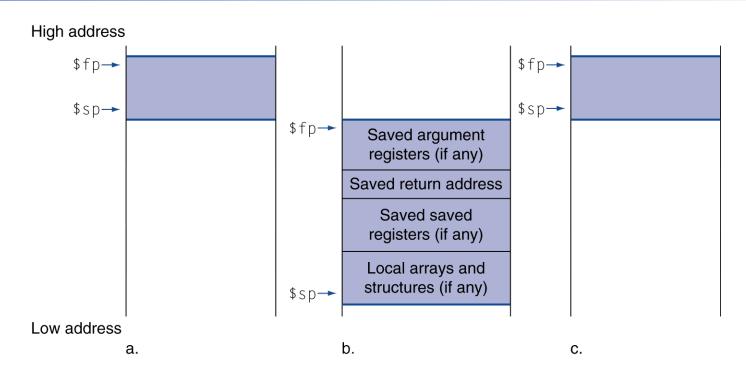
```
fact:
   addi $sp, $sp, -8
                       # adjust stack for 2 items
                        # save return address
   sw $ra, 4($sp)
   sw $a0, 0($sp)
                        # save argument
   slti $t0, $a0, 1
                       # test for n < 1
   beq $t0, $zero, L1
   addi $v0, $zero, 1 # if so, result is 1
   addi $sp, $sp, 8
                        # pop 2 items from stack
   jr $ra
                        # and return
L1: addi $a0, $a0, -1
                        # else decrement n
   jal fact
                        # recursive call
   lw $a0, 0($sp)
                        # restore original n
   lw $ra, 4($sp)
                        # and return address
   addi $sp, $sp, 8
                        # pop 2 items from stack
                        # multiply to get result
        $v0, $a0, $v0
   mul
   jr
        $ra
                        # and return
```

Stack frame – activation record

- The final complexity of stack is to store variables that are local to the procedure that donot fit in registers (eg, arrays etc)
- Stack segment which contains saved registers and local variables is called activation record

MIPS uses frame pointer (\$fp) to point to the first word of the frame. And stack pointer is used to point the variables and registers inside a frame.

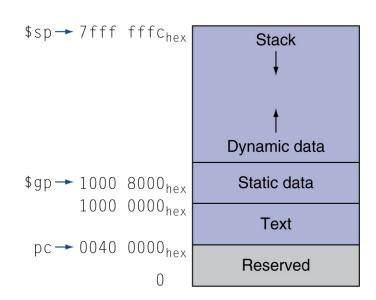
Local Data on the Stack



- Local data allocated by callee
 - e.g., C automatic variables
- Procedure frame (activation record)
 - Used by some compilers to manage stack storage

Memory Layout

- Text: program code
- Static data: global variables
 - e.g., static variables in C, constant arrays and strings
 - \$gp initialized to address allowing ±offsets into this segment
- Dynamic data: heap
 - E.g., malloc in C, new in Java
- Stack: automatic storage
- Memory leak, dangling pointers



Character Data

- Byte-encoded character sets
 - ASCII: 128 characters
 - 95 graphic, 33 control
 - Latin-1: 256 characters
 - ASCII, +96 more graphic characters

Byte/Halfword Operations

- Could use bitwise operations
- MIPS byte/halfword load/store
 - String processing is a common case

```
lb rt, offset(rs) lh rt, offset(rs)
```

Sign extend to 32 bits in rt

```
sb rt, offset(rs) sh rt, offset(rs)
```

Store just rightmost byte/halfword

strings

- Characters are normally combined to strings, which have variable no of chars
- To represent a string, 3 methods are
 - First position of string is reserved to give the length
 - Accompanying variable will have length value
 - The last position of string end indicator.
 - Eg "Cal" 67, 97,108,0

String Copy Example

- C code (naïve):
 - Null-terminated string

```
void strcpy (char x[], char y[])
{ int i;
    i = 0;
    while ((x[i]=y[i])!='\0')
        i += 1;
}
```

- Addresses of x, y in \$a0, \$a1
- i in \$s0

String Copy Example

MIPS code:

```
strcpy:
   addi $sp, $sp, -4 # adjust stack for 1 item
                      # save $s0
   sw $s0, 0($sp)
   add $s0, $zero, $zero # i = 0
L1: add $t1, $s0, $a1 # addr of y[i] in $t1
   1b t2, 0(t1) # t2 = y[i]
   add $t3, $s0, $a0 # addr of x[i] in $t3
   sb t2, 0(t3) # x[i] = y[i]
   beq $t2, $zero, L2 # exit loop if y[i] == 0
   addi $s0, $s0, 1
                        # i = i + 1
                        # next iteration of loop
        L1
L2: 1w $s0, 0($sp)
                        # restore saved $s0
   addi $sp, $sp, 4
                        # pop 1 item from stack
                        # and return
        $ra
   jr
```

Half words

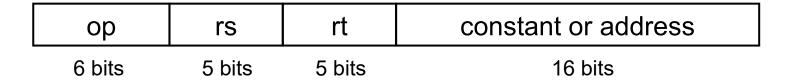
- To load and store 16 bit quanities (half word) MIPS provides you
 - Ih loads half word from memory, placing it in the right most 16 bits of the register
 - sh reverse operation

32-bit Constants

- Most constants are small
 - 16-bit immediate is sufficient
- For the occasional 32-bit constant lui rt, constant
 - Copies 16-bit constant to left 16 bits of rt
 - Clears right 16 bits of rt to 0

Branch Addressing

- Branch instructions specify
 - Opcode, two registers, target address
- Most branch targets are near branch
 - Forward or backward



- PC-relative addressing
 - Target address = PC + offset × 4
 - PC already incremented by 4 by this time

Jump Addressing

- Jump (j and jal) targets could be anywhere in text segment
 - Encode full address in instruction

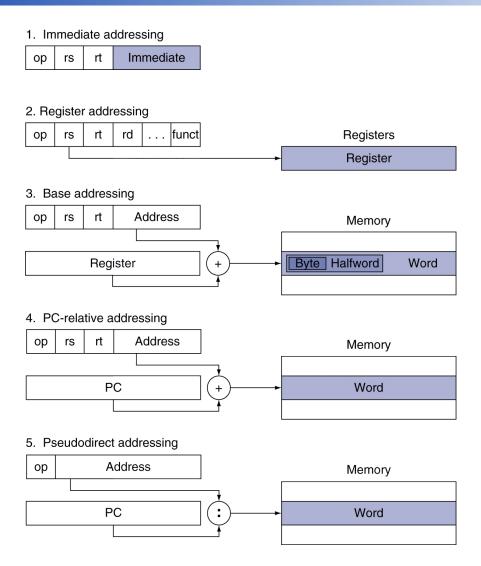
ор	address
6 bits	26 bits

- (Pseudo)Direct jump addressing
 - Target address = PC_{31...28}: (address × 4)

Branching Far Away

- If branch target is too far to encode with 16-bit offset, assembler rewrites the code
- Example

Addressing Mode Summary





COMPUTER OF CENIZATION AND DESIGN



The Hardware/Software Interface

MIPS operands

Name		Example	Comments		
		\$s0-\$s7, \$t0-\$t9, \$zero,	Fast locations for data. In MIPS, data must be in registers to perform		
32 regis	ters	\$a0-\$a3, \$v0-\$v1, \$gp,	arithmetic. MIPS register \$zero always equals 0. Register \$at is		
		\$fp, \$sp, \$ra, \$at	reserved for the assembler to handle large constants.		
		Memory[0],	Accessed only by data transfer instructions. MIPS uses byte addresses, so		
2 ³⁰ me	mory	Memory[4],,	sequential words differ by 4. Memory holds data structures, such as arrays,		
words		Memory[4294967292]	and spilled registers, such as those saved on procedure calls.		

MIPS assembly language

Cate	aorv	Instruction	Example	Meaning	Comments
Arithme		add	add \$s1, \$s2, \$s3	\$s1 = \$s2 + \$s3	Three operands; data in registers
		subtract	sub \$s1, \$s2, \$s3	\$s1 = \$s2 - \$s3	Three operands; data in registers
		add immediate	addi \$s1, \$s2, 100	\$s1 = \$s2 + 100	Used to add constants
	ansfer	load word	lw \$s1, 100(\$s2)	\$s1 = Memory[\$s2 + 100]	Word from memory to register
		store word	sw \$s1, 100(\$s2)	Memory[\$s2 + 100] = \$s1	Word from register to memory
Data tra		load byte	lb \$s1, 100(\$s2)	\$s1 = Memory[\$s2 + 100]	Byte from memory to register
		store byte	sb \$s1, 100(\$s2)	Memory[\$s2 + 100] = \$s1	Byte from register to memory
		load upper immediate	lui \$s1, 100	\$s1 = 100 * 2 ¹⁶	Loads constant in upper 16 bits
	onal	branch on equal	beq \$s1, \$s2, 25	if (\$s1 == \$s2) go to PC + 4 + 100	Equal test; PC-relative branch
Conditi		branch on not equal	bne \$s1, \$s2, 25	if (\$s1 != \$s2) go to PC + 4 + 100	Not equal test; PC-relative
branch		set on less than	slt \$s1, \$s2, \$s3	if (\$s2 < \$s3) \$s1 = 1; else \$s1 = 0	Compare less than; for beq, bne
		set less than immediate	slti \$s1, \$s2, 100	if (\$s2 < 100) \$s1 = 1; else \$s1 = 0	Compare less than constant
		jump	j 2500	go to 10000	Jump to target address
Uncond	i-	jump register	jr \$ra	go to \$ra	For switch, procedure return
tional ju	mp	jump and link	jal 2500	\$ra = PC + 4; go to 10000	For procedure call

Arrays & Pointers in MIPS

C Sort Example

Swap procedure (leaf)
 void swap(int v[], int k)
 {
 int temp;
 temp = v[k];
 v[k] = v[k+1];
 v[k+1] = temp;
 }

v in \$a0, k in \$a1, temp in \$t0

The Procedure Swap

The Sort Procedure in C

- bubble sort function
- Non-leaf (calls swap) void sort (int v[], int n) int i, j; for (i = 0; i < n; i += 1) { for (j = i - 1;j >= 0 && v[j] > v[j + 1];i -= 1) { swap(v,j);
 - v in \$a0, k in \$a1, i in \$s0, j in \$s1

C Sort Example

Swap procedure (leaf)
 void swap(int v[], int k)
 {
 int temp;
 temp = v[k];
 v[k] = v[k+1];
 v[k+1] = temp;
 }

v in \$a0, k in \$a1, temp in \$t0

The Procedure Swap

The Sort Procedure in C

```
Non-leaf (calls swap)
  void sort (int v[], int n)
    int i, j;
    for (i = 0; i < n; i += 1) {
      for (j = i - 1;
            j >= 0 \&\& v[j] > v[j + 1];
            i -= 1) {
        swap(v,j);
```

v in \$a0, n in \$a1, i in \$s0, j in \$s1

The Procedure Body

```
# save $a0 into $s2
       move $s2, $a0
                                                            Move
       move $s3, $a1  # save $a1 into $s3
                                                            params
       move $s0, $zero # i = 0
                                                            Outer loop
for1tst: slt $t0, $s0, $s3 # $t0 = 0 if $s0 \ge $s3 (i \ge n)
       beq t0, zero, exit1 # go to exit1 if s0 \ge s3 (i \ge n)
       addi \$s1, \$s0, -1 # j = i - 1
for2tst: s1ti t0, s1, 0 # t0 = 1 if s1 < 0 (i < 0)
       bne t0, zero, exit2 # go to exit2 if s1 < 0 (j < 0)
       Inner loop
       add $t2, $s2, $t1 # $t2 = v + (j * 4)
       1w $t3, 0($t2) # $t3 = v[j]
       1w $t4, 4($t2) # $t4 = v[j + 1]
       \$1t \$t0, \$t4, \$t3  # \$t0 = 0 if \$t4 \ge \$t3
       beq t0, zero, exit2 # go to exit2 if t4 \ge t3
       move $a0, $s2 # 1st param of swap is v (old $a0)
                                                            Pass
       move $a1, $s1  # 2nd param of swap is j
                                                            params
                           # call swap procedure
       jal swap
                                                            & call
       addi $s1, $s1, -1 # j -= 1
       i for2tst
                                                            Inner loop
                           # jump to test of inner loop
                           # i += 1
       addi $s0, $s0, 1
exit2:
       i for1tst
                           # jump to test of outer loop
                                                            Outer loop
```

The Full Procedure

```
sort:
       addi $sp,$sp, -20 # make room on stack for 5 registers
       sw $ra, 16($sp) # save $ra on stack
       sw $s3,12($sp) # save $s3 on stack
       sw $s2, 8($sp) # save $s2 on stack
       sw $s1, 4($sp) # save $s1 on stack
       sw $s0, 0(\$sp)
                         # save $s0 on stack
                          # procedure body
       exit1: lw $s0, 0($sp) # restore $s0 from stack
       lw $s1, 4($sp) # restore $s1 from stack
       lw $s2, 8($sp) # restore $s2 from stack
       lw $ra,16($sp) # restore $ra from stack
       addi $sp,$sp, 20
                         # restore stack pointer
       jr $ra
                          # return to calling routine
```

Arrays vs. Pointers

- Array indexing involves
 - Multiplying index by element size
 - Adding to array base address
- Pointers correspond directly to memory addresses
 - Can avoid indexing complexity

Example: Clearing and Array

```
clear2(int *array, int size) {
clear1(int array[], int size) {
 int i;
                                           int *p;
 for (i = 0; i < size; i += 1)
                                           for (p = \&array[0]; p < \&array[size];
   arrav[i] = 0:
                                                p = p + 1
                                             *p = 0:
                                         }
      move $t0,$zero
                       # i = 0
                                                move t0,a0 # p = & array[0]
loop1: sll $t1,$t0,2  # $t1 = i * 4
                                                s11 $t1,$a1,2 # $t1 = size * 4
       add $t2,$a0,$t1 # $t2 =
                                                add t2,a0,t1 # t2 =
                       # &array[i]
                                                                   &array[size]
                                         loop2: sw zero,0(t0) \# Memory[p] = 0
       sw zero, 0(t2) # array[i] = 0
       addi $t0,$t0,1 # i = i + 1
                                                addi t0,t0,4 \# p = p + 4
       s1t $t3,$t0,$a1 # $t3 =
                                                s1t $t3,$t0,$t2 # $t3 =
                       # (i < size)
                                                                #(p<&array[size])</pre>
      bne $t3,$zero,loop1 # if (...)
                                                bne $t3,$zero,loop2 # if (...)
                          # goto loop1
                                                                    # goto loop2
```

Concluding Remarks

Measure MIPS instruction

Instruction class	MIPS examples		
Arithmetic	add, sub, addi		
Data transfer	lw, sw, lb, lbu, lh, lhu, sb, lui		
Logical	ori, sll, srl		
Cond. Branch	beq, bne, slt, slti, sltiu		
Jump	j, jr, jal		