Department of Computer Science and Engineering
National Institute of Technology Calicut
Tentative Course Details – Monsoon Semester 2017

CS2001 LOGIC DESIGN

Lecture: B Slot

Lecture Hours : Monday 11.15 am - 12.15 pm, Tuesday 8.00 am – 9.00 am, Thursday 9.00 am - 10.00 am, Friday 2.00 pm - 3.00 pm
Lecture Hall : ELHC 203/401

Instructor:

Name : Athira P K
Office : MB 209 E
Email : athirapk@nitc.ac.in

Course Outcomes:

CO1: Perform the conversion among different number systems.
CO2: Reduce complex logical expressions using various postulates of Boolean algebra.
CO3: Describe graphical methods (like K- Map, Quine-McClusky) for the simplification of complex logical expressions.
CO4: Define and describe basic logic gates.
CO5: Describe design methodology for different combinational logic circuit.
CO6: Describe the structure of various semiconductor programmable logic devices.
CO7: Design concepts of sequential circuits.

Syllabus

Module 1
Number systems and codes, Boolean algebra: postulates and theorems, constants, variables and functions, switching algebra, Boolean functions and logical operations, Karnaugh map: prime cubes, minimum sum of products and product of sums

Module 2
Quine-McClusky algorithm, prime implicant chart, cyclic prime implicant chart, Petrick's method, Combinational Logic: introduction, analysis and design of combinational logic circuits, parallel adders and look-ahead adders, comparators, decoders and encoders, code conversion, multiplexers and de-multiplexers, parity generators and checkers

Module 3
Programmable Logic Devices, ROMs, PALs, PLAs, PLA folding, design for testability. Introduction to sequential circuits, memory elements, latches

Module 4
Flip-flops, analysis of sequential circuits, state tables, state diagrams, design of sequential circuits, excitation tables, Mealy and Moore models, registers, shift registers, counters

References:

1. T. L. Floyd, R. P. Jain, Digital Fundamentals, 8/e, Pearson Education, 2006
2. C. H. Roth, Jr., L. L. Kinney, Fundamentals of Logic Design, 6/e, Cengage Learning, 2009
3. M M Mano, M D Ciletti, Digital Design, 4/e, Pearson Education, 2008
4. N. N. Biswas, Logic Design Theory, Prentice Hall of India, New Delhi, 1993

Grading: Marks Distribution

Mid-Term Exam I	:	20%
Mid-Term Exam II	:	20%
Quizzes/Assignments	:	10%
Final Exam	:	50%

Grading Policy:

- Grading will be relative.
- Even though the grading will be relative here is a tentative grade distribution: 90-100: S, 80-89:A, 70-79: B, 60-69: C, 50-59: D, 40-49: E, 30-39: R, <30: F.
- Absence for exams/quizzes without prior written permission from the instructor will be equivalent to zero marks in the corresponding exam/quiz.
- There will be no makeup exams except in case of genuine reasons. In the event of such exceptional cases, the student must discuss the matter with the instructor and must get written permission before the date of exam.
- All issues regarding valuation of exams and quizzes/assignments must be resolved within one week after the marks are announced.

Standard of Conduct:

Each student is expected to adhere to high standards of ethical conduct, especially those related to cheating. Any academic dishonesty will result in zero marks in the corresponding exam or quiz and will be reported to the department council for record keeping and for permission to assign F grade in the course.