Experiment 1 – Clock and Periodic Signal Generation

***Abstract*— This document is a report for experiment #1 of Digital Logic Design Laboratory at ECE department, University of Tehran. The purpose of this experiment is to provide different methods for clock generation.**

***Keywords*— Clock, Ring Oscillator, LM555 Timer, Schmitt Triger Oscillator, Frequency Divider, T Flip-Flop**

I. Clock Generation using ICs and Analog Components

A. Ring Oscillator

Fig. 1 shows the circuit's implementation and Fig. 2 shows the output waveform.

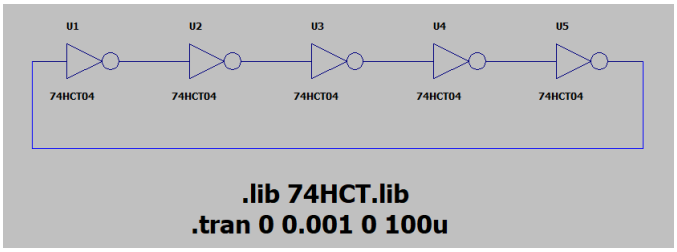

Fig. 1 Ring oscillator circuit

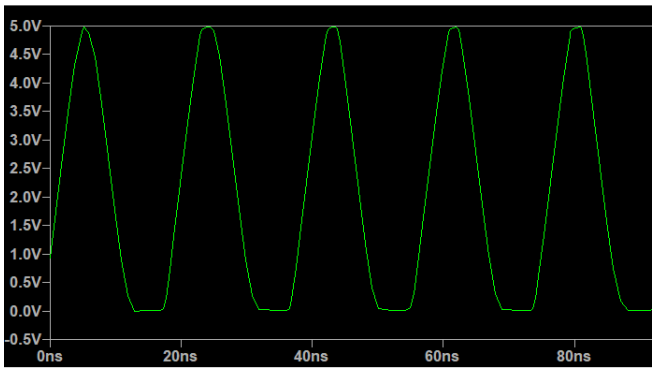

Fig. 2 Ring oscillator simulation waveform

1) Propagation Delay: To measure the propagation delay, the time from the 50% point of input to the 50% point of output should be calculated. As the voltage varies from 0 to 5v, 2.5v can be assumed for the 50% point.

$t_1 = 1.71ns$ $V = 2.504v$ slope +

$t_2 = 9.13ns$ $V = 2.504v$ slope –

$t_{PD} = 9.13 - 1.71 = 7.42ns$

2) Inverter Delay: Measuring the period time of the output requires two consecutive points with same phase. Consider the following two points:

$t_1 = 18.55ns$ $V = 0.994v$

$t_2 = 37.82ns$ $V = 0.994v$

$T = 37.82 - 18.55 = 19.27ns$

$2 \times n \times delay_{inv} = 19.27$, $n = 5 \Rightarrow delay_{inv} = 1.92ns$

NOR-flipflop based circuit implementation and its output waveform are shown in Fig. 3 and Fig. 4, respectively.

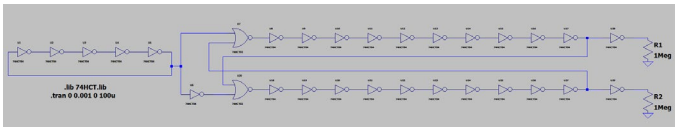

Fig. 3 NOR-flipflop based circuit implementation

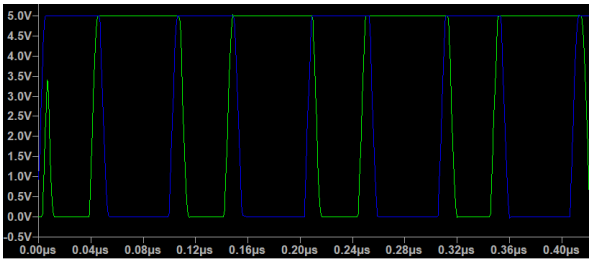

Fig. 4 NOR-flipflop based output waveform

As shown in Fig. 2, the ring oscillator acts like a clock generator. The oscillator's output is connected to a NOR-flipflop based circuit which has two outputs, Phase1 and Phase2. Fig. 4 shows the two outputs' waveforms. The waveforms confirm that Phase1 and Phase2 can be used as a two-phase clock generator from a single clock signal. Also, the two signals are non-overlapping as when one of them is activated, the other one is not activated and vice versa.

B. LM555 Timer

1) NE555 component can be used instead of the LM555 in LTspice.

$T = 0.693 \times (R_1 + 2R_2) \times C = 0.693 \times 101 \times 10^3 \times 10 \times 10^{-9} = 0.699ms \Rightarrow f = 1 \div 0.699 = 1430Hz$

$Duty\ Cycle = (R_1 + R_2) \div (R_1 + 2R_2) = 50 \div 101 = 50.4\%$

The circuit implementation and its output waveform are represented in Fig. 5 and Fig. 6, respectively.

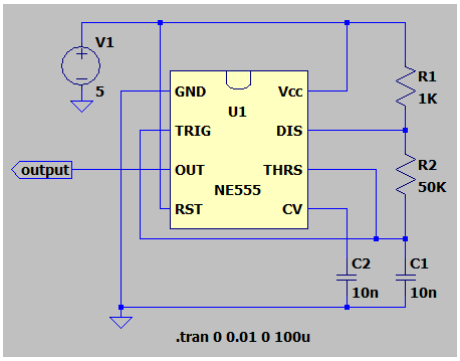

Fig. 5 LM555 Timer implementation

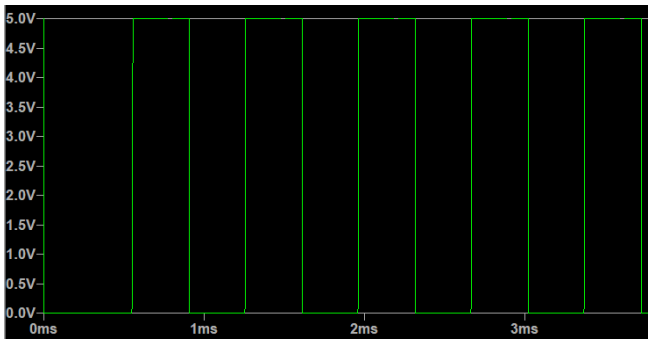

Fig. 6 LM555 waveform

Choosing two points on the same phase shows that the theoretical period is calculated correctly.

t_1 = 0.56ms V = 5v
t_2 = 1.26ms V = 5v
T = 1.26 – 0.56 = 0.7ms (based on waveform)

Also, the waveform confirms that the duty cycle is almost 50%.

2) Three other values for R_2:
R_2 = 1kΩ => T = $0.693 \times 3 \times 10^3 \times 10 \times 10^{-9}$ = 0.02ms
f = 50,000Hz
Duty Cycle = 2 ÷ 3 = 66.6%
Fig. 7 shows the output waveform of the above circuit.

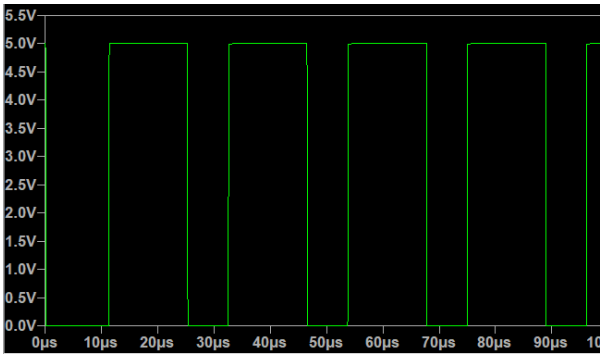

Fig. 7 Output waveform for R_2 = 1kΩ

t_1 = 0.01ms V = 5v
t_2 = 0.03ms V = 5v
T = 0.03 – 0.01 = 0.02ms (based on waveform)

Also, the waveform shows that the duty cycle is about 66%.

R_2 = 10kΩ => T = $0.693 \times 21 \times 10^3 \times 10 \times 10^{-9}$ = 0.14ms
f = 7142Hz
Duty Cycle = 11 ÷ 21 = 52.3%
Fig. 8 shows the output waveform of the above circuit.

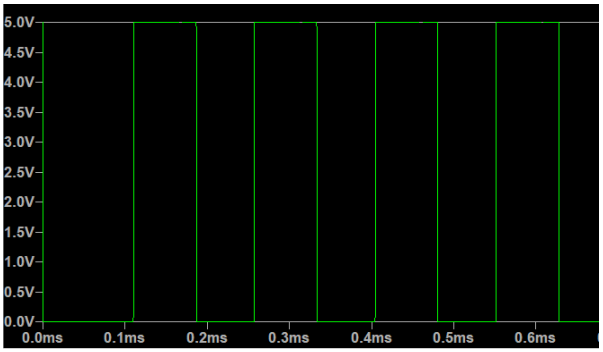

Fig. 8 Output waveform for R_2 = 10kΩ

t_1 = 0.11ms V = 5v
t_2 = 0.25ms V = 5v
T = 0.25 – 0.11 = 0.14ms (based on waveform)

Also, the waveform shows that the duty cycle is about 50%.

R_2 = 200kΩ => T = $0.693 \times 401 \times 10^3 \times 10 \times 10^{-9}$ = 2.77ms
f = 361Hz
Duty Cycle = 201 ÷ 401 = 50.1%
Fig. 9 shows the output waveform of the above circuit.

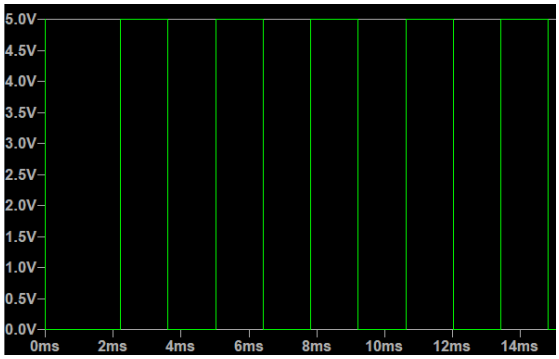

Fig. 9 Output waveform for R_2 = 200kΩ

t_1 = 2.2ms V = 5v
t_2 = 5.0ms V = 5v
T = 5.0 – 2.2 = 2.8ms (based on waveform)

Also, the waveform shows that the duty cycle is about 50%.

C. *Schmitt Triger Oscillator*

Fig. 10 shows the implemented circuit.

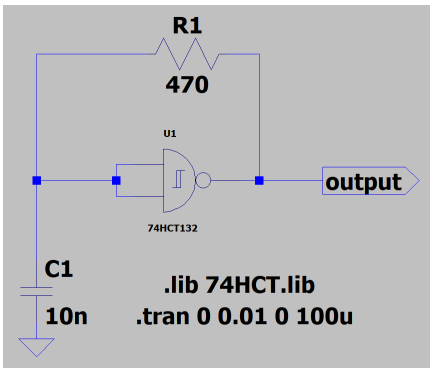

Fig. 10 Schmitt trigger oscillator

R = 470Ω, C = 10nF
Fig. 11 shows the output waveform of the above circuit.

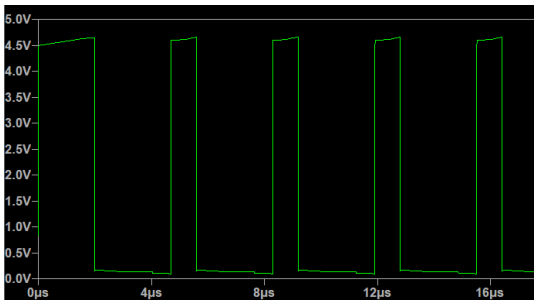

Fig. 11 Schmitt trigger oscillator with R = 470Ω

t_1 = 9.2µs V = 4.672v
t_2 = 12.8µs V = 4.672v
T = 12.8 – 9.2 = 3.6µs => f = 277,777Hz
α = 2777777 × 470 × 10 × 10^{-9} = 1.30

R = 1000Ω, C = 10nf
Fig. 12 shows the output waveform of the above circuit.

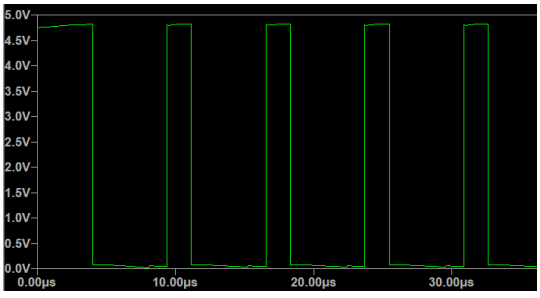

Fig. 12 Schmitt trigger oscillator with R = 1000Ω

t_1 = 11.11µs V = 4.821v
t_2 = 18.27µs V = 4.821v
T = 18.27 – 11.11 = 7.16µs => f = 139,664Hz
α = 139664 × 1000 × 10 × 10^{-9} = 1.39

R = 2000Ω, C = 10nF
Fig. 13 shows the output waveform of the above circuit.

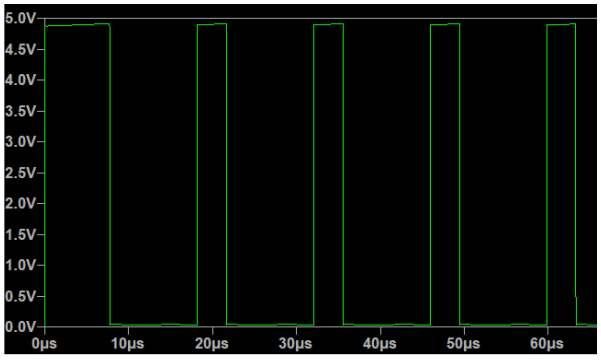

Fig. 13 Schmitt trigger oscillator with R = 2000Ω

t_1 = 21.66µs V = 4.910v
t_2 = 35.56µs V = 4.910v
T = 35.56 – 21.66 = 13.9µs => f = 71,942Hz
α = 71942 × 2000 × 10 × 10^{-9} = 1.43

II. FPGA Design

A. *Ring Oscillator*

The oscillator's Verilog description and its testbench are included in the assignment folder. Fig. 14 shows the output waveform of the ring oscillator with 5 inverters and a delay of 1.9ns for each inverter.

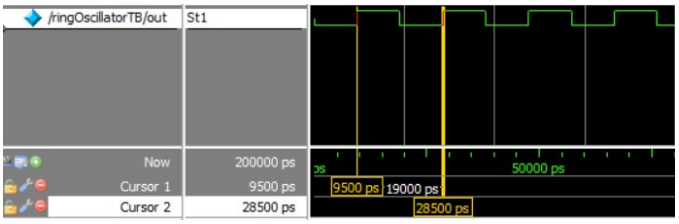

Fig. 14 Ring oscillator waveform in ModelSim

As it is obvious, the signal's period is 19ms which is almost the same as the one simulated in LTspice.
T = 19ms => f = 52.63Hz

B. *Synchronous Counter as a Frequency Divider*

As the mentioned counter does not provide clock synchronicity, activation of the carry out signal leads to load activation which results in deactivating the carry out. As a result, the carry out signal cannot be seen in the simulator. However, the moment that the carry out signal should be activated, it can be seen that the load signal (which is connected to carry out) is activated and as a result, the counter value is set to the load value (152). Fig. 15 shows the circuit design while Fig. 16 shows the waveform for the circuit. A better-quality picture is provided in the zip file. Also, a DFF can be provided in order to save the carry out.

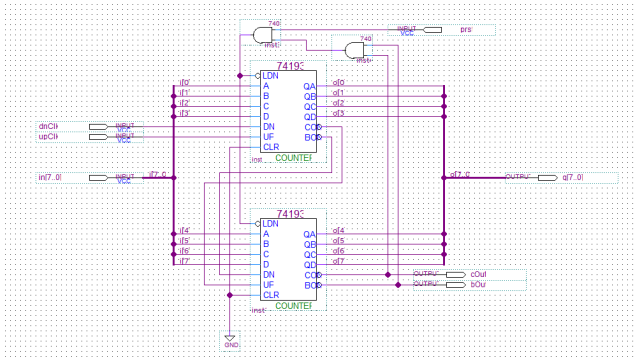

Fig. 15 Frequency divider circuit

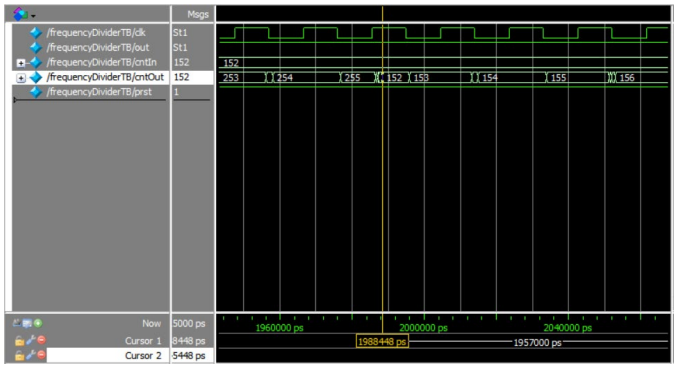

Fig. 16 Frequency divider waveform

The waveform shows that the load period is 1957ns. As mentioned in the last part, the ring oscillator period is 19ns. As a result, the frequency is divided by 1957 ÷ 19 = 103.

C. *T Flip-Flop*

The above circuit has a duty cycle of 102 ÷ 103 ≈ 99%. A TFF is used to make a duty cycle of 50%. This results in dividing the frequency by 103 × 2 = 206. As required, the TFF is made from a JK Flip Flop by connecting the J input to the K input. The connection of the two inputs is called T. The T inputs is connected to VCC and the carry out signal is connected to TFF's clock. This design is required as the ring oscillator's clock and the carry out signals are active-low while the T input and the TFF's clock are active-high. Fig. 17 shows the TFF design and Fig. 18 represents the circuit design including the TFF.

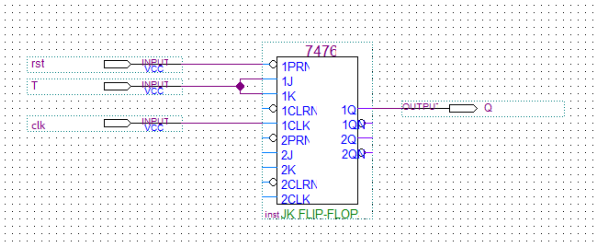

Fig. 17 TFF design

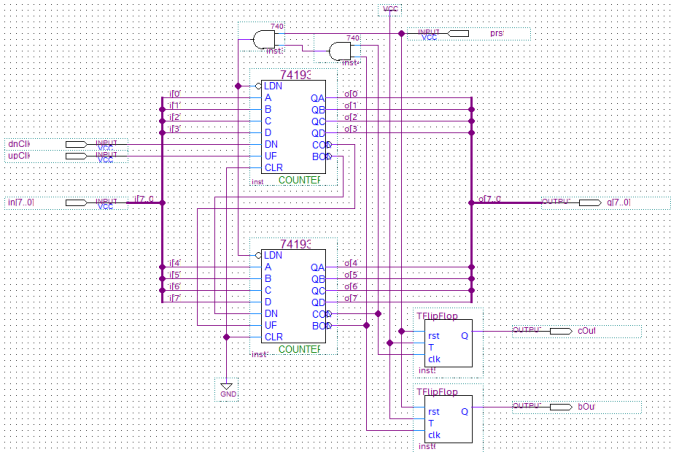

Fig. 18 Circuit design using TFF

Fig. 19 shows the output waveform for the above circuit. A better-quality picture is provided in the zip file.

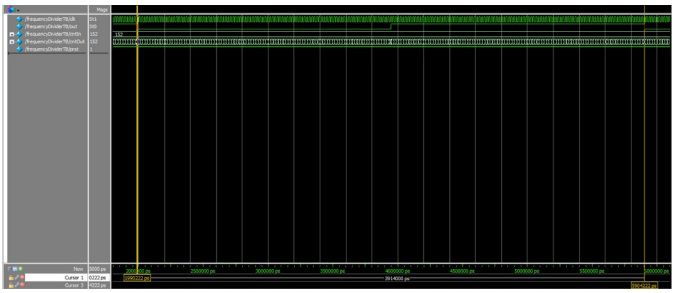

Fig. 19 Frequency divider with 50% duty cycle

According to the waveform, the TFF's output period is 3914ns. So, the frequency is divided by 3914 ÷ 19 = 206. Also, as shown in the waveform, the signal's duty cycle is 50%.

III. Baud Rate Generator for UART Serial Communication

A. *Automatic Baud Rate Calculator*

Fig. 19 shows the ABRCKT controller state diagram. A better-quality picture is provided in the zip file. Fig. 20 represents the required circuit design using ABRCKT schematic symbol. The frequency divider is used in the down counting mode in order to calculate the required frequency.

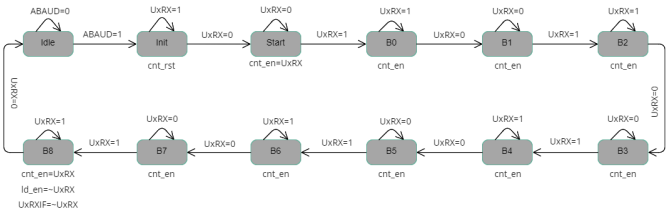

Fig. 19 BRGCKT controller state diagram

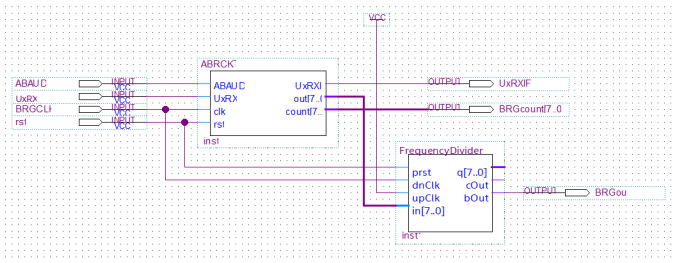

Fig. 20 BRGCKT block diagram

Fig. 21 displays the waveform for Baud rate calculation process. A better-quality picture is provided in the zip file. Also, k = 1 is used in the testbench. As it is visible in the waveform, 10 clock cycles are used before the 5th UxRX falling edge.

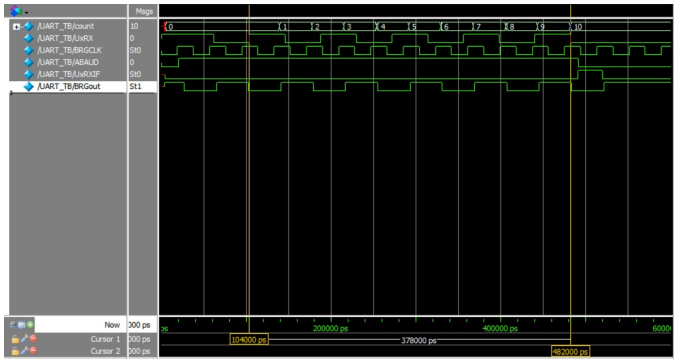

Fig. 21 BRGCKT baud rate calculation process

Theorical calculation:

N = 10, k = 1, T = 19ns

=> $f = (10^9 \div 19) \div (10 \times 2^1 \times 2) \approx 1{,}315{,}789\text{Hz}$

Fig. 22 shows the waveform for the BRGout after the baud rate calculation is completed. A better-quality picture is provided in the zip file.

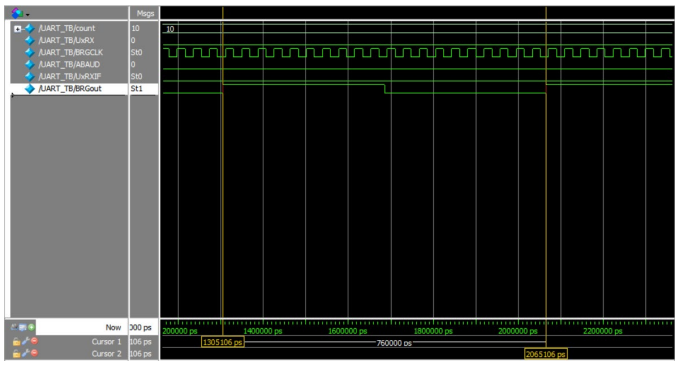

Fig. 22 BRGout signal after baud rate calculation

As it is visible in the waveform, the signal's period is 760ns. The signal's frequency is calculated as below:

$f = 10^9 \div 760 \approx 1{,}315{,}789\text{Hz}$

Which is equal to the theorical frequency calculated in the previous part.

REFERENCES

[1] 74HCT132 Schmitt Trigger datasheet

[2] 74LS193 Up-Down Counter datasheet