# Experiment 1 - Clock and Periodic Signal Generation

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***Abstract*— This document is a report for experiment #1 of Digital Logic Design Laboratory at ECE department, University of Tehran. The purpose of this experiment is to provide fundamental information about gate delays and also different methods for clock generation.**

***Keywords*— Clock, Ring Oscillator, LM555 Timer, Schmitt Trigger Oscillator, Frequency Divider, T Flip-Flop**

## I. Introduction

This experiment is to introduce the concepts of static characteristics of digital logic gates, delay times, clock frequency generation and digital systems.

## II. Clock Generation using ICs and Analog components

### A. Ring Oscillator

We were given a Ring Oscillator, and told to build a circuit with an odd number of inverters. In order to do that we connect some of the consecutive inverters that are built-in to our IC which was 74HCT04. Output waveform and circuit's implementation pictures are respectively shown below.

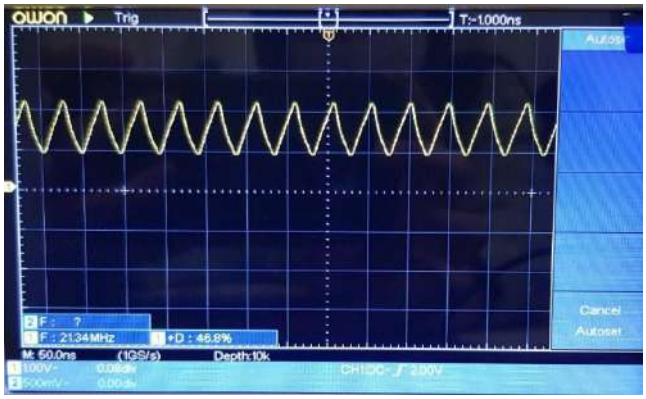


Fig. 1 output waveform

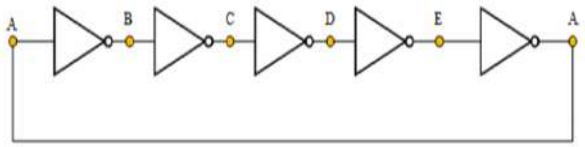


Fig. 2 circuit's implementation

1) *Propagation Delay*: It's the time between 50% point of input to the 50% point of output. Since input and output are connected we measure it as half of the period so:

$f = 1 \div T \Rightarrow T = 46.86\,ns$
therefore it would be about 23ns.

2) *Inverter Delay*: Since it's relatively very fast and we don't have high quality equipment, in order to measure that. We use several inverters and then divide it.we have period time of output and it's consist of 5 inverters each of which toggles the input twice so:
$T = 2N * Delay_{inv} \Rightarrow Delay_{inv} = T \div 10$
$\Rightarrow Delay_{inv} = 4.686ns$

### B. LM555 Timer

According to the circuit demonstrated below, the capacitor charges through R1 and R2 and discharges through R2 so the charging and discharging time that we annotate respectively with T1 and T2 is calculated with the shown formula.

$T1 = 0.693 \times (R1 + R2) \times C$
$T2 = 0.693 \times R2 \times C$

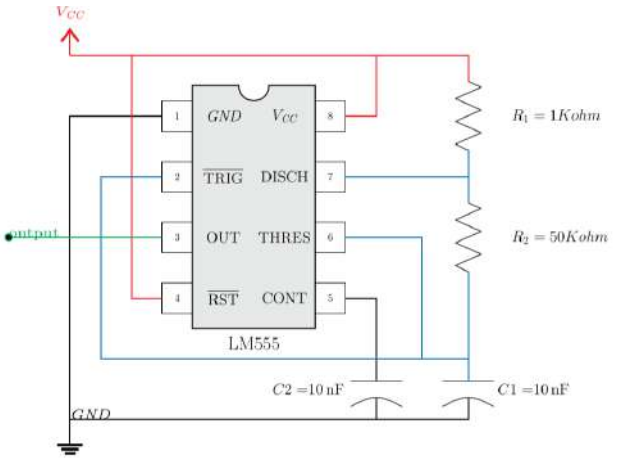


Fig. 2 LM55 circuit

1) *With 50kΩ R2*: So total time period which is equal to sum of T1 and T2 will be equal to:

$T = 0.693 \times (R1 + 2R2) \times C = 0.693 \times 101 \times 10^{3} \times 10 \times 10^{-9} = 0.699ms \Rightarrow f = 1 \div 0.699 = 1428Hz$
Duty Cycle = $(R1 + R2) \div (R1 + 2R2) = 50 \div 101 = 50.4\%$

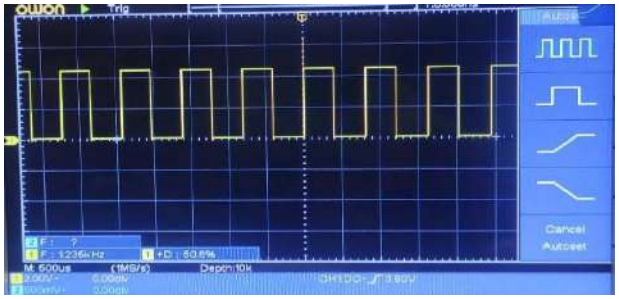

Fig. 3 the output waveform of this circuit in part 1

2) *With three different values for R2*: we repeat the previous part with 1kΩ, 10kΩ, 100*h*Ω. The respective results are:

R2 = 1kΩ ⇒ T = 0.693 × 3 × $10^3$ × 10 × $10^{-9}$ = 0.021ms ⇒ f = 47.6kHz

Duty Cycle = 2 ÷ 3 = 66.6%

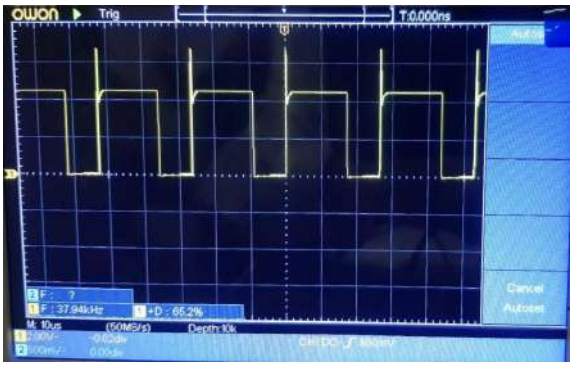

Fig. 4 the output waveform of this circuit in part 2 with 1kΩ resistance

R2 = 10kΩ ⇒ T = 0.693 × 21 × $10^3$ × 10 × $10^{-9}$ = 0.14ms ⇒ f = 6871Hz
Duty Cycle = 11 ÷ 21 = 52.3%

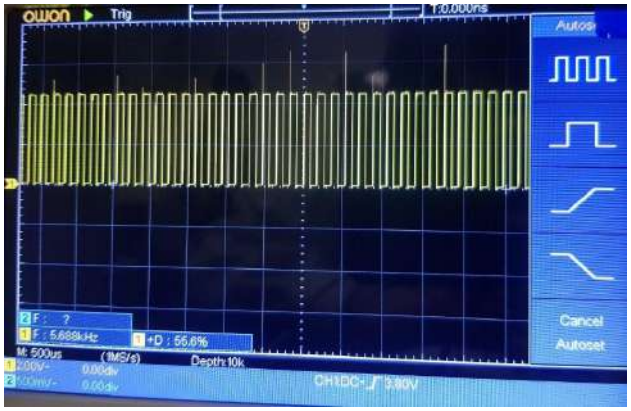

Fig. 5 the output waveform of this circuit in part 2 with 10kΩ resistance

R2 = 100kΩ ⇒ T = 0.693 × 201 × $10^3$ × 10 × $10^{-9}$ = 1.39ms ⇒ f = 718Hz
Duty Cycle = 101 ÷ 201 = 50.2%

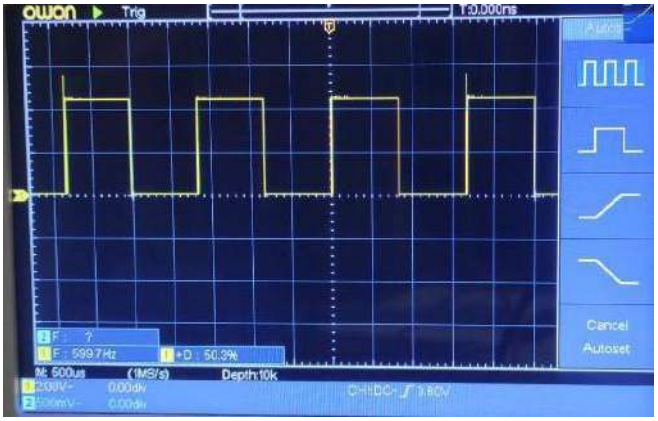

Fig. 5 the output waveform of this circuit in part 2 with 100kΩ resistance

### *C. Schmitt Trigger Oscillator*

Non-controlled oscillators are special blocks in that they don't have an input. Instead, they consist of an amplifier and a feedback loop. In the case of this circuit, the feedback loop is an RC network, which behaves as the transient model of the series RC circuit. For the Schmitt inverter oscillator circuit we have used 74HCT14.

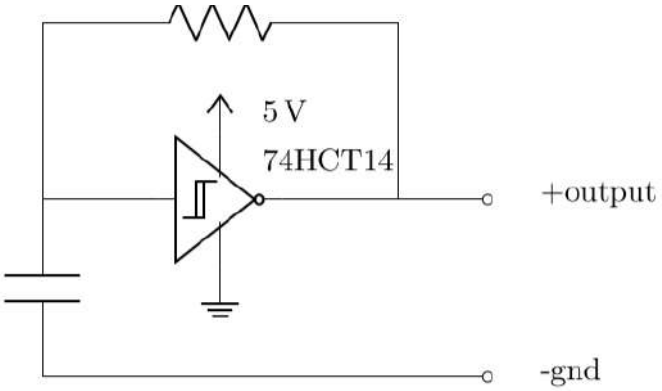


Fig. 6 Schmitt inverter oscillator circuit

These are special gates that do not respond to a single voltage threshold in their inputs. Instead, their inputs respond to one rising (higher) threshold voltage and one falling (lower) threshold voltage: Whenever the input voltage exceeds the rising threshold, the input logical level is regarded as *high*, and whenever the input voltage drops below the falling threshold, the input is considered *low*. This means that a Schmitt Trigger input has some means of recalling its current level, which is the last level it changed to.

This behavior is known as hysteresis, and it's ideal for oscillators, as you'll see below.

The following figure shows a noisy negative pulse that goes from 5V to 0V and then back up to 5V, and the output of a regular inverter and two different Schmitt Trigger inverters when fed that noisy signal:

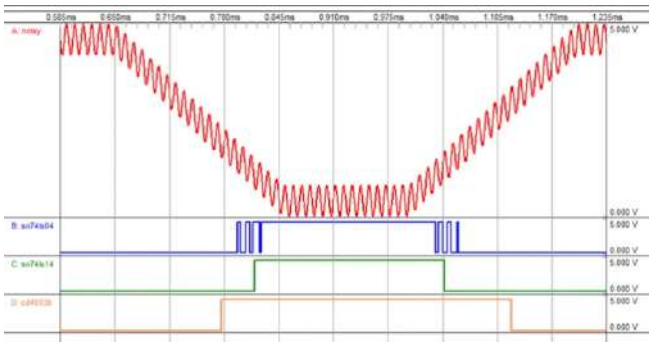

Fig. 7 example of why Schmitt Trigger Oscillator is more desired

The basic oscillator consists of a series RC circuit driven by a Schmitt Trigger inverter. The inverter's input is the capacitor's voltage. Thus, the inverter is forced to:

1. Charge the capacitor when its voltage is below $V_{T+}$ and the output is high.
2. Discharge the capacitor when its voltage is above $V_{T-}$ and the output is low.

Here's an implementation of this oscillator with a 74LS14 Schmitt Trigger inverter:

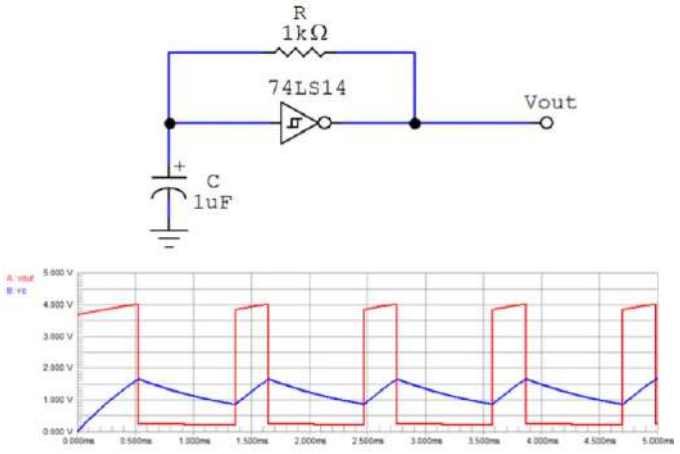


Fig. 8 An RC oscillator implemented with a 74LS14 inverter

Now that we are quite familiar with Schmitt trigger's functionality we will implement three circuits with different values for it's resistance and then determine the α (which is a constant determined only by hardware, it means that if we change the resistance the frequency will be changed in a way that we get the same result for α) by given formula:

$$f = \alpha \div (RC)$$

1) *Implement circuit with three different values:* we will repeat the experiment to determine if α is only related to hardware, not the circuit or any external part. In all repetition of experiment the capacitor is the same and has capacitance of 10nF.

For first experiment we have R = 470Ω

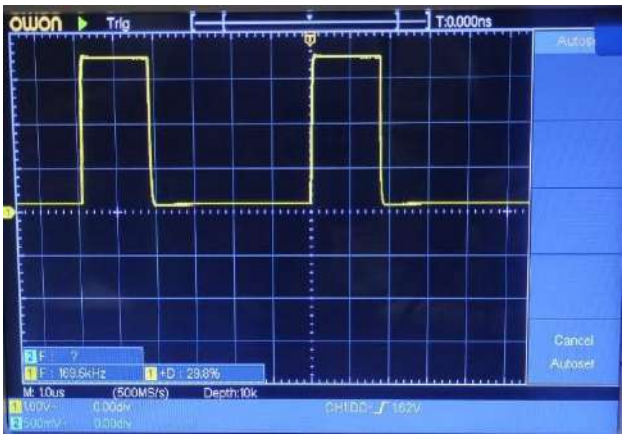


Fig. 8 output wave in 470Ω resistance

$$R = 470\Omega,\ f = 169.5kHz \Rightarrow \alpha = 796 \times 10^{-3}$$

For second experiment we have R = 1kΩ

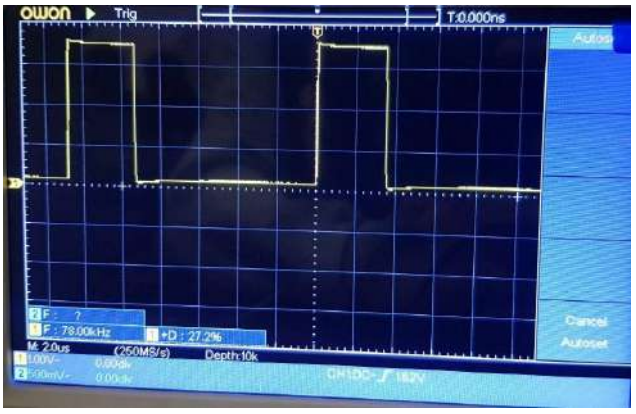


Fig. 9 output wave in 1kΩ resistance

$$R = 1k\Omega,\ f = 78kHz \Rightarrow \alpha = 78 \times 10^{-2}$$

For third experiment we have R = 2.2kΩ

Fig. 10 output wave in 2.2kΩ resistance

$$\text{R} = 2.2\text{k}\Omega,\ f\ =\ 30.35kHz \Rightarrow\ \alpha\ =\ 667\ \times\ 10^{-3}$$

As you can see in all of them almost α is constant so we realize that it is not affiliated with other components whatsoever.

*D. Synchronous Counter as a Frequency Divider*

It is really difficult to produce low-frequency waves because the usual time error for these waves will be about 1-2% and it's too much for low-frequency waves while it is acceptable for high-frequency waves. Counters can be used as a frequency divider. 74LS193 or 74HC193 is a synchronous 4-bit up/down counter. if we have a desired modulus that we we want to divide our frequency with it we will load an initial value that is found by this method:

$$initial\ value\ =\ maximum\ value\ -\ modulus$$

So in order to build a 200 synchronous up-counter we have to load 56 since it's an eight-bit counter.

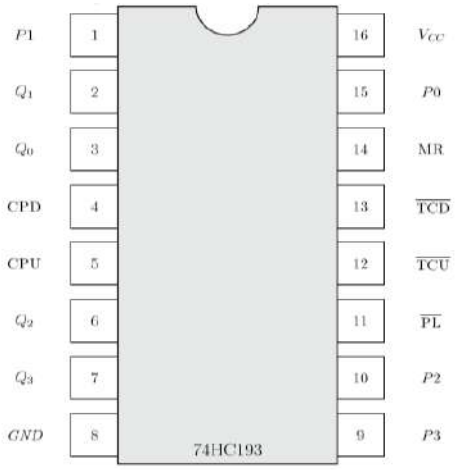


Fig. 11 pin layout of 74193

As shown in the above figure there are some parts for loading a number namely, P3-P0 and some for output namely Q3-Q0, parallel load which allows the inputs (i.e. P3-P0 parts) to be presetted. We only need to load values when we have completed a cycle, so when the carry out of MSB is enabled and also presetting is enabled we have to load the inputs. To implement this logic we need an AND gate for which we use the first three parts of 74HC08 IC in which the result of the third part is the output of the AND gate between the first and second part. Obviously the carry out of LSB is also the clock input of MSB and that of LSB is connected to the output of the ring oscillator built in part *A*. By doing so the frequency of input, namely, output of the ring oscillator (which was about 20MHz) will be divided by 200 and be around 100kHz as you can see below.

Fig. 12 output wave of the MSB's $\overline{TCU}$ part

As we expected the result has a frequency of about one-two-hundredth of that of the ring oscillator.

*E. T Flip-Flop*

Although we reached a low-frequency wave with a neglectable time error percentage, still the duty cycle is not 50% and in order to fix that we use a T flip-flop. But we only had D flip-flop in our laboratory so to convert it to T flip-flop we connected the Q1bar to the DATA1(the red line in Fig. 13) so with each clock signal it would toggle.

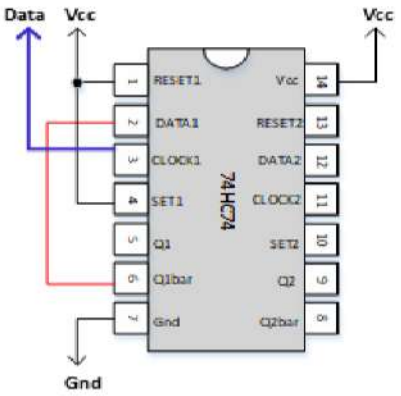


Fig. 13 pin layout of 74HC74 (i.e. D flip-flop)

Obviously since the T flip-flop needs two clock signals to get back to initial value it will divide the frequency by two and also gives us a signal with duty cycle of 50% which is depicted in Fig. 14.

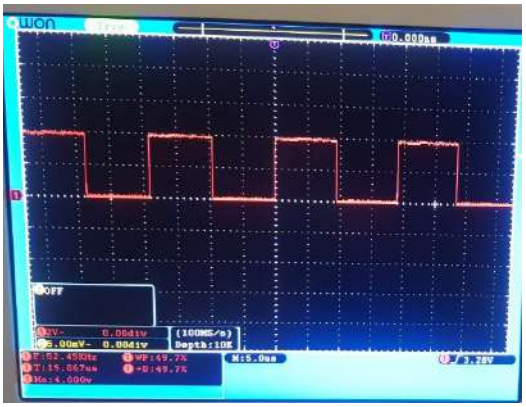

Fig. 14 output wave of T flip-flop

## III. Conclusions

The general ideas discussed in this experiment were:

A. Power supply, Function Generator, and Oscilloscope
B. 74 Series Basic Logic Gates
C. Different oscillator circuits (a LM555 timer IC, Schmitt trigger Oscillator)
D. Sequential circuits using clocks and counters


## Acknowledgment

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## References


[1] Exactly How Schmitt Trigger Oscillators Work [Online]. Available: https://www.allaboutcircuits.com/technical-articles/exactly-how-schmitt-trigger-oscillators-work/