## Problem for Assignment 1

1. Design a logic circuit in Verilog that will take one **3-bit** input **A**, check whether all of the input bits are **equal or not** and determine the **logic level (0/1)** of the unique bit. Find the possible input conditions and the expected outputs in the following table: **[15]**

| **Possible input condition** | **Output** |
|---|---|
| All bits are equal | 3 |
| Unique bit at position 2 | 2 |
| Unique bit at position 1 | 1 |
| Unique bit at position 0 | 0 |

Expected Output:
Show all possible outputs in your timing diagram with appropriate inputs and briefly explain your results.

2. Design a **5-bit end around left shift register** that operates at the **negative edge** of a clock in Verilog with external **load** functionality. For example, the output of the shift register would be ( for each **negedge** clock time t(i) to t(i+2) and so on): **[15]**

| t(i) | t(i+1) | t(i+2) |
|---|---|---|
| 10110 | 01101 | 11010 |

Expected Output:
Perform the simulation for enough time to get at least **two** repetitions of the initial input after the external **load**. Determine the total number of clock cycles required to get one repetition of the input from the timing diagram and briefly explain your reasoning for that.