Problem for Assignment 2

1. An FSM has an input w and an output z. The machine has to generate z = 1 when the following patterns in w are detected: 11 or 111; otherwise, z = 0. Reset functionality is not mandatory. **Draw the state diagram, the state-assigned table, write the Verilog code, run simulations and verify your answer.** An example timing diagram can be found here:

clock	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}	t_{11}	t_{12}
w	0	1	1	1	0	1	0	1	1	1	1	0
z	0	0	0	**1**	**1**	0	0	0	0	**1**	**1**	**1**

Expected Output:

The timing diagram should contain waveforms as described in the table. The clock period should be 10 ns. The discussion must contain a state diagram, state assigned table, and brief explanations of all high output situations e.g. z is high during t_5, $t_{11,}$ and t_{12} clock cycles. Briefly explain these situations in light of the problem statement and your derived state diagram/state assigned table.

2. You have to design a vending machine for a 4 Tk product. The vending machine can only accept inputs: no money (can be represented as input w=00), Tk 1 (can be represented as input w=01), and Tk 3 (can be represented as input w=10). Once an acceptable input is more than or equal to 4 Tk, the machine immediately generates an output Q=1, goes back to the initial state, and gives back the change (if required). Change in Tk is represented as 2 digit binary output c={c1c2}. Output c has to be calculated and initialized. Suppose, changes are 1Tk, 2Tk (assumed). Initialize 1Tk as c=00 and 2Tk as c=01. Reset functionality is not mandatory. **Draw the state diagram, the state-assigned table, write the Verilog code, run simulations and verify your answer.**

clock	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}	t_{11}	t_{12}
Tk input	0	1	3	0	3	1	0	3	3	0	3	0
w	00	01	10	00	10	01	00	10	10	00	10	00
Q	0	0	1	0	0	1	0	0	1	0	0	0
c	?	?	?	?	?	?	?	?	?	?	?	?