Problems for Assignment 4

1. Draw the layout (without using the MOS generator from the design palette) of the logic circuit in correspondence with it's stick diagram defined by the following expression:

$$Y = \overline{(A+B+C)D}$$

   Clear all the design errors (DRC) and determine the area of your designed layout.

   Expected Output:

   Draw the stick diagram of the circuit. Determine the height, width and area of the stick diagram and compare them with the corresponding parameters derived from your design in Microwind. Attach the timing diagram with the time scale set to 5 ns.

2. Draw the layout of a 3-input NAND gate using the MOS generator from the design palette in Microwind. Clear all the design errors (DRC) and determine the area of your designed layout.

   Expected Output:

   Draw the stick diagram of the circuit. Determine the height, width and area of the stick diagram and compare them with the corresponding parameters derived from your design in Microwind. Attach the timing diagram with the time scale set to 10 ns.

3. Compile the layout using Microwind from the Verilog code of the following schematic diagram: