Problem for Assignment 0

1. Design the digital logic circuit in Verilog from the following logic expression:

$$Y = \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}\bar{C} + ABC$$

Submit the answers to the following questions (provide necessary simulation outputs where applicable):

(a) Draw the truth table for the logic circuit expressed by the equation above and explain the logic operation performed by the circuit. **[5]**

(b) Assign suitable clocks to the input pins in Verilog to generate all possible input combinations as in the truth table in Q.1(a), perform simulation for 50 ns and show the timing diagram. From the timing diagram, pick the outputs from two randomly selected time instances and crosscheck the input/output values with the truth table in Q.1(a). **[5]**

(c) Assign random values to the input pins in Verilog **at half grid intervals**, perform simulation for 50 ns and show the timing diagram. From the timing diagram, pick the outputs from two randomly selected time instances and crosscheck with the truth table in Q.1(a). **[5]**

(d) Modify the equation so that the logic circuit is composed of only **NAND** gates. Simulate the logic circuit in Verilog for 50 ns and show the timing diagram by assigning suitable clocks to the input pins to generate all possible input combinations. Provide the circuit diagram synthesized by the Verilog compiler. **[5]**