# Problems for Assignment 3

*(All problems must be done in dsch2 and you can't use a pre designed gate. You need to build the gate from scratch)*

1. Derive the Boolean logic expression from the following K-Map and implement the logic function using CMOS technology. You may use blocks/sub-circuits made using CMOS technology but cannot use readily available logic gates.

| CD \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | 0 | 1 | 1 |
| 01 | 1 | d | d | 0 |
| 11 | d | d | 1 | 0 |
| 10 | 1 | 1 | 0 | 1 |

**Expected Output:**

Show the necessary steps to derive the logic expression from the K-Map and draw the CMOS circuit in *dsch2.* Assign clocks of suitable frequencies to each of the inputs so that all possible input combinations are generated in the timing diagram. From your timing diagram explain one case where *Output = 1* and another case where *Output = 0*. Verify the values with your theoretical values calculated from the logic expressions.

2. Implement the following logic expression using an ***16 to 1*** multiplexer.

$$f(A,B,C,D,E) = \sum(0,4,5,8,9,12,15,21,22,29,30);\ \text{don't care } 7$$

The ***16 to 1*** multiplexer is to be designed using sub-circuit blocks of ***4 to 1*** multiplexers only.