Ahnaf Shahriar

Email | LinkedIn | Github

Education

University of Waterloo Waterloo, ON

Bachelor of Applied Science in Computer Engineering *Sept. 2021 – May 2026*

- Recipient of Richard & Elizabeth Madter Entrance Scholarship and President's Scholarship of Distinction
- **Relevant Courses**: Digital Communication Systems, Computer Networks, Computer Architecture, Real Time Operating Systems, Digital Hardware systems(Verilog)

Experience

IC Design and Verification Intern Jan. 2024 – May 2024

NXP Semiconductors Canada *Kanata, ON*

- **IP Design**: Designed multiple IP blocks for NXP's flagship dataplane processing SOCs upto *100Gbps*.
- **Timing Analysis**: Spearheaded critical path improvements for IP to meet *600Mhz* from 400Mhz.
- **Funcitonal Testing**: Designed brand new End-to-End functional tests for *ECC Detection* on Chip.

IC Design Verification Intern May 2023 – Aug. 2023

NXP Semiconductors Canada *Kanata, ON*

- **UVM SystemVerilog**: Designed the *IP specific Virtual Sequence* and corresponding *Covergroups*.
- **Test Planning**: Created Simulation scenarios for testing IP block features in Dataplane processing.
- **Workflows**: Spearheaded migration to *Git* and designed Bash scripts for regression testing.

Software Engineering Intern Sept. 2022 – Dec. 2022

Synapse Product Development *Seattle, WA*

- **Prototyping**: Leveraged Zephyr RTOS to create a proof of concept on *NRF52 BLE* device.
- **Python APIs**: Developed company specific lab automation software for equipment from *Agilent, Keysight, NI, Tektronik.*
- **Automation**: Streamlined testing and in house procedures using *Python* and *Bash.*
- **Driver Development**: Designed and implemented *drivers* for the controls of PCB testing Device*(I2C, UART)*

Firmware developer Jan. 2022 – April 2022

Ford Motor Company of Canada *Remote*

- **Unity/Cmock Test framework**: Lead developer for optimization for unit testing, achieving up to *30% faster* runtime while using *50%* less manually written test cases.
- **Automation**: Improved *Jenkins CI/CD* pipelines to support unit testing automatino using *Python* for Linux server.
- **Embedded Trace Debugging**: Tested logging and interrupt algorithms and debugged on hardware test benches through CAN and Serial.
- **Automotive Design**: Maintained *AUTOSAR* standard design with *ISO26262 safety design* using *Davinci Configurator*.

Projects

RISC-V processor: A 5 stage pipelined FPGA processor in Verilog. Designed and tested with Vivado for Zynq-7000.

Stereo System: An FPGA designed in Quartus and programmed in C. Implements stereo playback speed options.

Real Time Executable: A STM32 RTOS implementation capable of Pre-emptive task switching and its very own Malloc.

VHDL Compiler: A Java Compiler for creating combinational VHDL circuits. Using a boolean intermediate representation

Technical Skills

Languages: Python, Java, C/C++, Tcl, Bash scripting, ASM, VHDL, SystemVerilog/Verilog,
Tools: Quartus, Git, Linux, Qemu, GNU Tools, Docker, WireShark, UVM, Matlab
Hardware: Oscilloscopes, Logic Analyzer, Multimeters, Spectrum Analyzer
Protocols:TCP/IP, JTAG, Serial, Ethernet, CAN/CAN-FD, LIN