Ahnaf Shahriar

Email | LinkedIn | Github

Education

University of Waterloo Waterloo, ON

Bachelor of Applied Science in Computer Engineering *Sept. 2021 – Apr. 2026*

- Recipient of Richard & Elizabeth Madter Entrance Scholarship and President's Scholarship of Distinction
- **Relevant Courses**: Computer Architecture(Verilog), Computer Networks, Systems Programming and Concurrency, Embedded Microprocessing Systems, Analog Control Systems, Compilers(Java), Numerical Methods

Experience

IC Design and Verification Intern May 2023 – Aug. 2023, Jan. 2024 – May 2024

NXP Semiconductors Canada *Kanata, ON*

- **IP Design**: Designed multiple IP blocks NXP's flagship dataplane processing chips.
- **Timing Analysis**: Spearheaded critical path improvements in IP block to increase speed by 50%.
- **Functional Testing**: Designed brand new End-to-End functional tests in simulating traffic for IP.
- **Unit Test Planning**: Created Simulation scenarios for testing High speed Dataplane Processing features.

Embedded Software Engineering Intern Sept. 2022 – Dec. 2022

Synapse Product Development *Seattle, WA*

- **Prototyping**: Leveraged Zephyr RTOS to create a proof of concept on *NRF52 BLE* device.
- **Python APIs**: Developed company specific lab automation software for equipment from *Agilent, Keysight, NI, Tektronik.*
- **Automation**: Streamlined testing and in house procedures using *Python* and *Bash.*
- **Driver Development**: Designed and implemented *drivers* of automated PCB testing Device*(I2C, UART)*

Firmware developer Jan. 2022 – April 2022

Ford Motor Company of Canada *Remote*

- **Unity/Cmock Test framework**: Lead developer for optimization for unit testing, achieving up to *30% faster* runtime while using *50%* less manually written test cases.
- **Automation**: Improved *Jenkins CI/CD* pipelines to support unit testing automation using *Python* for Linux server.
- **Embedded Trace Debugging**: Tested logging and interrupt algorithms and debugged on hardware test benches through CAN and Serial.
- **Automotive Design**: Maintained *AUTOSAR* standard design with *ISO26262 safety design* using *Davinci Configurator.*

Firmware Team Member Sept. 2021 – Sept. 2023

UW Midnight Sun Solar Rayce Car Team *Waterloo, ON*

- **Macro Functionality**: Designed abstractions for RTOS functionalities through macros based on New central CAN architecture model.
- **Testing**: Programmed *I2C and SPI* Data logging through centralized CAN messages.
- **CAN API autogeneration**: Implemented C file autogeneration using input yaml files through Python

Projects

LC-3 Emulator: A C emulator for an educational ISA. Improves by 25% on research paper using *Python* data logging.

Real Time Executable: A RTOS implementation in STM32 capable of Pre-emptive task switching and its own Malloc

Stereo System: An embedded C implementation of a stereo playback system. Created with Quartus on Artix FPGA.

VHDL Compiler: A Java Compiler for creating combinational VHDL circuits. Using a boolean intermediate representation

Technical Skills

Languages: C/C++, Java, Python, Tcl, Bash scripting, ASM, VHDL, SystemVerilog/Verilog
Tools: Keil, Quartus, Git, Linux, Qemu, LLDB/GDB , Docker, WireShark, UVM, Matlab
Hardware: Oscilloscopes, Logic Analyzer, Multimeters, Spectrum Analyzer
Protocols: TCP/IP, JTAG, Serial, Ethernet, CAN/CAN-FD, LIN