Md. Shahriar Khan Limon

ID: 19101444 Sec: 08 _ CSE350 Lab 3

Experiment 3

Study of a TTL NAND gate with totem pole output

Objective:

1. Building standard TTL-NAND gate.
2. Measure the voltages and verify the circuit.

Circuit:

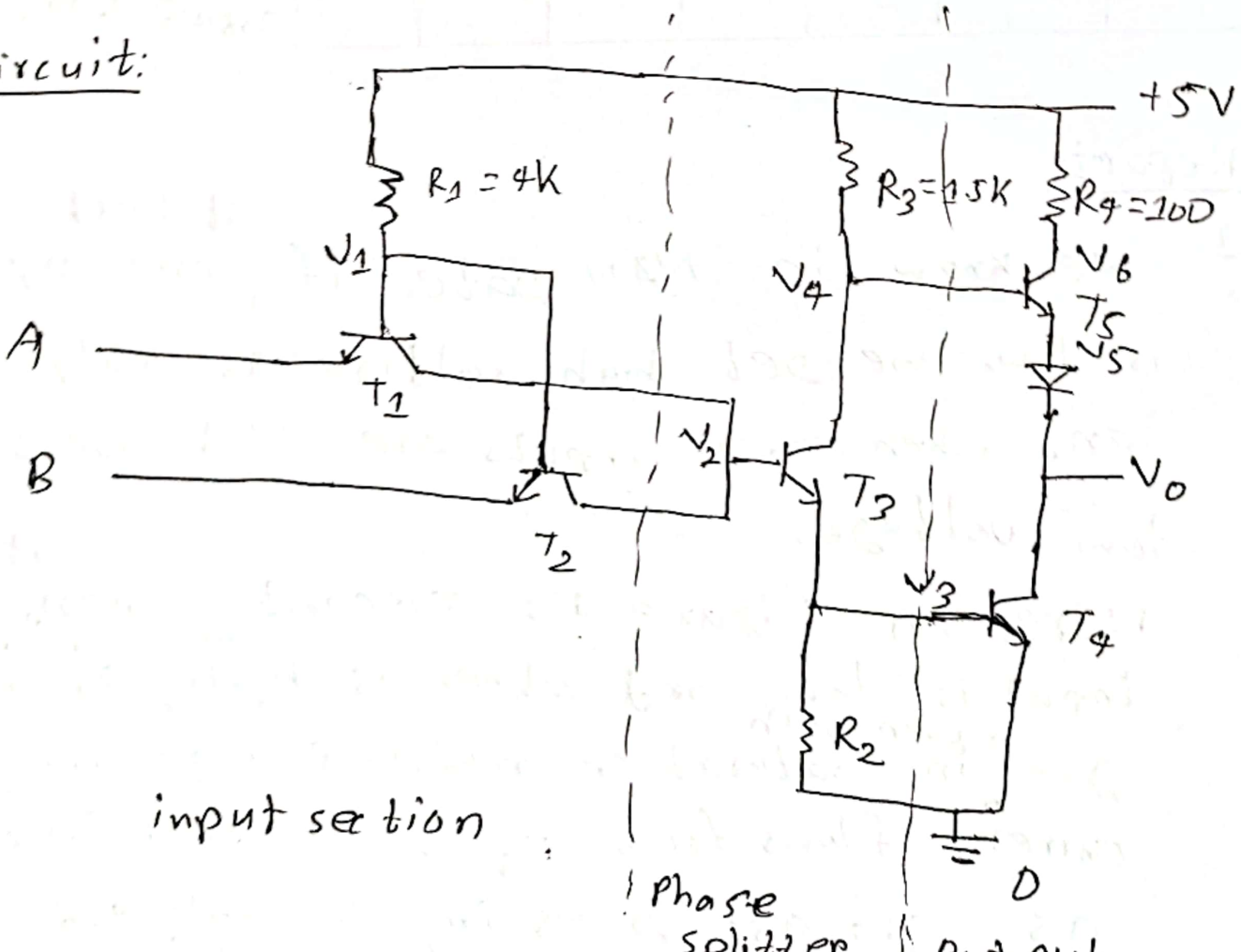
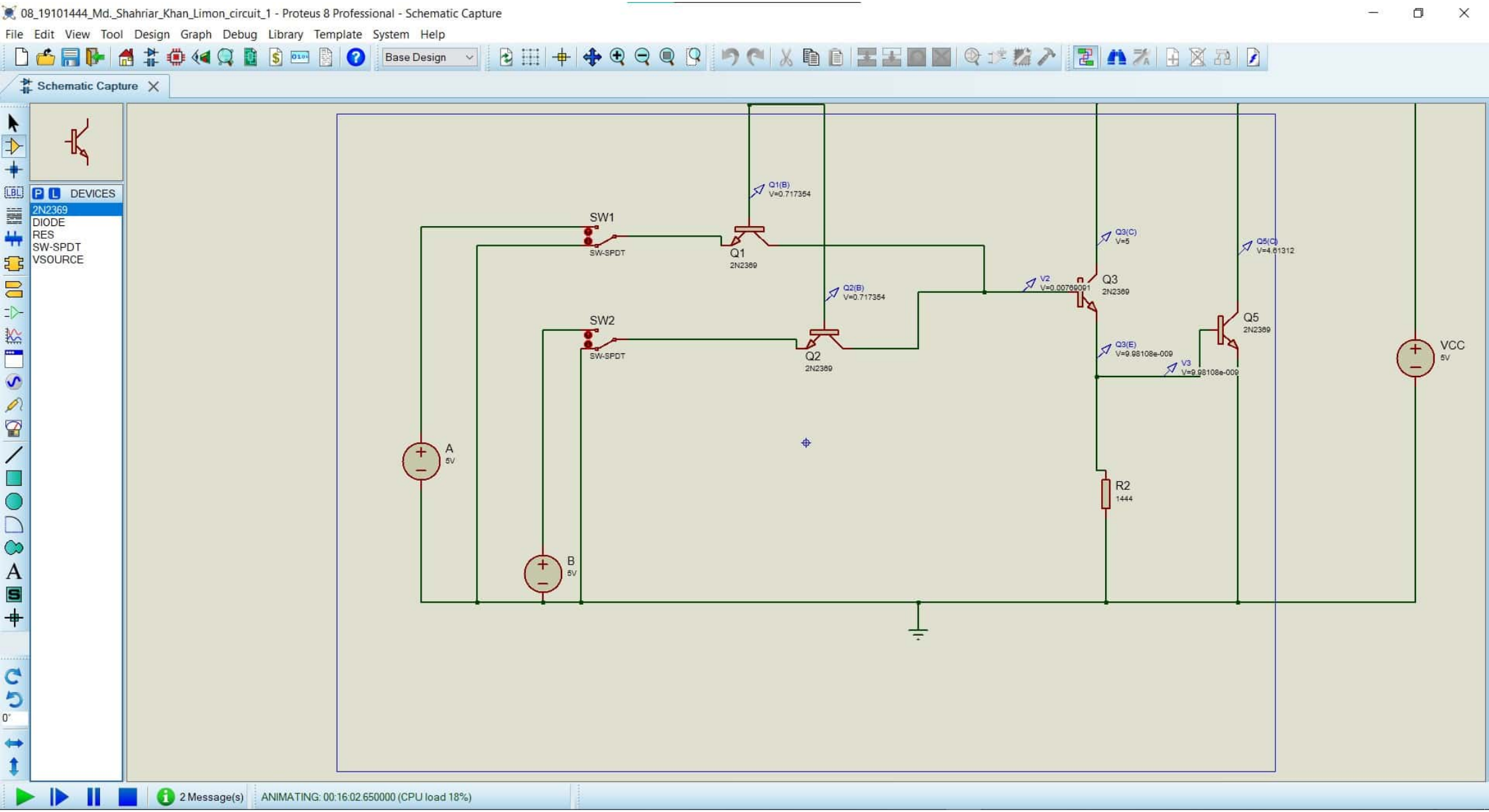


Figure: TTL-NAND gate with Totem Pole output


08_19101444_Md._Shahriar_Khan_Limon_circuit_1 - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
DEVICES
2N2369
DIODE
RES
SW-SPDT
VSOURCE
SW1
SW-SPDT
SW2
SW-SPDT
Q1
2N2369
Q2
2N2369
Q3
2N2369
Q5
2N2369
Q1(B)
V=0.717354
Q2(B)
V=0.717354
Q3(C)
V=5
Q5(C)
V=4.61312
V2
V=0.00769091
Q3(E)
V=9.98108e-009
V3
V=9.98108e-009
A
5V
B
5V
VCC
5V
R2
1444
2 Message(s)
ANIMATING: 00:16:02.650000 (CPU load 18%)

Procedure:

my ID is 19101444, and my last 4 digits 1444. so, $R_2 = 1444\ \Omega$

Input A	Input B	Input (V_A)	Input (V_B)	V_0 (V)	V_1 (V)	V_2 (V)	V_3 (V)	V_4 (V)	V_5 (V)	V_6 (V)
0	0	0V	0V	4.61312	0.21735	0.00269	0	5	4.80314	5
0	1	0V	5V	4.61312	0.255312	0.04941	1.006×10^{-8}	5	4.80314	5
1	0	5V	0V	4.61312	0.255312	0.04941	1.006×10^{-8}	5	4.80314	5
1	1	5V	5V	0.009218	2.67357	1.96409	1.05959	1.15125	4.99603 0.581424	4.99603

Reports:

1. We know in NAND gate, if at least one input is low, we get high voltage as output. and when all inputs are high, we get low voltage.

Here, in Figure-1's circuit, when at least an input is low or low, T_1 or T_2 transistor goes in or even both saturation mode, a very small current flows from T_3, so it goes in cut-off as T_4 also goes in cutoff. And T_5 is at base and current flows. so, the voltage

5 V goes, and it will lose some of voltage but still we get a high voltge.

But when both inputs are high, T_1 ~~or~~ T_2 which works as a one transmitter works as a reverse active mode. Then T_3 goes in saturation mode; and a high amount voltage goes from T_3 to T_4, which also goes in saturation mode, so, T_5 goes in cut-off mode and we get the low amount voltage from the T_4.

So, this is how figure-1 works as NAND gate.

2. Totem pole stage is also defined as push-pull output stage of an electrical ~~cuit~~ circuit ~~who~~ which is made up of two complimentary transistors. And it is determined what will be output like high or low in totem pole.

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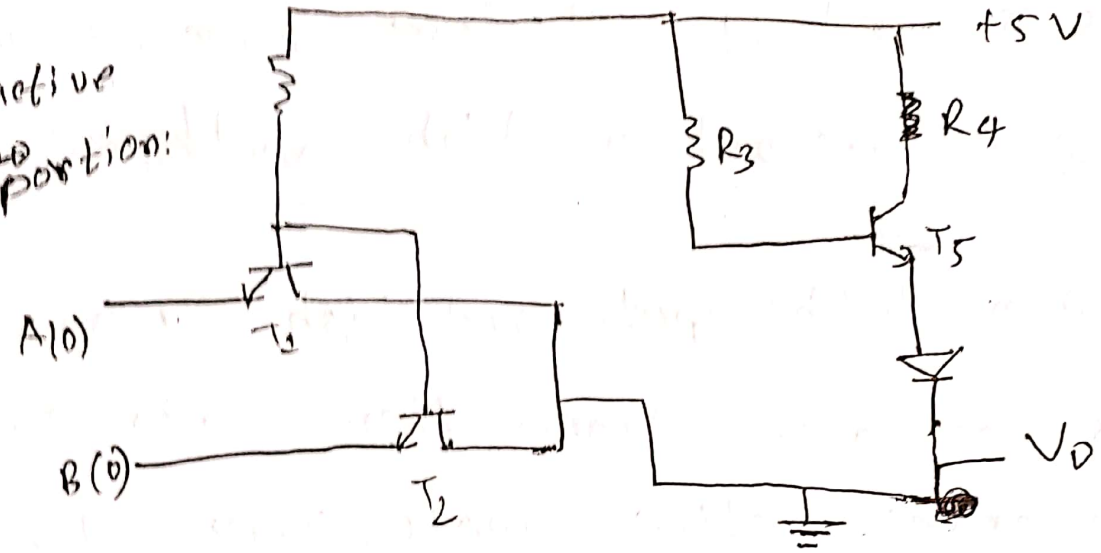
3. active pull-up portion:



4. In TTL circuit, transistor T_3 is located at phase splitter section. So, it works to phase ~~split~~ split.

T_3 works when the value of T_1 or T_2 transistor's high, it also high (it's base voltage), then it makes the emitter voltage low, and as a result T_4 can't turn on, and T_5 on. On the contrary, when T_3's base is ~~high~~, low, it makes the emitter high, so, T_5 turned off and T_4 is turned on.

Moreover, it conducts in a way if one side of the ~~output~~ transistor on, it makes the other one to cut-off mode.

5. if Diode D_1 is not used in the circuit, we won't get the outputs as NAND gate, especially when both inputs are high.

when A, B both are high, T_3 works as a saturation mode, then current flows from T_4 transistor and T_5 is cut-off as to turn on T_5, we at least need 1.4 V (0.2 V from D_1 and 0.2 for the transistor as on) At that time, ~~T_5~~ T_3's base voltage is 0.9V for that, the required 1.4V can't be passed through T_5. But if there is not D_1, then only 0.2 V is needed to active the T_5. so, the T_5 will not be

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(6) in cut-off any more and we will get high voltage. ~~thus~~

Thus, it won't work as a NAND gate any more.

6. From the table which we get from simulation,

for T_5 transistor, (when at least one input is low)

$V_C = V_6 = 5\ V$

$V_B = V_4 = 4.80314\ V$

$V_E = V_5 = 4.80314$

so, $V_{CE} = V_C - V_E = 5 - 4.80314$

$= 0.19686\ V$

$\approx 0.2\ V$

only in forward active mode,

$V_{CE} \geq 0.2\ V$.

So, the mode of T_5 is forward active.

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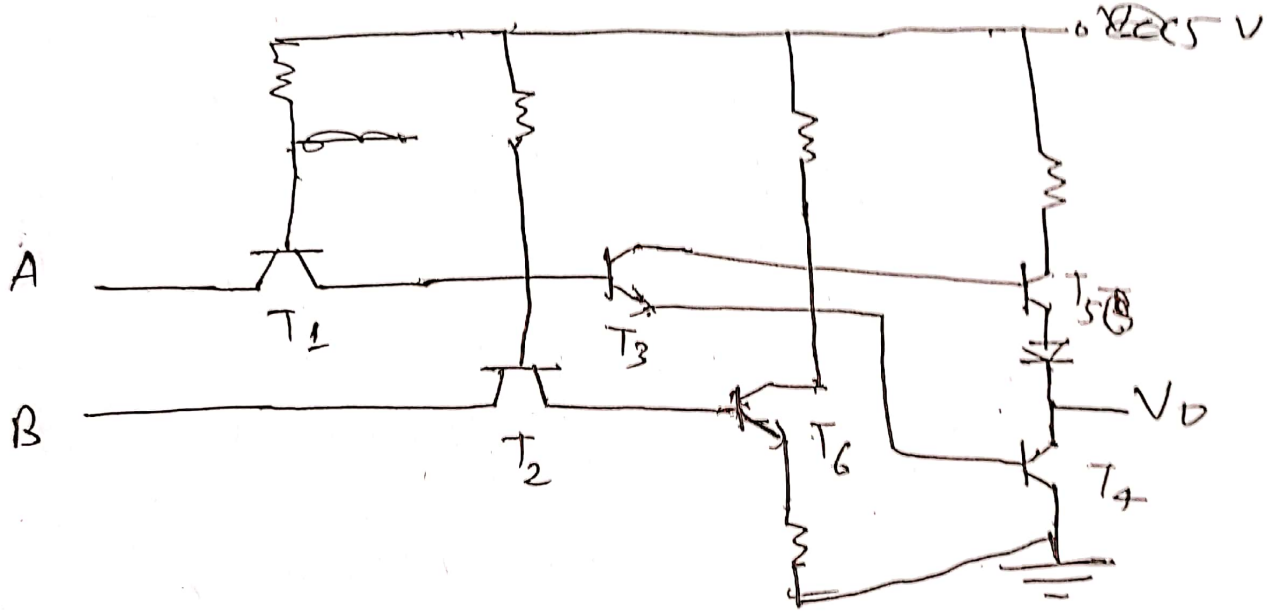
7. the circuit is:



TTL NOR gate