Md. Shahriar Khan Limon

ID: 1910144 Sec.: 08

CSE350 Lab Assignment 2

Experiment No: 2

Objective:

1. Construct a DTL logic gate.
2. Understand the circuit operation

Circuit Diagram:

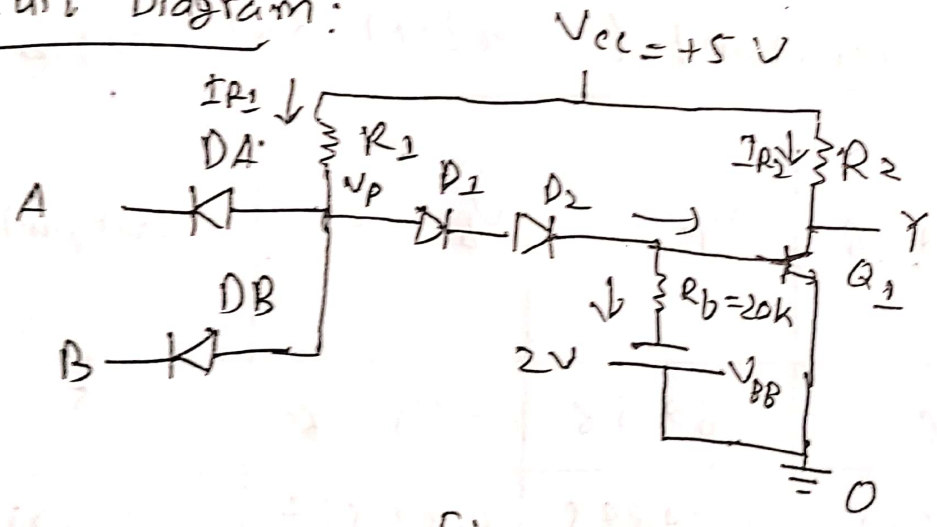

Fig: 1

Laboratory Tasks:

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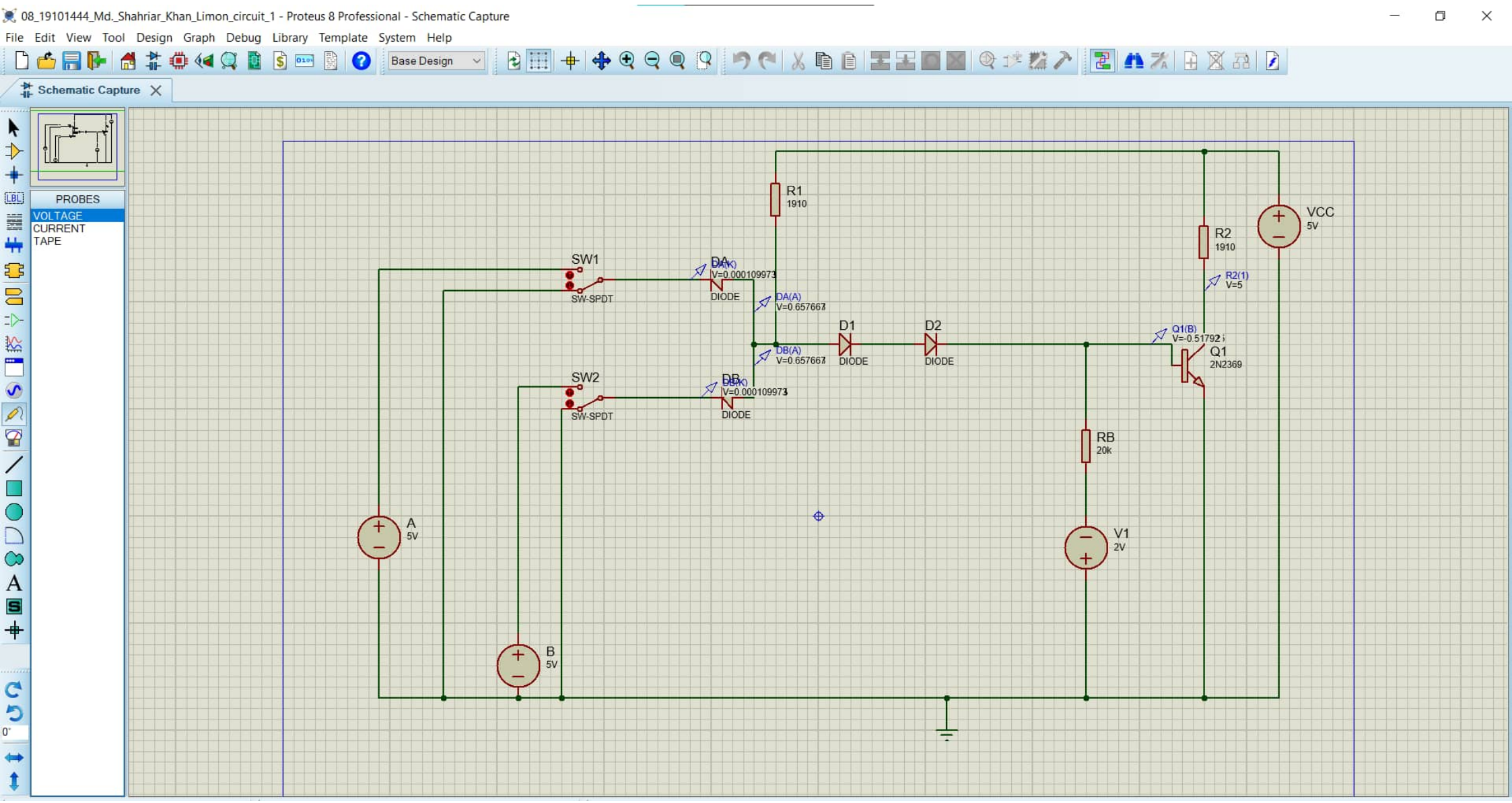
so, $R_1 = R_2 = 1910\ \Omega$


08_19101444_Md._Shahriar_Khan_Limon_circuit_1 - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
PROBES
VOLTAGE
CURRENT
TAPE
R1
1910
R2
1910
VCC
5V
SW1
SW-SPDT
DA
DIODE
DA(A)
V=0.657667
D1
DIODE
D2
DIODE
DB(A)
V=0.657667
Q1(B)
Q1
2N2369
R2(1)
V=5
SW2
SW-SPDT
DB
DIODE
RB
20k
A
5V
B
5V
V1
2V

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(2)

for NAND gate table

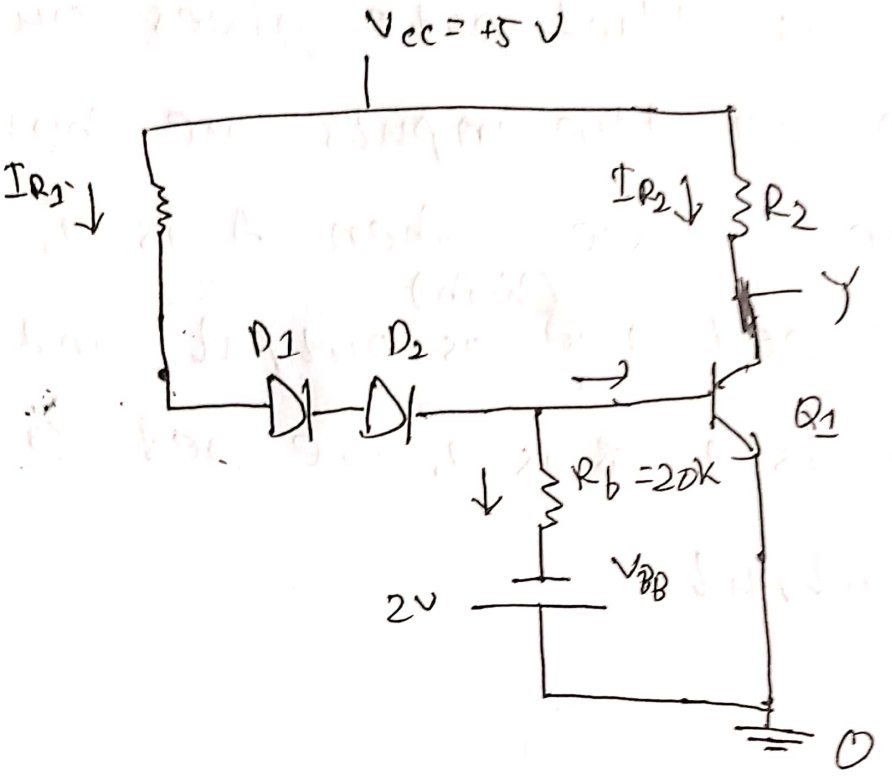
Input A	Input B	V_{DA}	V_{DB}	V_p	I_{D_1}	I_{D_2}	V_b	Output Y
0	0	0.6525	0.6525	0.6525	0.002223	0	-0.55332	5
0	1 (5V)	0.62558	-4.3244	0.62558	0.002264	0	-0.500605	5
1 (5V)	0	-4.3244	0.62558	0.62558	0.002264	0	-0.500605	5
1 (5V)	1 (5V)	-2.85155	-2.85155	2.14895	0.001492	0.002562	0.8137529	0.0958625

for +5V constant (Inverter) gate Table

Input A	Input B	V_p	V_b	Output Y
1 (5V)	0	0.62558	-0.500605	5
1 (5V)	1 (5V)	2.14895	0.8137529	0.0958625

Report

1.



2. In table 2, the input A is high always, (5V) and we are changing just Input B. It is a inverter ~~circuit~~. gate. As when A is 1 and B is 0, we get the output 1, ~~abi~~ also when A, B is on, we get output 0. But we can also say, it is operating as NAND gate. We know from the theory NAND ~~get~~

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gate gives output 1, when any input is 0.

~~and~~ And Nand gate gives output 0, when all the inputs are high (on).

Here, we see when A is 1, B is 0, we get 1 (high) as output and when A is 1, B is 1, we get 0 (low) as output.

3. At first when both inputs are ON (high), here, D_A, D_B will be turned off. So, Vp here will be greater than 2.1V, and to turn the transistor ON, the Vp should be greater than 2.1V. here, $D_1 = 0.2$, $D_2 = 0.2$ and $V_b = 0.2$ V. So, total $0.2 + 0.2 + 0.2 = 2.1$ V will go from transistor and both junctions will be forward bias and so it will be in saturation mode and we will get output 0V (low).

When either A or B of one is high and the other is low.

here, if D_A on, then D_B off,

so for one of the A or B is ON, V_p will be like 0.2 V, that is less than 2.1 V. So, the transistor won't be ON. It will be in cut off mode, no current will pass through it, and we will get the 5 V from V_{cc} which is high volt.

When both inputs are low:

here, D_A, D_B will be on, so V_p will be 0.2 V, so no current flow again from transistor as it is less than 2.1 V, so again we will get 5 V ~~from~~ of V_{cc}, so the output will be high.

4. Q1 is transistor.

To turn the transistor we need 2.1V from the base voltage.

But when A is high and B is low or B is high and A is low, the diode D_A or D_B will on based on which input is on.

As a result, D_A or D_B will give 0.7 V which is not enough ($< 2.1V$) to turn the transistor on so, the Q_1 transister will be like cut off mode and there won't be any current flow, so from there we will count 0 current.

5.

if A is 5V. an B is 1.1 V or less than 1.1 V we get outpnt still high. Similarly for B is 5V and A is less than 1.1 V.