Md. Shahriar Khan Limon
ID: 19101444 Sec: 08 CSE 350

Lab 4

Name of the experiment: Analysis of the binary weighted and R/2R ladder D/A converters.

Report:

1. Yes, we can get output higher than 15 V in D2A converters.
We can get output ~~#~~ we want by increasing the value of the input bits, when we use the binary weighted one, also by increasing the voltage sources and the R_F resistance, again we can do this by decreasing the value of the resistance connected to each input.
And when we work with R and 2R, we simply increase the value of the input bits, the R_L resistance, the voltage sources. Also, by ~~decr~~ decreasing the value of R_L and

R. Thus we will get output which will be higher than 15 V.

2. with R and 2R resistors,

the full step output = -9.4 V

resolution = 0.62 V

using Binary weighted Resistors,

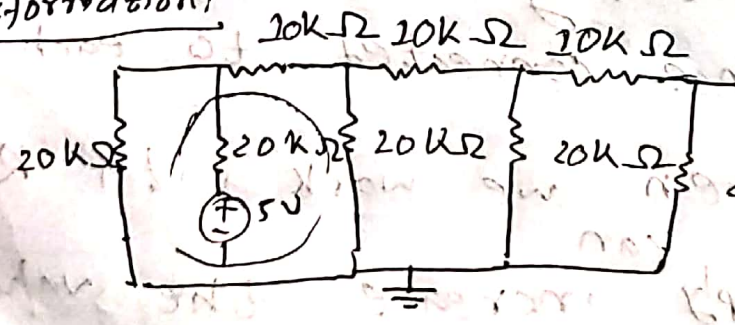
full step output = -2.5 V

resolution = 0.5 V

3. selecting the data entry 0001 of binary value.

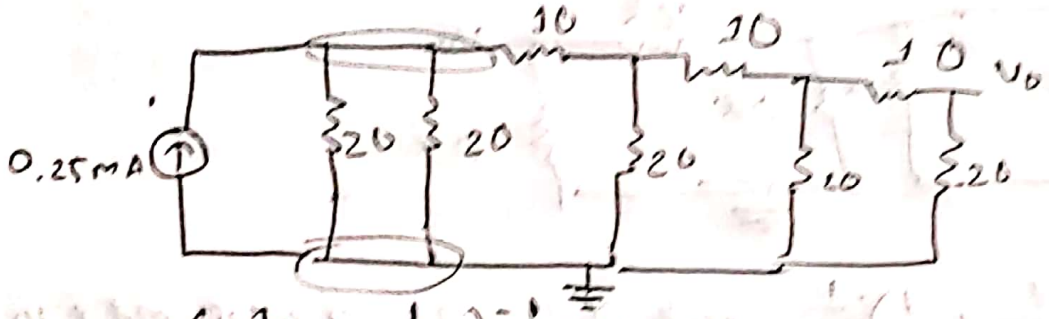
Let, here A is 5V and B, C, D is 0V.

Source transformation,

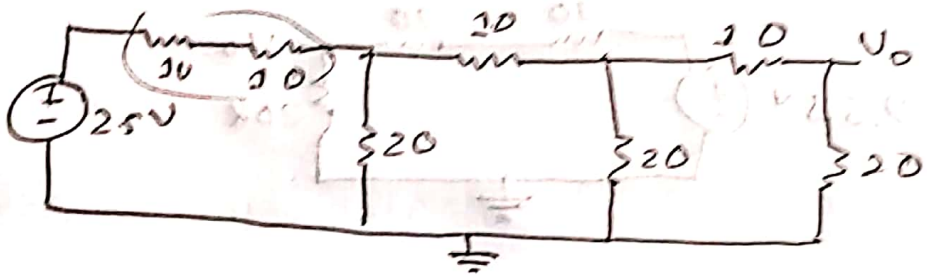


$$\therefore I = \frac{5V}{20k} = 0.25mA$$

=)

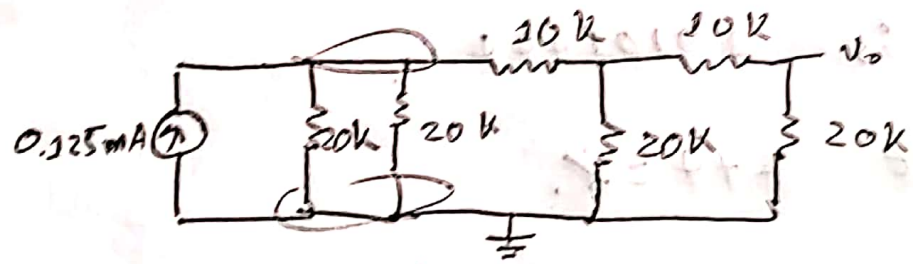


$R = \left(\frac{1}{20} + \frac{1}{20}\right)^{-1} = 10\,K\Omega \qquad V = 0.25 \times 10 = 2.5\,V$

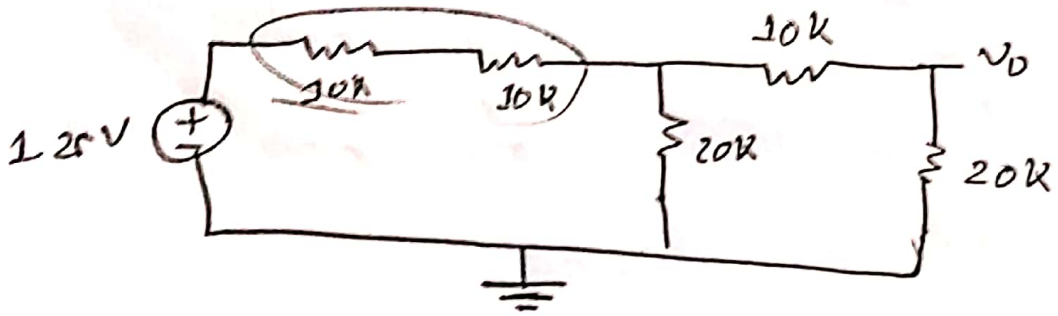


$R = (10+10)K = 20K\Omega \qquad I = \frac{0.25\,V}{20\,K} = 0.125\,mA$

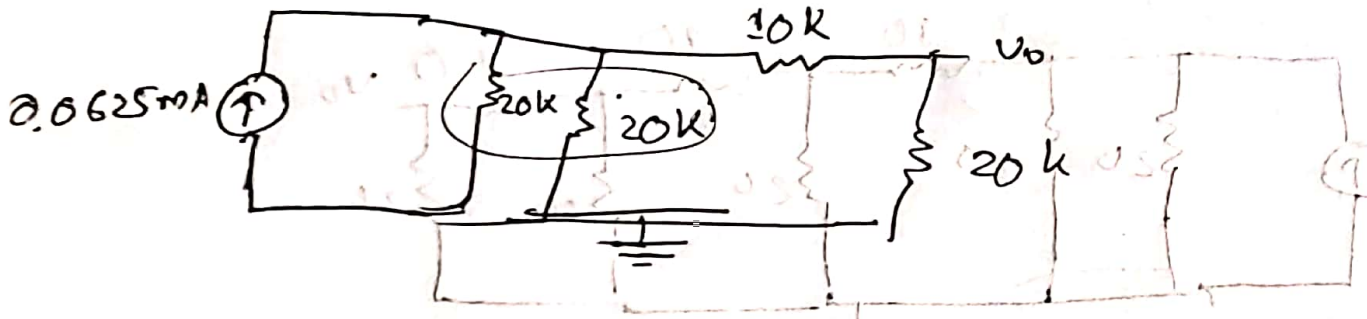
②



$R = \left(\frac{1}{20} + \frac{1}{20}\right)^{-1} = 10\,K\Omega \qquad V = 0.125mA \times 10K = 1.25V$

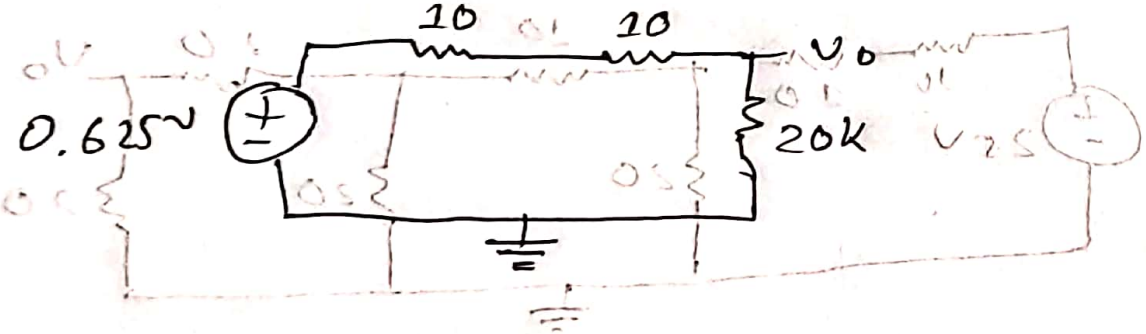


$R = (10+10) = 20K \qquad I = \frac{1.25\,V}{20K} = 0.0625\,mA$



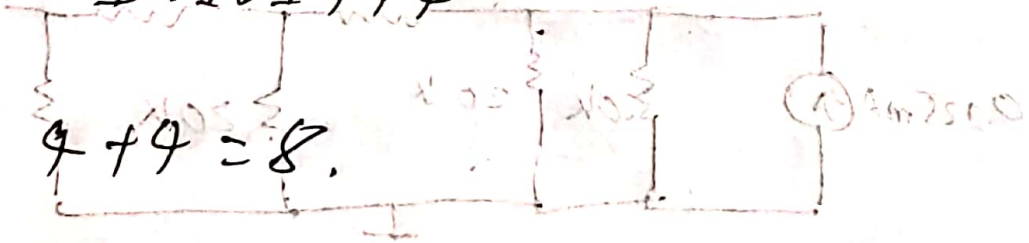
$$R = \left(\frac{1}{20} + \frac{1}{20}\right)^{-1} = 10\,k\Omega$$

$$V = 0.0625\ mA \times 10\ k = 0.625\ V$$



Thus we get $0.625 \approx 0.62\ V$

4. My id is 19101444



here $4+4=8$.

4.

Datasheet for circuit 1:

Input configuration	D	C	B	A	Output Voltage, Vo(V)
1	0	0	0	0	0.0027
2	0	0	0	1	-0.797
3	0	0	1	0	-1.597
4	0	0	1	1	-2.397
5	0	1	0	0	-3.197
6	0	1	0	1	-3.997
7	0	1	1	0	-4.797
8	0	1	1	1	-5.597
9	1	0	0	0	-6.397
10	1	0	0	1	-7.197
11	1	0	1	0	-7.997
12	1	0	1	1	-8.797
13	1	1	0	0	-9.597
14	1	1	0	1	-10.397
15	1	1	1	0	-11.197
16	1	1	1	1	-11.997

5.

We know,

$$\text{Resolution} = \frac{RF}{R_1} V_{high}$$

and we get resolution from step size.

so, step $\propto$ RF.

trinket Python3 Run Share Remix

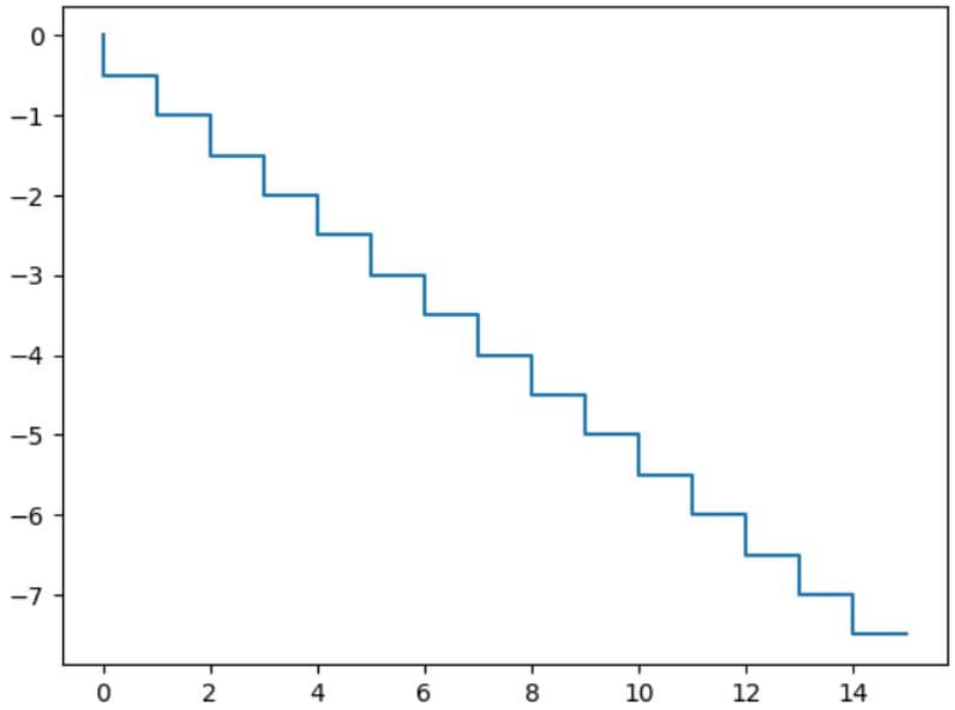
main.py

```
# Online Python compiler (interpreter) to run Python online.
# Write Python 3 code in this online editor and run it.
# Get started with interactive Python!
# Supports Python Modules: builtins, math,pandas, scipy
# matplotlib.pyplot, numpy, operator, processing, pygal, random,
# re, string, time, turtle, urllib.request
import matplotlib.pyplot as plt
import pandas as pd
import numpy as np
import scipy as sp
import matplotlib.pyplot as plt

x = [0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15]
y = [0,-0.5,-1,-1.5,-2,-2.5,-3,-3.5,-4,-4.5,-5,-5.5,-6,-6.5,-7,-7.5]

plt.step(x, y)
plt.show()
```

Powered by trinket



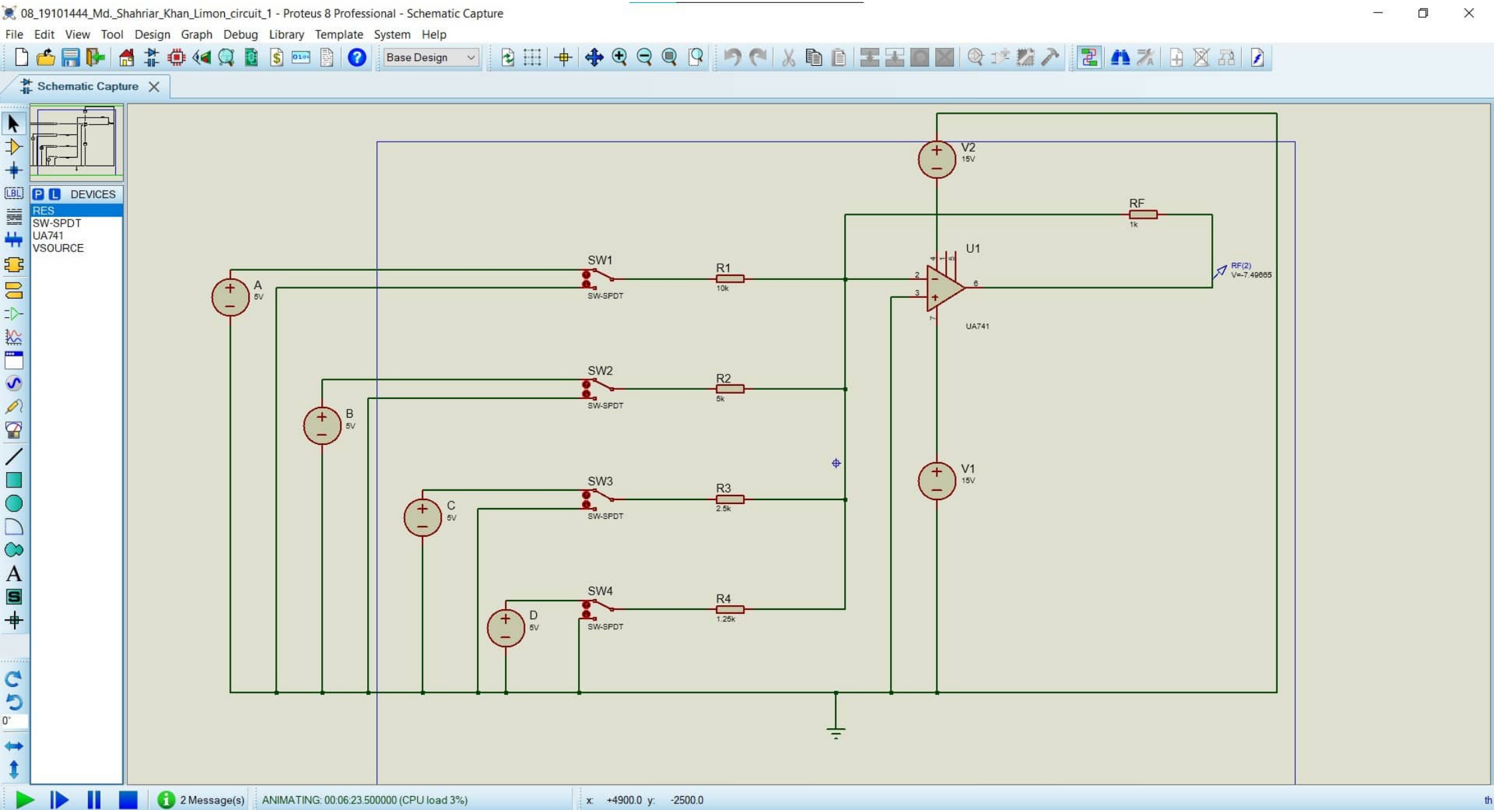
trinket_plot.png

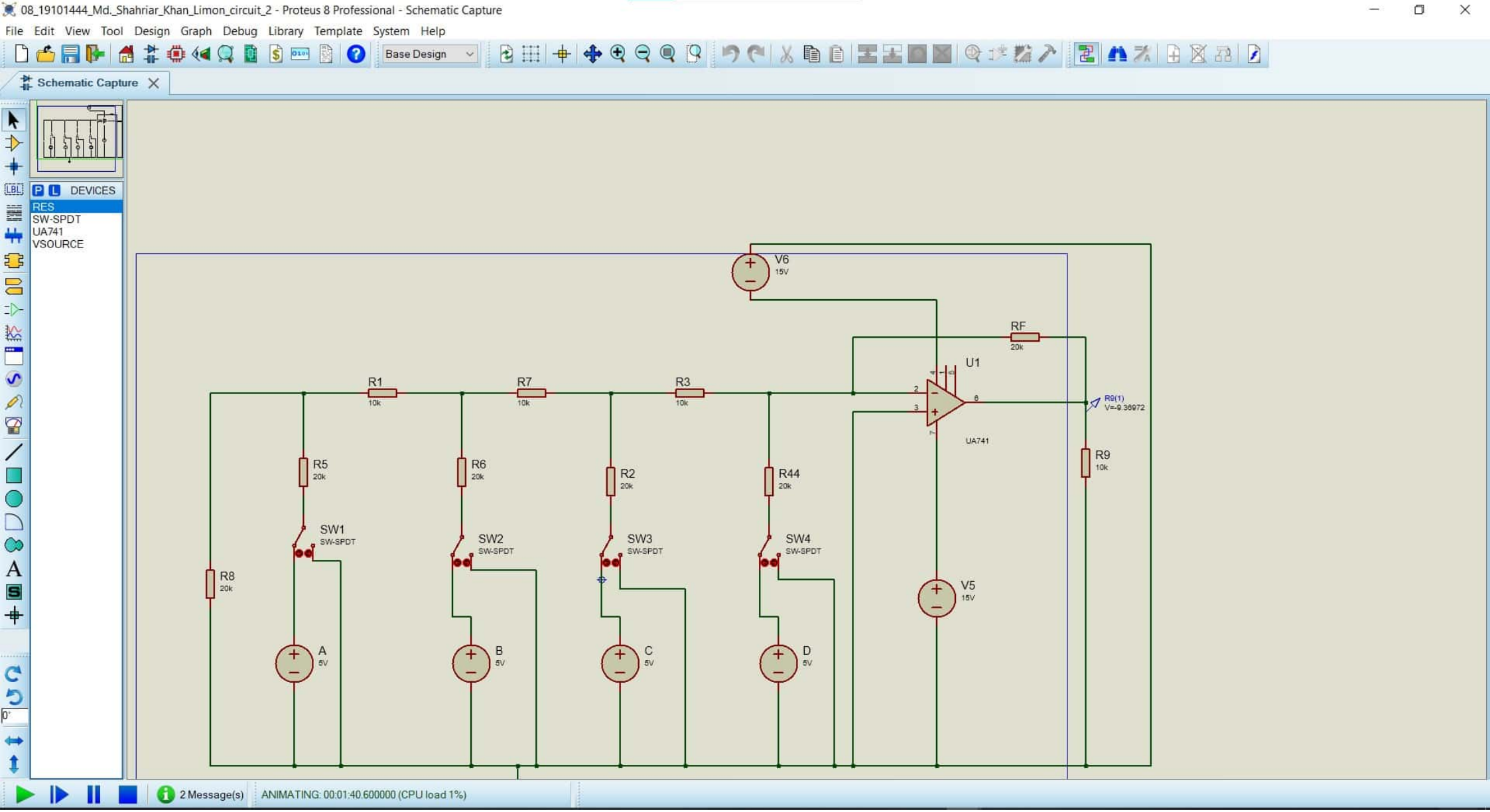
Datasheet for circuit 1:

Input configuration	D	C	B	A	Output Voltage, Vo(V)
1	0	0	0	0	0.00271
2	0	0	0	1	-0.497
3	0	0	1	0	-0.997
4	0	0	1	1	-1.497
5	0	1	0	0	-1.997
6	0	1	0	1	-2.497
7	0	1	1	0	-2.997
8	0	1	1	1	-3.497
9	1	0	0	0	-3.997
10	1	0	0	1	-4.497
11	1	0	1	0	-4.997
12	1	0	1	1	-5.497
13	1	1	0	0	-5.997
14	1	1	0	1	-6.497
15	1	1	1	0	-6.997
16	1	1	1	1	-7.497

Datasheet for circuit 2:

Input configuration	D	C	B	A	Output Voltage, Vo(V)
1	0	0	0	0	0.00495
2	0	0	0	1	-0.620
3	0	0	1	0	-1.245
4	0	0	1	1	-1.869
5	0	1	0	0	-2.495
6	0	1	0	1	-3.119
7	0	1	1	0	-3.744
8	0	1	1	1	-4.369
9	1	0	0	0	-4.995
10	1	0	0	1	-5.619
11	1	0	1	0	-6.245
12	1	0	1	1	-6.869
13	1	1	0	0	-7.491
14	1	1	0	1	-8.119
15	1	1	1	0	-8.745
16	1	1	1	1	-9.369


08_19101444_Md._Shahriar_Khan_Limon_circuit_1 - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
DEVICES
RES
SW-SPDT
UA741
VSOURCE
A
5V
B
5V
C
5V
D
5V
SW1
SW2
SW3
SW4
SW-SPDT
R1
10k
R2
5k
R3
2.5k
R4
1.25k
RF
1k
U1
UA741
RF(2)
V=-7.49665
V1
15V
V2
15V
2 Message(s)
ANIMATING: 00:06:23.500000 (CPU load 3%)
x: +4900.0 y: -2500.0


08_19101444_Md._Shahriar_Khan_Limon_circuit_2 - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
DEVICES
RES
SW-SPDT
UA741
VSOURCE
V6
15V
RF
20k
U1
UA741
R1
10k
R7
10k
R3
10k
R9(1)
V=-9.36972
R9
10k
R5
20k
R6
20k
R2
20k
R44
20k
SW1
SW-SPDT
SW2
SW-SPDT
SW3
SW-SPDT
SW4
SW-SPDT
R8
20k
V5
15V
A
5V
B
5V
C
5V
D
5V
2 Message(s)
ANIMATING: 00:01:40.600000 (CPU load 1%)