SHAHRIAR KHAN

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RESEARCH INTERESTS

FET-Based Biosensors · Tunnel FETs · 2D Materials · Semiconductor Device Physics · Nanoelectronic Devices

EDUCATION

- **Bangladesh University of Engineering and Technology** *2024 - Present*
  M.Sc. in Electrical and Electronic Engineering
  Major: Electronics and Photonics

- **Bangladesh University of Engineering and Technology** *2018 - 2024*
  B.Sc. in Electrical and Electronic Engineering CGPA: 3.77/4.00
  Major: Electronics
  Thesis: Designing the Cavity Architecture in Double Gate Junctionless Field Effect Transistor for Enhanced Biomolecule Detection
  Supervisor: Dr. Ehsanur Rahman

TECHNICAL STRENGTHS

Computer Languages	C, MATLAB
Development Environment	Silvaco TCAD, Cadence, Quartz, Proteus, PSPICE, AutoCAD, Windows

RELEVANT COURSEWORK

Solid State Devices · Compound state devices · Electrical Properties of Materials · VLSI Circuit and Design · Analog Integrated Circuit and Design · Microprocessor and Embedded System · Digital Electronics · Optoelectronics · Processing and Fabrication Technology

PUBLICATIONS

- **Shahriar Khan**, Ehsanur Rahman, *"Designing the Cavity Architecture in Double Gate Junctionless Field Effect Transistors for Enhanced Biomolecule Detection."* *Nanoscale Advances*, 7(12), 3746–3763 (2025) · DOI:10.1039/D4NA00928B

RESEARCH PROJECTS

Polar Gate Engineering and Cavity Optimization in JL-TFET Biosensors for Ultra-Sensitive Label-Free Detection [MS Thesis] Ongoing *January 2025*
BUET *Supervised by Dr. Ehsanur Rahman*

· Investigating optimal placement of the polar gate by analyzing various biosensing parameters to identify the best configuration.
· Assessing different cavity architectures and varying gate work function to optimize overall device performance.

Comparative Design of TMDC and Si-based Junctionless TFETs for Biosensing Applications Ongoing *July 2025*
BUET *Supervised by Dr. Ehsanur Rahman*

· Evaluating TMDC materials versus silicon in junctionless TFETs for biomolecule detection using identical device parameters.
· Conducting TCAD simulations and MATLAB analysis to compare structural and electrical performance across both material platforms.

Automated Experimental Setup to Measure Optical Power-Current Characteristics of LEDs *January 2024*
[Under Review]
BUET *Supervised by Dr. Md Zunaid Baten*

· Developed a low-cost Arduino-driven setup to measure LED L–I characteristics, incorporating an LDR and black-box design with two-step calibration.
· Validated measurements against a standard optical power meter and plotted accurate L–I curves for red, green, and blue LEDs in MATLAB.

8:1 Analog Multiplexer Design in Cadence Virtuoso *July 2023*
BUET *Supervised by Dr. Muhammad Abdullah Arafat*

· Designed an 8:1 analog multiplexer using hierarchical 2:1 blocks with selector logic and transmission gates.
· Conducted schematic simulations to verify correct switching behavior.

Hybrid 4-Way Traffic Control System Using 74-Series ICs *July 2023*
BUET *Supervised by Dr. Lutfa Akter*

· Designed a 4-way traffic control system with jam management, priority handling for emergency/VIP vehicles, and pedestrian automation, with manual override using 74-series ICs.

Automated Greenhouse Control System Using Feedback *July 2023*
BUET

· Developed an Arduino UNO–based greenhouse prototype integrating sensors for climate and soil regulation.
· Implemented feedback control to maintain optimal conditions and support sustainable farming.

WORK EXPERIENCE

- **Adjunct Lecturer**, Department of EEE *Fall 2024–Present*

  Ahsanullah University of Science and Technology

  Courses: Electronic Circuits I and LAB · Electrical Circuits I and II · Electrical Properties of Materials

  Responsibilities: Conducted theory and laboratory classes and provided mentorship to a group of 25 students, including assignment evaluation, academic guidance, and grading for the final exam.

INTERNSHIP

- **THiNK Silicon** *November 2023*
  - Supported embedded system tasks focusing on SCADA Modbus protocols in industrial automation.
  - Exposed to PCB design processes, including circuit layout and hardware development.

ACHIEVEMENTS

- Earned placement on the **Dean's Award List** for two consecutive semesters
- Honored with **University Merit Scholarship** for academic excellence in three terms
- Placed in the **top 2%** (Rank 216/12,000) in the BUET Admission Test (2018).
- Awarded **Talent Pool scholarship** in JSC,2013, and **General scholarship** in SSC,2016

REFERENCES

Dr. Ehsanur Rahman
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Dr. Mohammad Jahangir Alam
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