Bangladesh University of Engineering and Technology

Department of Computer Science and Engineering

Course: CSE 206 (Digital Logic Design Sessional)
Experiment No. 7
Topic: Flip-Flops and Registers

Implement the following problems:

1. Design and implement a **master-slave JK** flip-flop using only **NAND** gates.
2. Design and implement a 4-bit universal shift register.

Report:
For each of the problems above, the report should cover the following items:
1. Problem specification.
2. Excitation Table.
3. Truth table and function minimization (if required)
4. Required instruments.
5. Circuit diagram.
6. Observations (if any).

Submission Instruction:
1. Prepare separate circ file for each problem. Name each file as follows:
Sec_<SectionName>_Group_<GroupID>_Problem_<ProblemNo>.circ
2. Prepare one report for all the problems. Name it Sec_<SectionName>_Group_<GroupID>_Report.pdf.
3. Put all the above items in a folder that is named as Sec_<SectionName>_Group_GroupID.
4. Zip the above folder, name it as Sec_<SectionName>_Group_GroupID.zip
5. Submit the zip file.
6. The submission deadline is 11:55pm, June 12, 2021.