Bangladesh University of Engineering and Technology

Course: CSE 206

Digital Logic Design Sessional

Experiment 4
Comparator, Adder and Subtractor

Group No: 05

Section: B2

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Problem-1

Problem Specification:

In this problem, we have to design a 2-bit comparator to compare 2-bit numbers P and Q using basic gates where there will be 3 output lines to indicate P > Q, P=Q, and P < Q

Required Instrument:

1. Logisim software
2. 2 IC 7408
3. 1 IC 7432
4. 1 IC 7404
5. 1 IC 7486
6. 4 input pins and 3 output pins
7. Electric wires

Truth Table:

P_1	P_0	Q_1	Q_0	G (P>Q)	E (P=Q)	L (P<Q)
0	0	0	0	0	1	0
0	0	0	1	0	0	1

0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

Simplification of Formula:

The Boolean functions are:

$G(P_1,P_0,Q_1,Q_0) = \sum (4,8,9,12,13,14)$

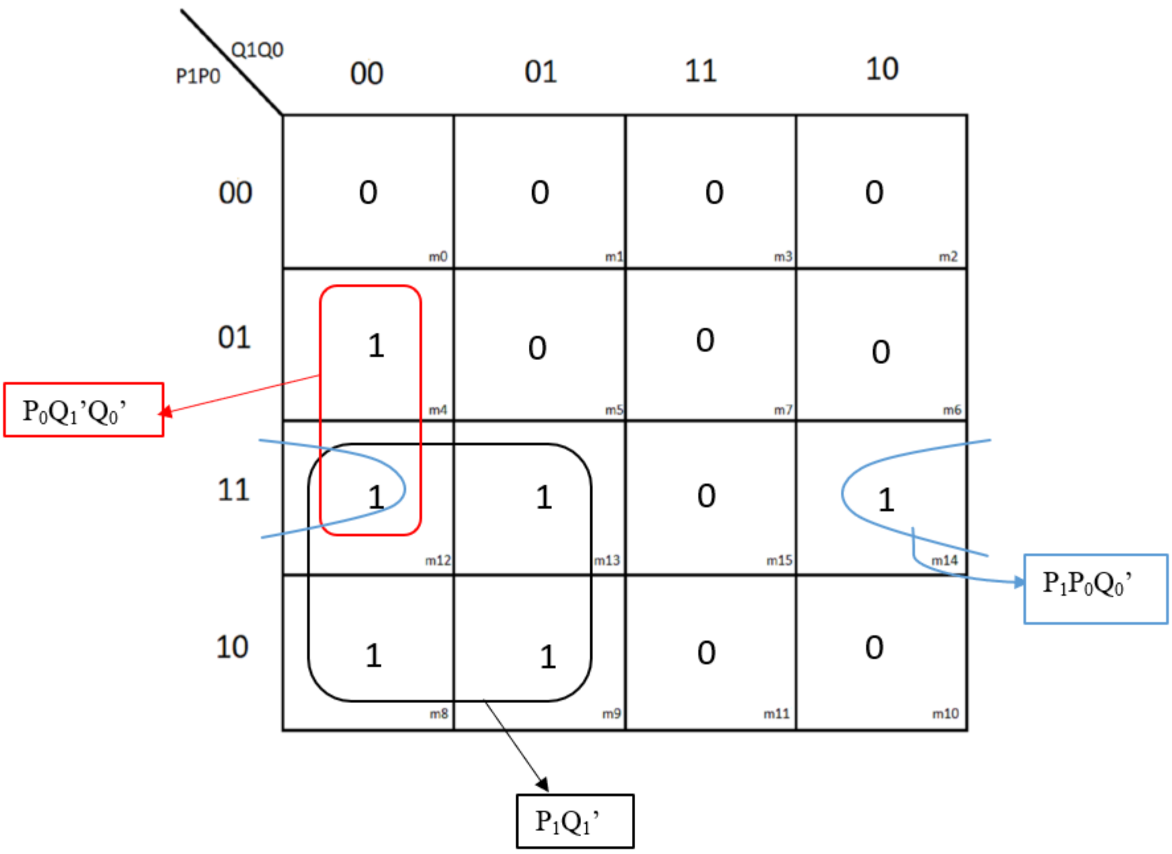
$E(P_1,P_0,Q_1,Q_0) = \sum (0,5,10,15)$

$L(P_1,P_0,Q_1,Q_0) = \sum (1,2,3,6,7,11)$

To simplify those equations we need K-MAP

K-MAP For G(P>Q):

$G(P_1,P_0,Q_1,Q_0) = \sum (4,8,9,12,13,14)$



From K-MAP the simplified equation of G is

$G(P_1,P_0,Q_1,Q_0) = P_1Q_1' + P_1P_0Q_0' + P_0Q_1'Q_0'$

K-MAP For E(P=Q):

$E(P_1,P_0,Q_1,Q_0) = \sum (0,5,10,15)$

P1P0 \ Q1Q0	00	01	11	10
00	$\boxed{1}$ m0	0 m1	0 m3	0 m2
01	0 m4	$\boxed{1}$ m5	0 m7	0 m6
11	0 m12	0 m13	$\boxed{1}$ m15	0 m14
10	0 m8	0 m9	0 m11	$\boxed{1}$ m10

From K-MAP the simplified equation of E is

$E(P_1,P_0,Q_1,Q_0)$

$= P_1P_0Q_1Q_0 + P_1'P_0Q_1'Q_0 + P_1P_0'Q_1Q_0' + P_1'P_0'Q_1'Q_0'$

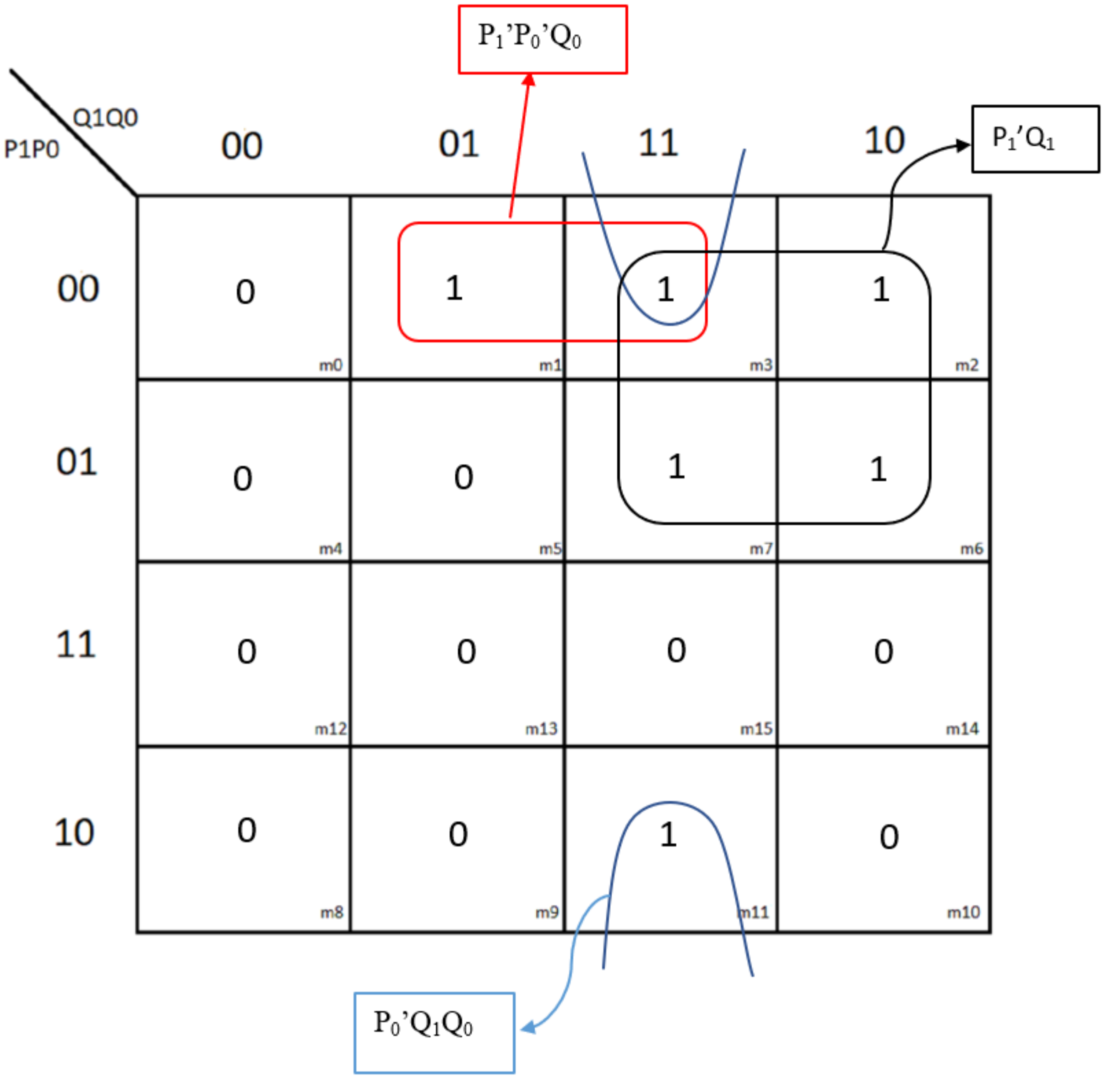
$=P_1Q_1(P_0Q_0+P_0'Q_0') + P_1'Q_1'(P_0Q_0+P_0'Q_0')$

$=(P_0Q_0+P_0'Q_0')\,(P_1Q_1 + P_1'Q_1')$

$= (P_0 \oplus Q_0)'\,(P_1 \oplus Q_1)'$

K-MAP For L(P<Q):

$L(P_1,P_0,Q_1,Q_0) = \sum(1,2,3,6,7,11)$



From K-MAP the simplified equation of L is

$L(P_1,P_0,Q_1,Q_0) = P_1'Q_1 + P_1'P_0'Q_0 + P_0'Q_1Q_0$

Circuit Diagram :

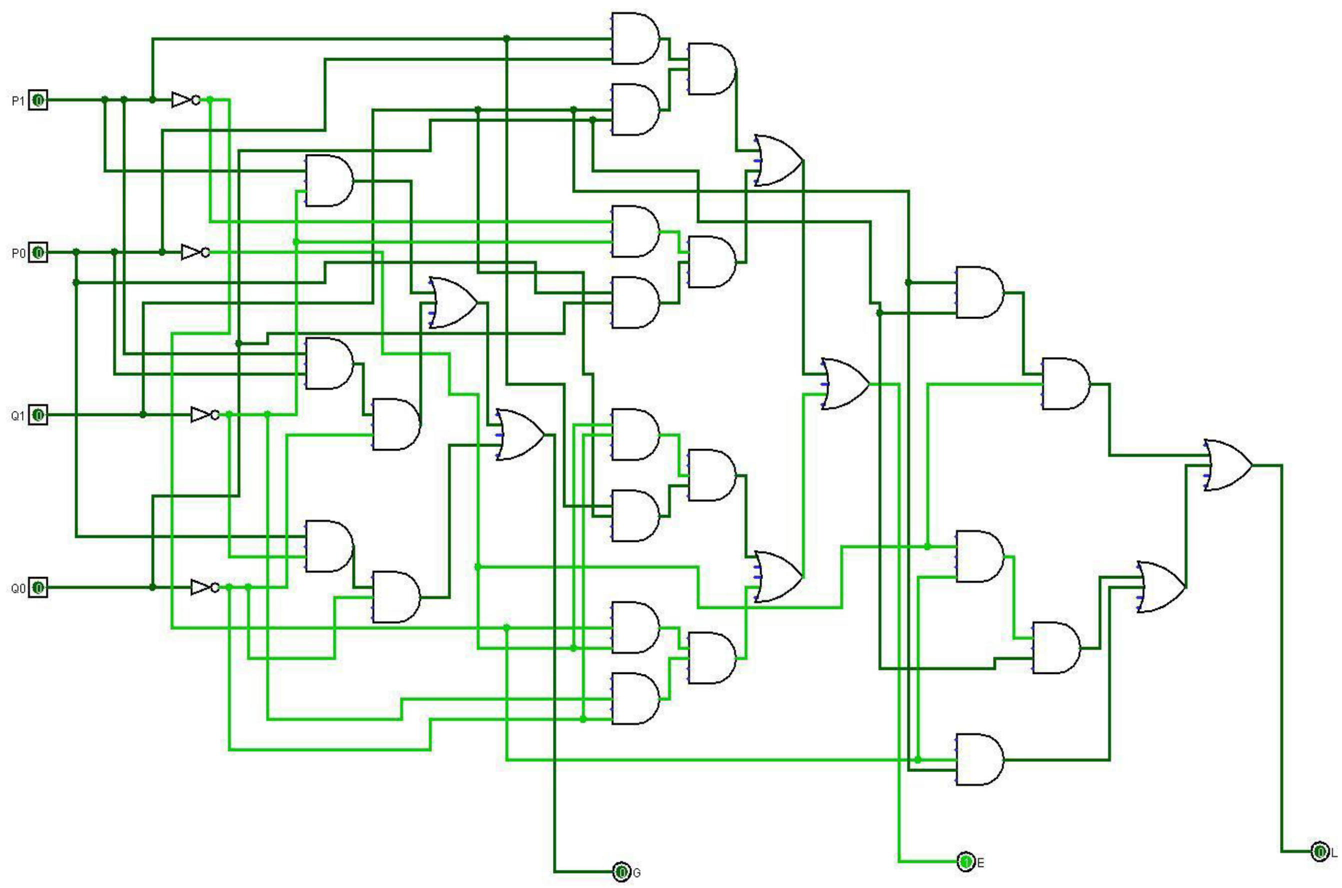


Figure 1: 2-Bit Comparator Circuit

Problem -2

Problem Specification:

In this problem, we have to design a 1-bit full subtractor circuit using basic logic gates where the inputs are D, E, and F denoting minuend, subtrahend, and previous borrow respectively. The outputs are R and B representing the difference and output borrow.

Required Instruments:

1. Logisim software
2. 2 IC 7408
3. 1 IC 7432
4. 1 IC 7404
5. 1 IC 7486
6. 3 input pins and 2 output pins
7. Electric wires

Truth Table:

D	E	F	R	B
0	0	0	0	0
0	0	1	1	1

0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Simplification of Boolean Function:

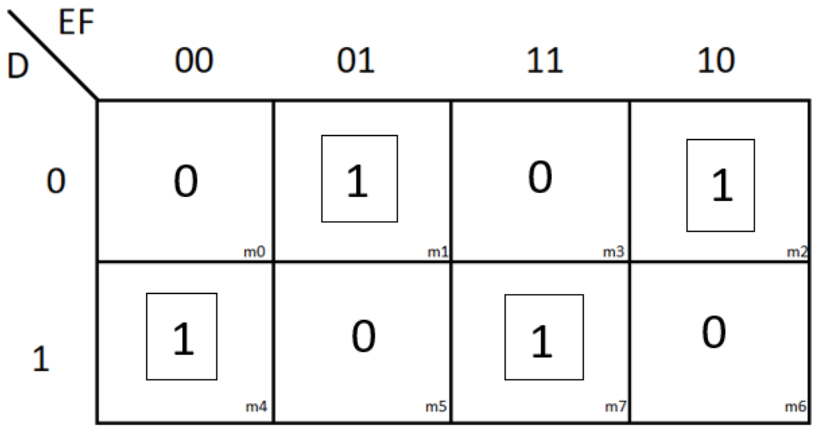
The Boolean functions are:

R(D,E,F) = $\sum(1,2,4,7)$

B(D,E,F) = $\sum(1,2,3,7)$

Using K-map for simplification:

K-MAP For R:



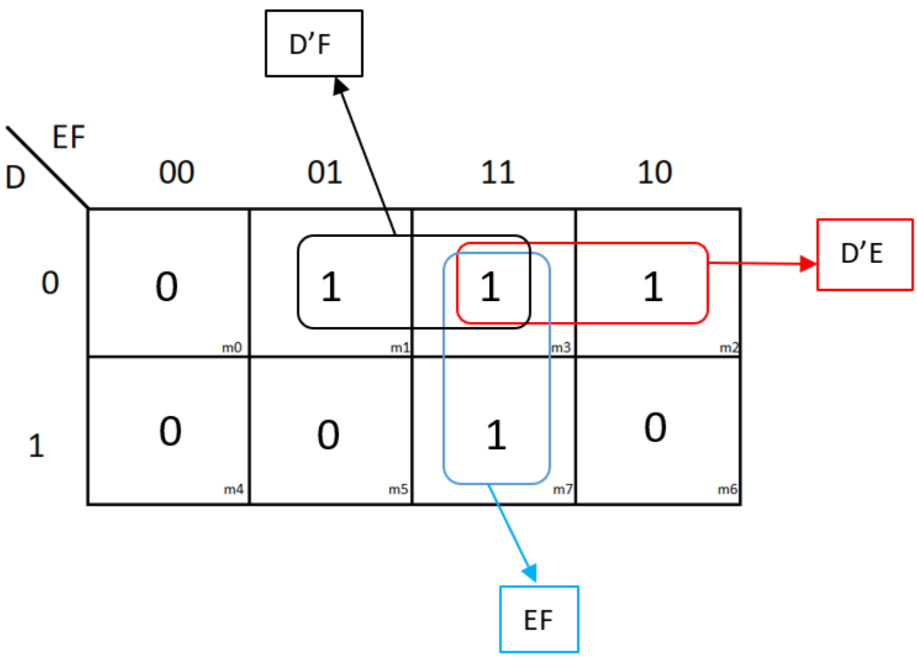
$R(D,E,F) = DE'F' + D'E'F + DEF + D'EF'$

$= D(EF + E'F') + D'(E'F + EF')$

$= D(E \oplus F)' + D'(E \oplus F)$

$= D \oplus E \oplus F$

K-MAP For B:



$B(D,E,F) = D'E+D'F+EF$

Circuit Diagram:

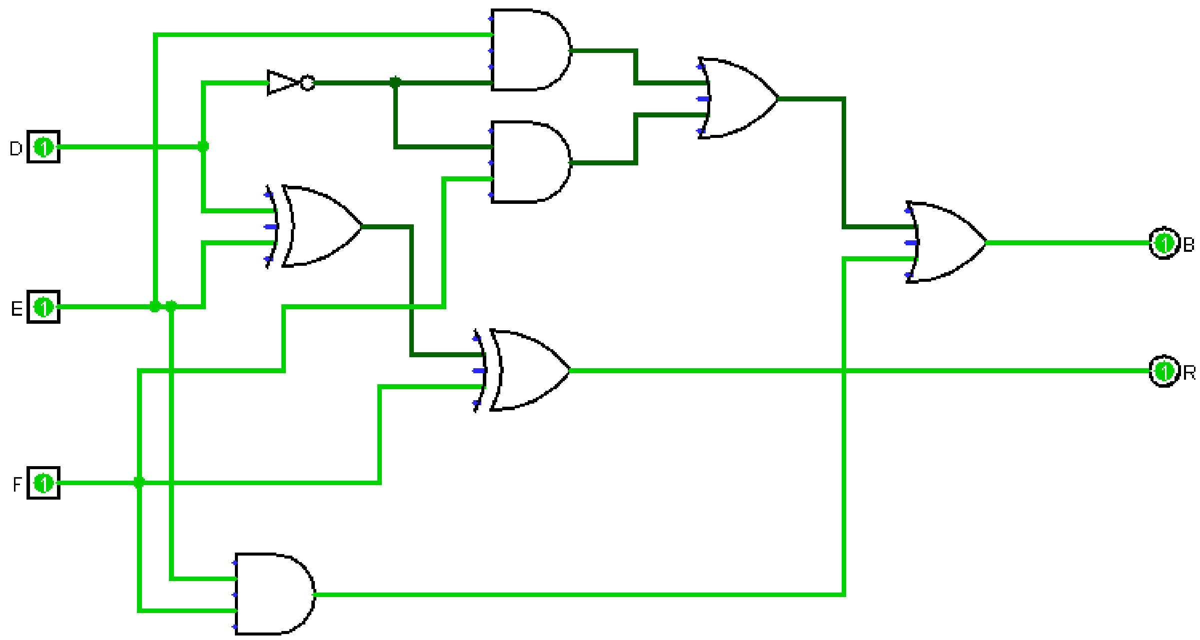


Figure 2: 1 Bit Full Subtractor