The University of Azad Jammu & Kashmir, Muzaffarabad

Computer Architecture & Logic Design

Lab 07: Encoder & Decoder

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LAB Objective

To design, simulate, and verify the working of:

1. A **Digital Encoder**
2. A **Digital Decoder**

using the Virtual Workbench tool, along with truth tables, circuit diagrams, and proper input-output verification.

IMPORTANCE IN DIGITAL SYSTEMS

- **Data Conversion:** Encoders and decoders enable transformation between human-readable values and machine-level binary codes.
- **Control Signal Generation:** Essential in processors, memory addressing, multiplexing, and display systems.
- **Foundational Circuits:** Base building blocks for ALUs, I/O modules, communication systems, and instruction decoding.

Encoder

What is an Encoder?

An encoder is a combinational logic circuit that converts active input signals into a coded binary output. It has 2^n input lines and n output lines, where only one input line is active at a time.

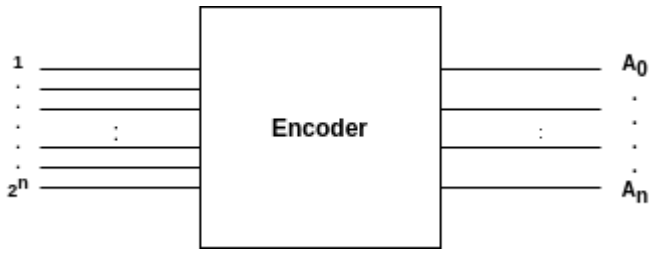
Logic Equations:

For an 8-to-3 encoder:

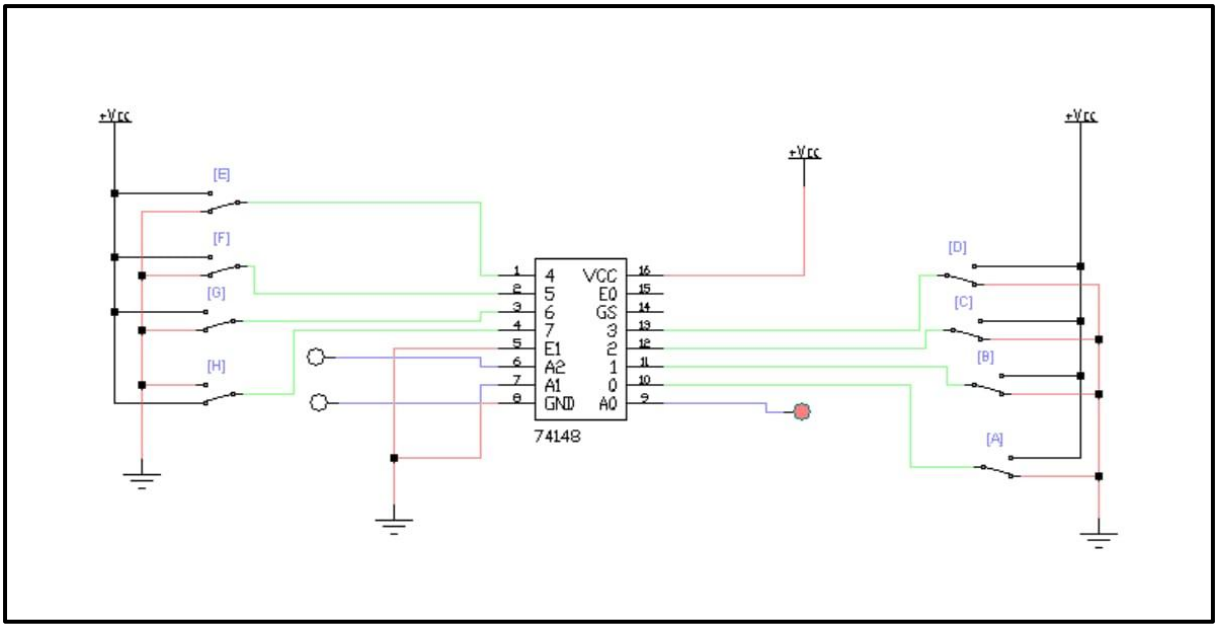
- $A_2 = D_4 + D_5 + D_6 + D_7$
- $A_1 = D_2 + D_3 + D_6 + D_7$
- $A_0 = D_1 + D_3 + D_5 + D_7$

Only one input should be HIGH at any time for correct encoding.

Block Diagram:



Implementations in EWB



TRUTH TABLE OF ENCODER (8 to 3)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A_2	A_1	A_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

2. Decoder

A Decoder is a combinational circuit that translates *n-bit binary input* into 2^n *unique outputs*. Each output represents one possible input combination and is activated when that binary code is received.

Logic Equations

For a 3-to-8 decoder:

$Y_0 = \overline{A}_2 \cdot \overline{A}_1 \cdot \overline{A}_0$

$Y_1 = \overline{A}_2 \cdot \overline{A}_1 \cdot A_0$

$Y_2 = \overline{A}_2 \cdot A_1 \cdot \overline{A}_0$

$Y_3 = \overline{A}_2 \cdot A_1 \cdot A_0$

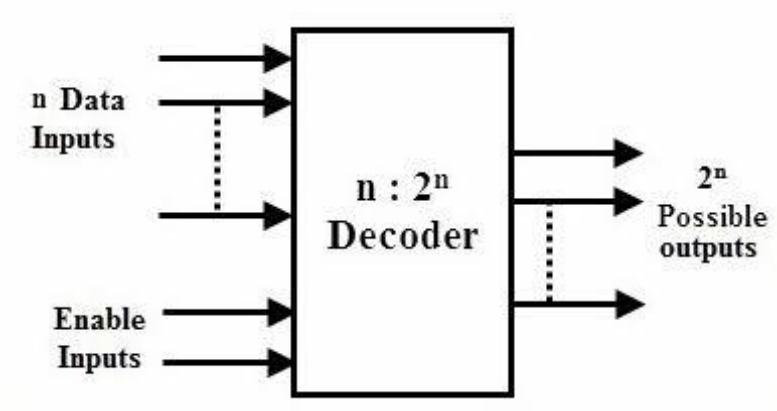
$Y_4 = A_2 \cdot \overline{A}_1 \cdot \overline{A}_0$

$Y_5 = A_2 \cdot \overline{A}_1 \cdot A_0$

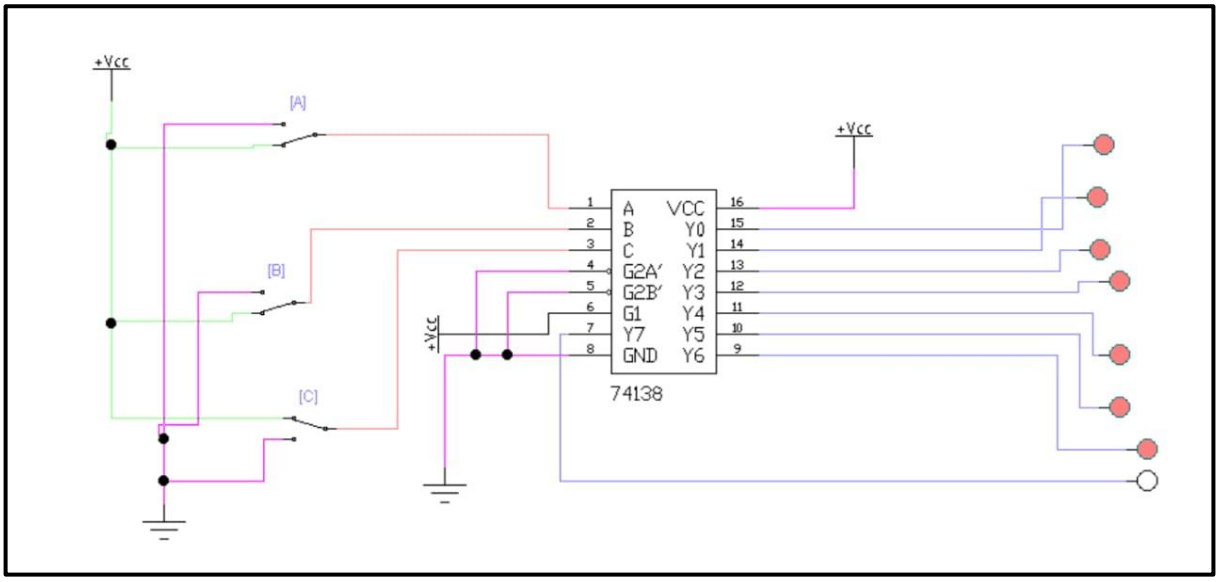
$Y_6 = A_2 \cdot A_1 \cdot \overline{A}_0$

$Y_7 = A_2 \cdot A_1 \cdot A_0$

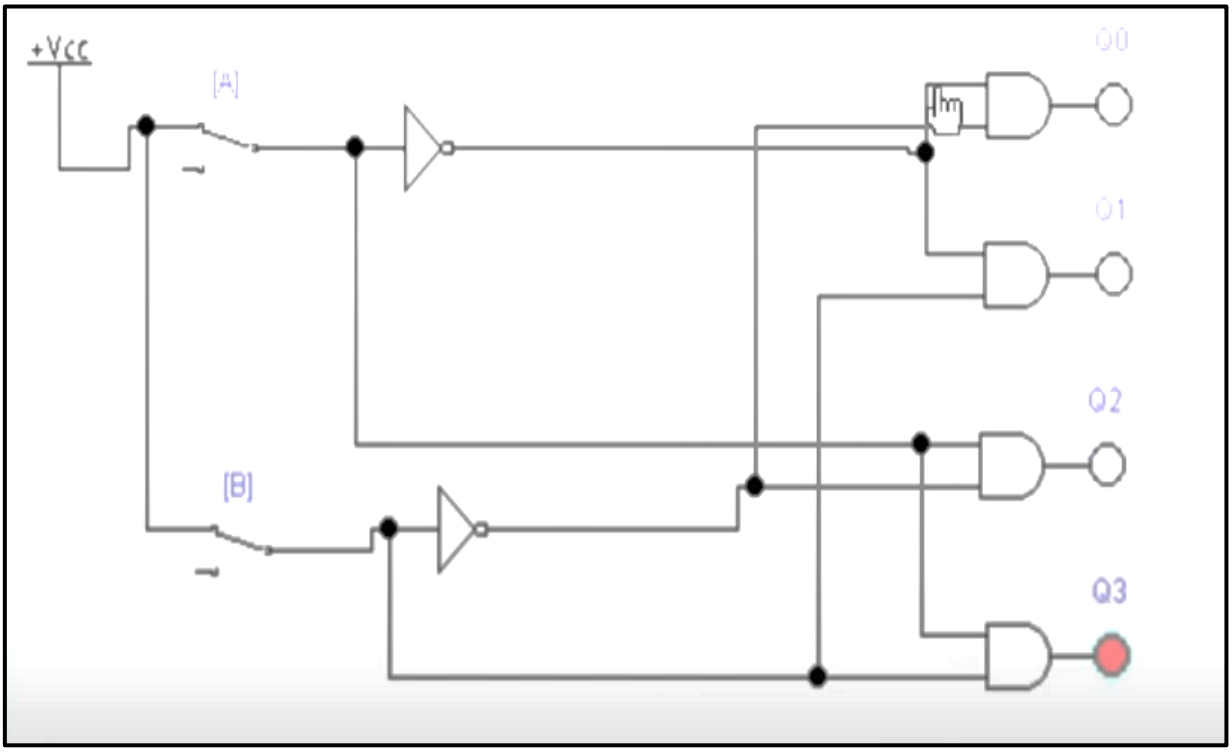
Block Diagram:



Implementation in EWB



Basic Gate Diagram



TRUTH TABLE OF Decoder (3 to 8)

A_2	A_1	A_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0