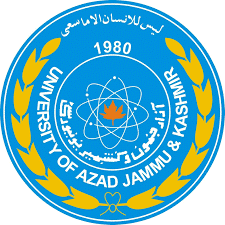
** The University of Azad Jammu & Kashmir, Muzaffarabad**

**Computer Architecture & Logic Design**

|  |  |
| --- | --- |
| **Student Name:** | Shahzad Ahmed Awan |
| **Roll No:** | 2024-SE-15 |
| **Course Title:** | C&LD |
| **Course Code:** | CS-1206 |
| **Instructor:** | Mam Sidra Rafique |
| **Submission Date:** | 20-August-2025 |
| **Department of Software Engineering** | |

**Lab 07: Encoder & Decoder**

**LAB Objective**

To design, simulate, and verify the working of:

1. A **Digital Encoder**
2. A **Digital Decoder**

using the Virtual Workbench tool, along with truth tables, circuit diagrams, and proper input-output verification.

**IMPORTANCE IN DIGITAL SYSTEMS**

* **Data Conversion:** Encoders and decoders enable transformation between human-readable values and machine-level binary codes.
* **Control Signal Generation:** Essential in processors, memory addressing, multiplexing, and display systems.
* **Foundational Circuits:** Base building blocks for ALUs, I/O modules, communication systems, and instruction decoding.

**Encoder**

**What is an Encoder?**

An encoder is a combinational logic circuit that converts active input signals into a coded binary output. It has 2ⁿ input lines and n output lines, where only one input line is active at a time.

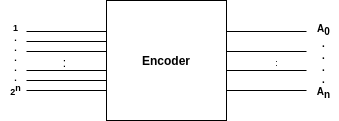
**Logic Equations:**

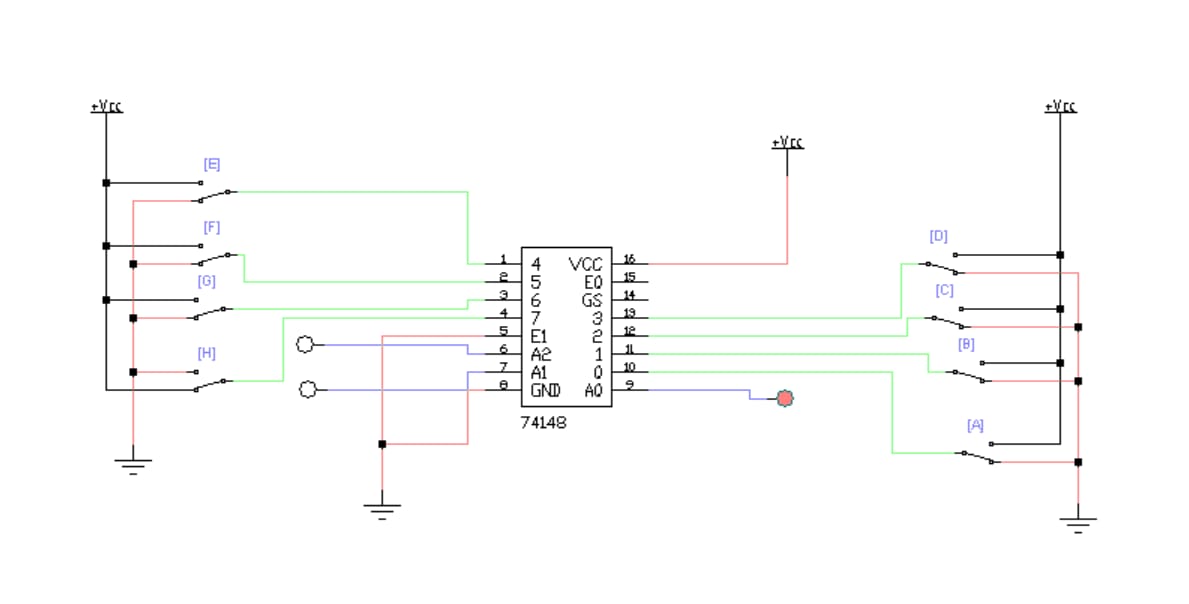
For an 8-to-3 encoder:

* A₂ = D₄ + D₅ + D₆ + D₇
* A₁ = D₂ + D₃ + D₆ + D₇
* A₀ = D₁ + D₃ + D₅ + D₇

Only one input should be HIGH at any time for correct encoding.

**Block Diagram:**

****

**Implementations in EWB**

**TRUTH TABLE OF ENCODER (8 to 3)**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| D₇ | D₆ | D₅ | D₄ | D₃ | D₂ | D₁ | D₀ | A₂ | A₁ | A₀ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

**2. Decoder**

A Decoder is a combinational circuit that translates *n-bit binary input* into *2ⁿ unique outputs*. Each output represents one possible input combination and is activated when that binary code is received.

**Logic Equations**

**For a 3-to-8 decoder:**

**Y₀ = A̅₂·A̅₁·A̅₀**

**Y₁ = A̅₂·A̅₁·A₀**

**Y₂ = A̅₂·A₁·A̅₀**

**Y₃ = A̅₂·A₁·A₀**

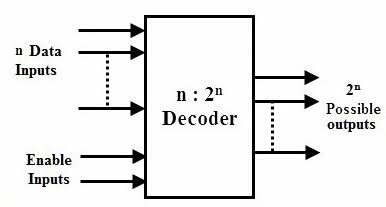
**Y₄ = A₂·A̅₁·A̅₀**

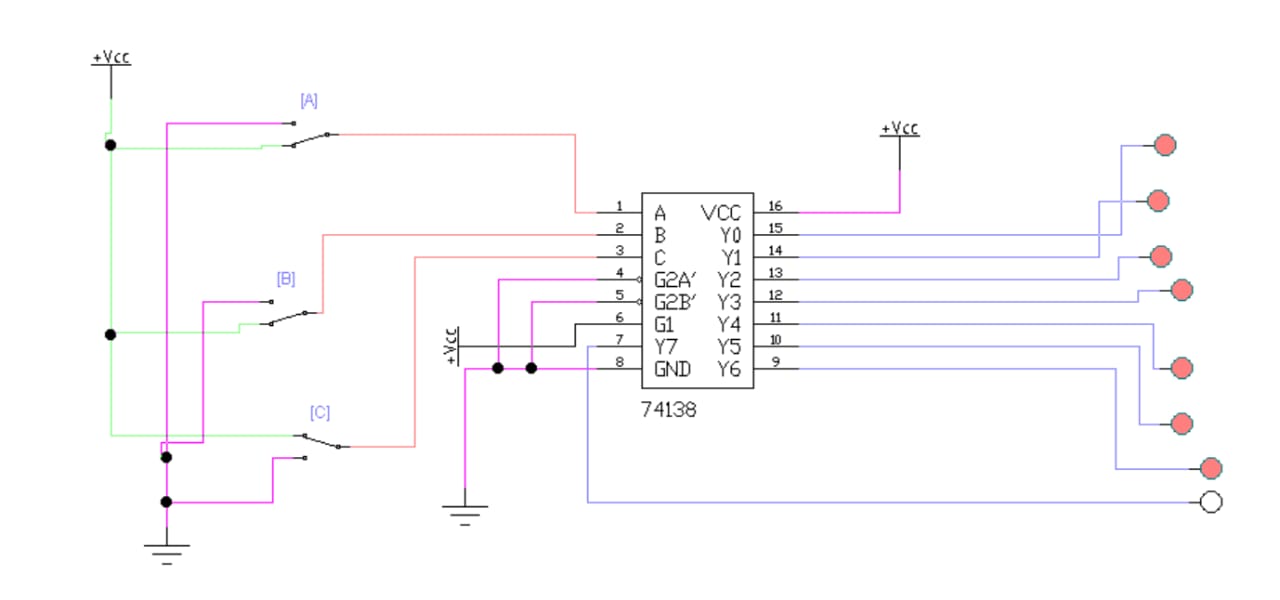
**Y₅ = A₂·A̅₁·A₀**

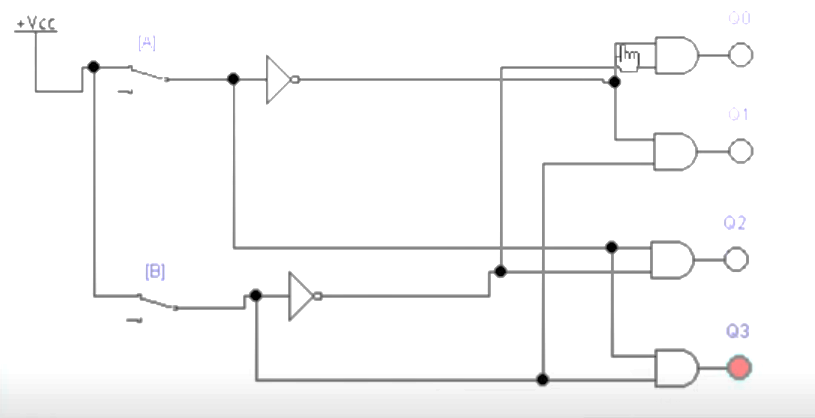
**Y₆ = A₂·A₁·A̅₀**

**Y₇ = A₂·A₁·A₀**

**Block Diagram:**



**Implementation in EWB**

**Basic Gate Diagram**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A₂ | A₁ | A₀ | Y₇ | Y₆ | Y₅ | Y₄ | Y₃ | Y₂ | Y₁ | Y₀ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**TRUTH TABLE OF Decoder (3 to 8)**