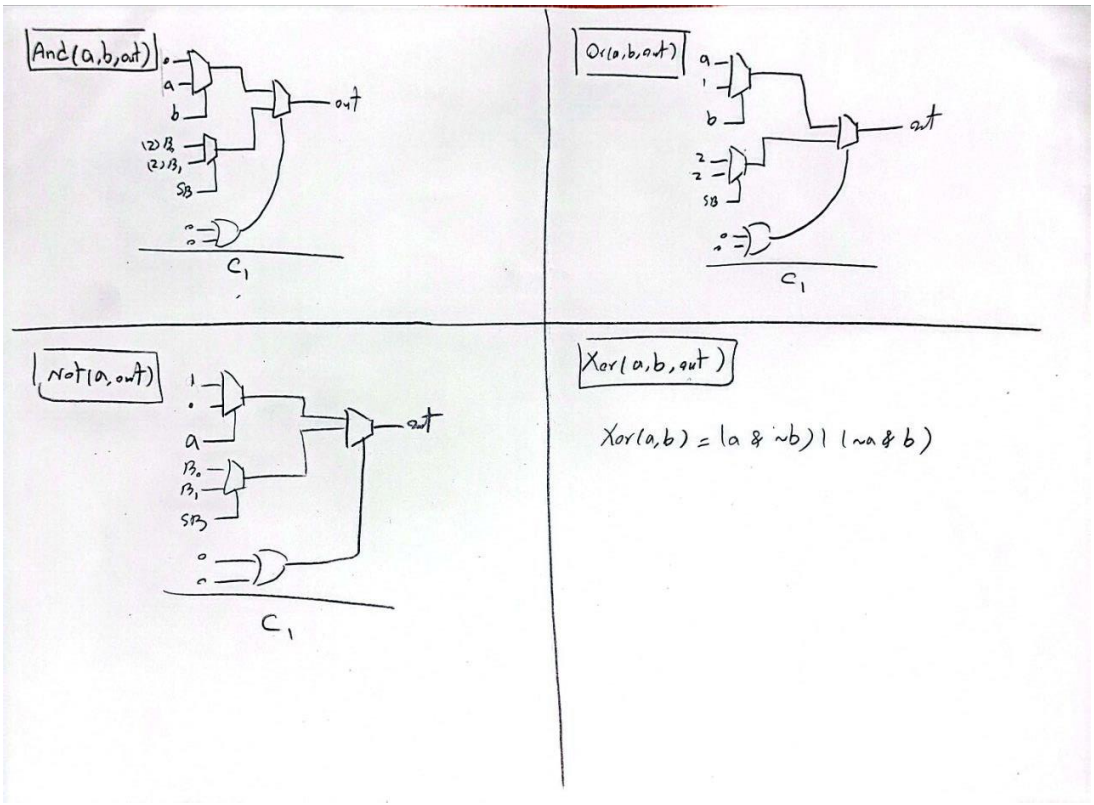
CAD - CA2

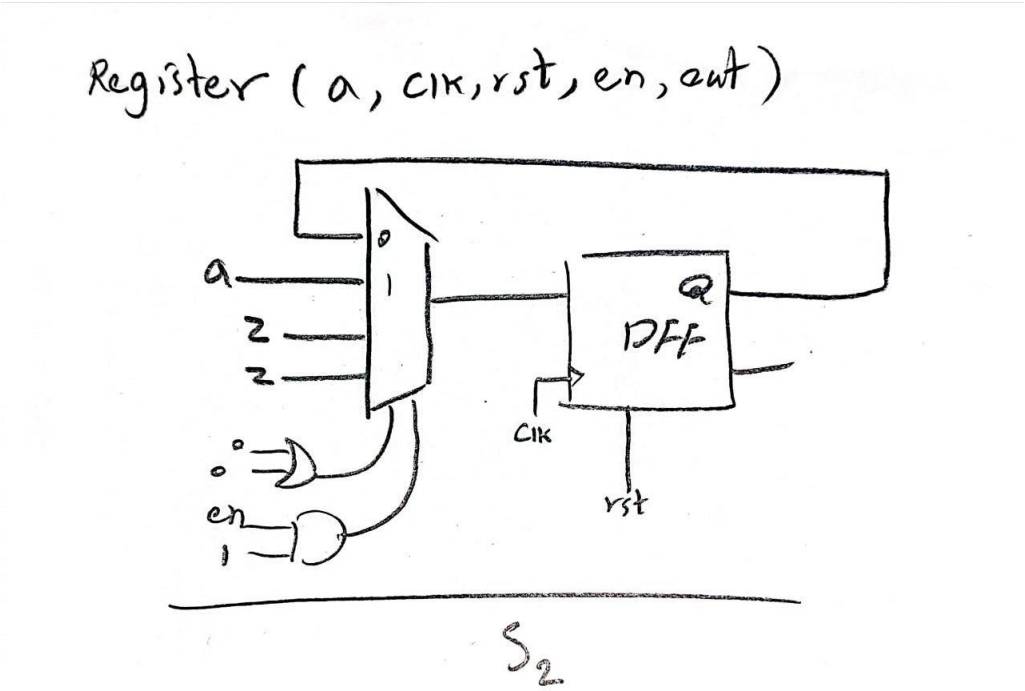
Mohammad Amanlou: 810100084

Shahzad Momayez: 810100272

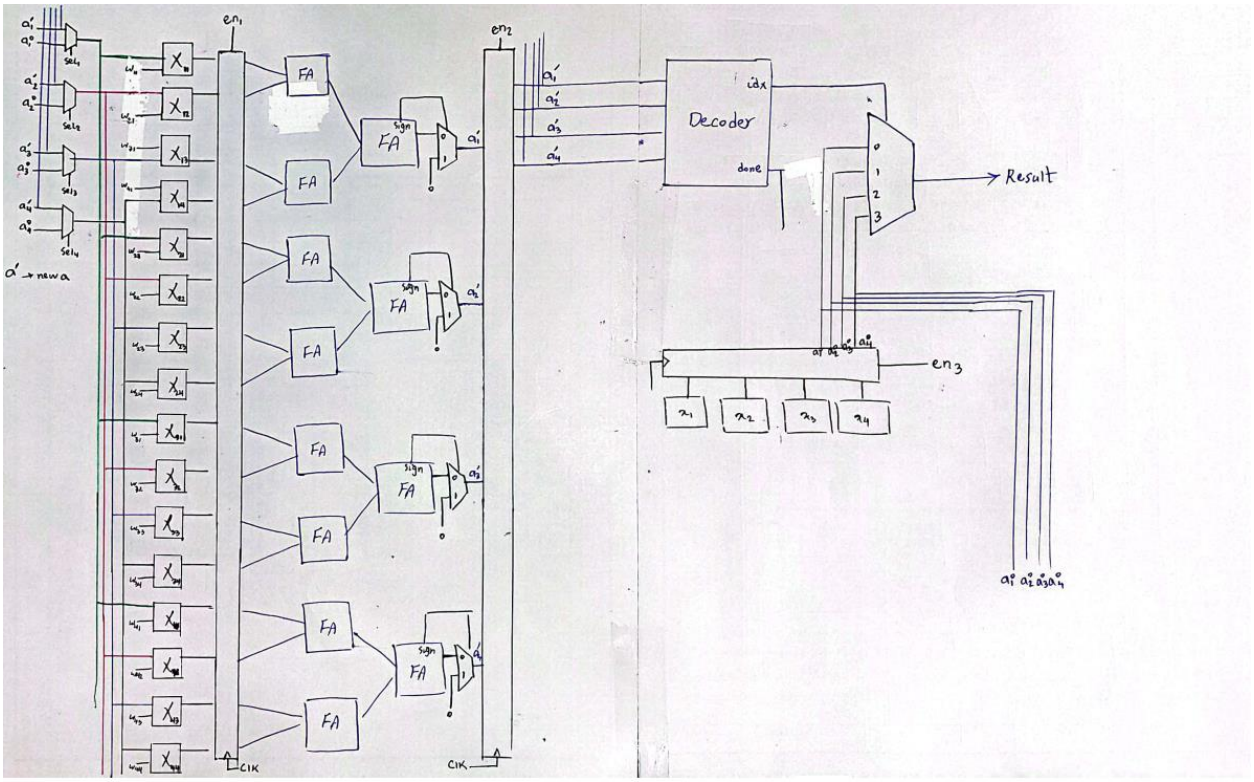
At first, after defining the given basic structures, with a little thought, we defined the basic Verilog gates like and or not.



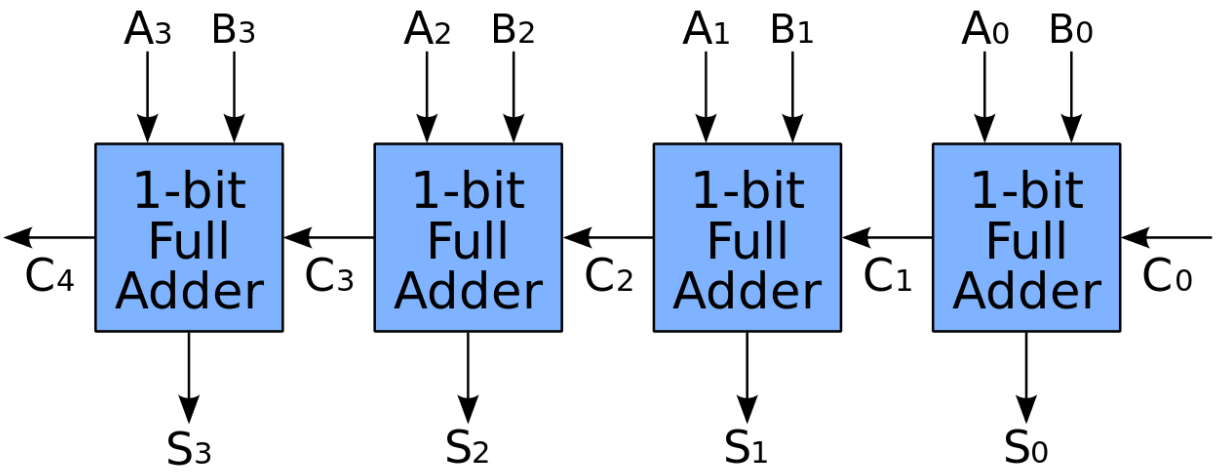
Then we defined a base register as follows:



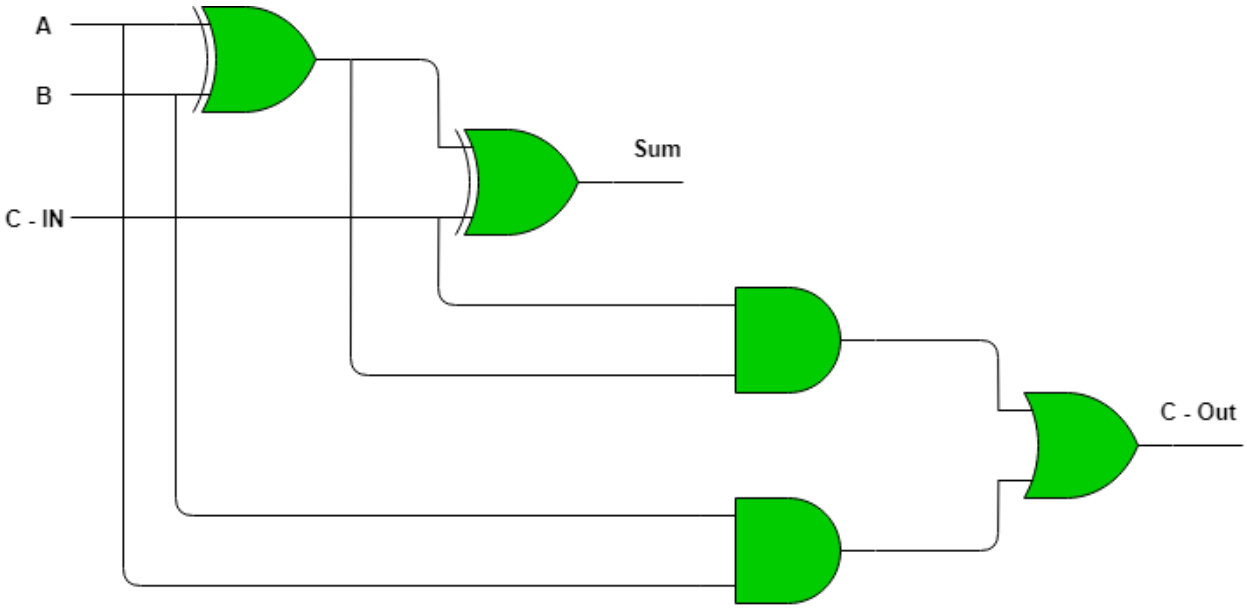
1. **Datapath:**



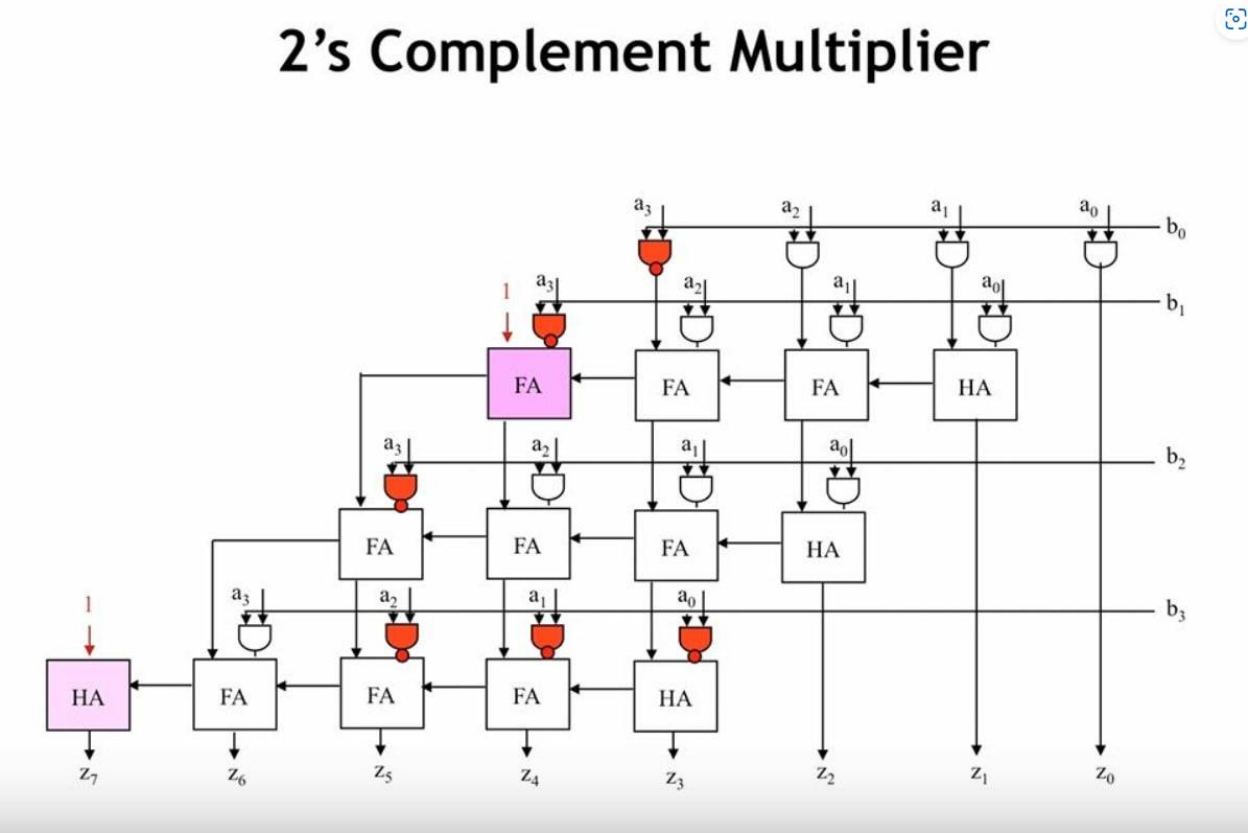
1.1. Adder: we have used a 5 bit Ripple Carry Adder



1.1.1. FA: we have used this formation of FA using XOR and AND and OR gates



1.2. Multiplier:

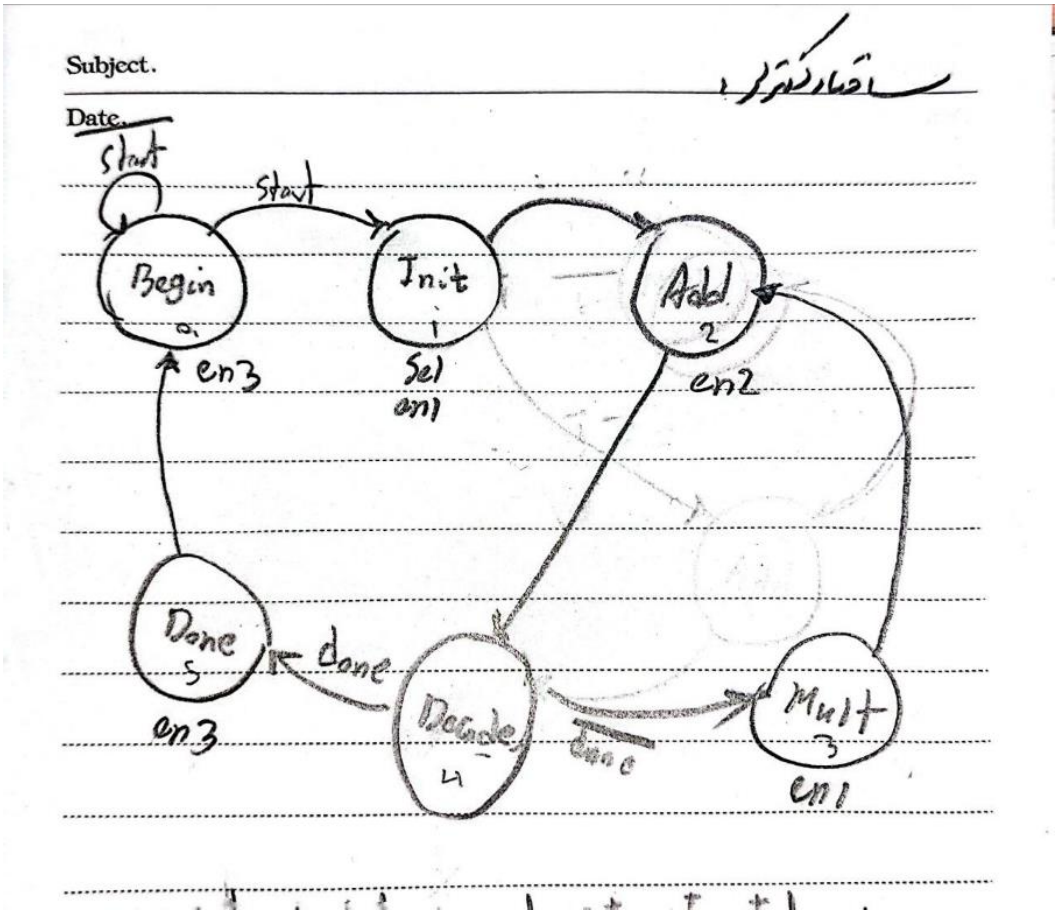


1.3. Decoder: First, we define an adder module to convert a 5-bit number to a 1-bit zero or one. Then we convert each number to a value of zero or one. Then, with some thought (a better way is to draw the Karnaugh map, which is omitted here for simplicity), we arrive at the following equation.

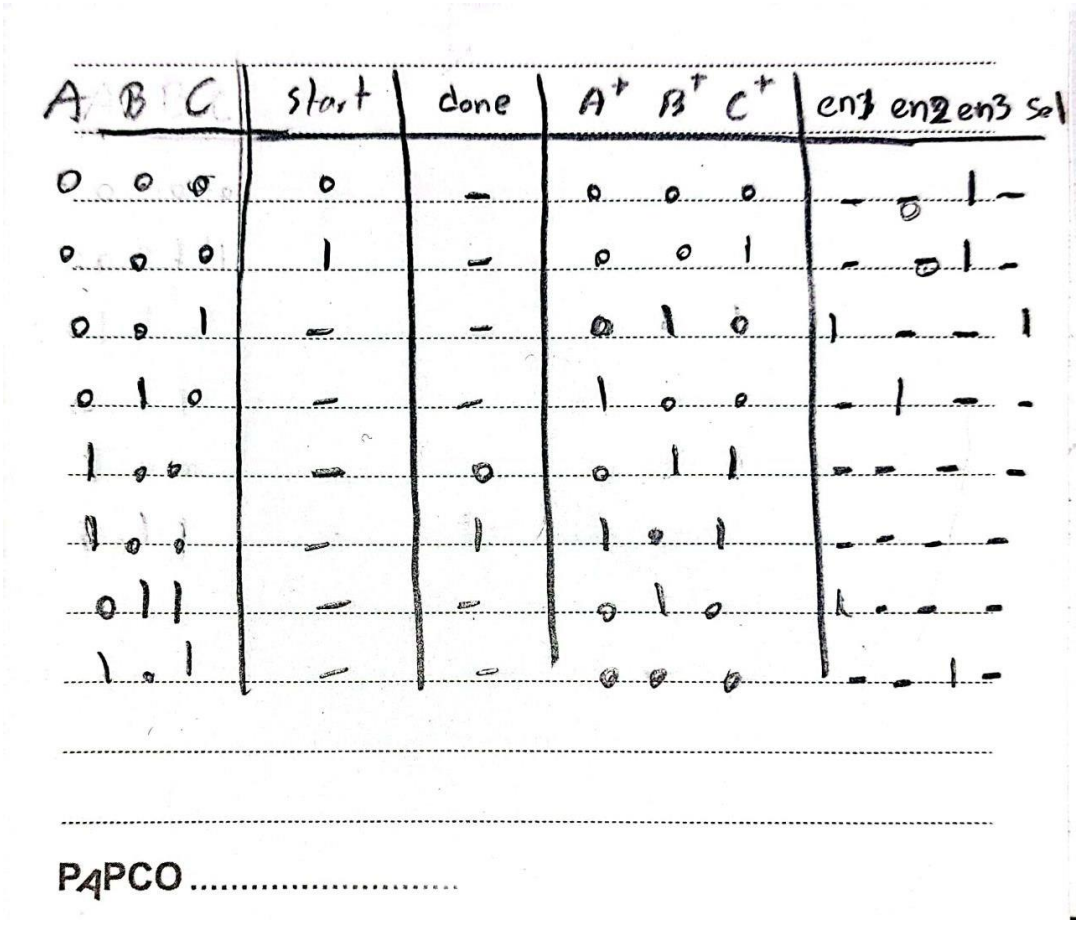
done = A1A2A3A4' + A1A2A3'A4 + A1A2'A3A4 + A1'A2A3A4

idx = {A1A2 , A1A3}

2. Controller:



2.1. Transition table:



A B C	start	done	A^+ B^+ C^+	en1 en2 en3 sel
0 0 0	0	-	0 0 0	- 0 1 -
0 0 0	1	-	0 0 1	- 0 1 -
0 0 1	-	-	0 1 0	1 - - 1
0 1 0	-	-	1 0 0	- 1 - -
1 0 0	-	0	0 1 1	- - - -
1 0 0	-	1	1 0 1	- - - -
0 1 1	-	-	0 1 0	1 - - -
1 0 1	-	-	0 0 0	- - 1 -

P4PCO .....

2.2. Boolean algebra:

Subject.

Date.

$A^+ = \bar{A}B\bar{C} + A\bar{B}\bar{C}$ Done

$B^+ = \bar{A}C + A\bar{B}\bar{C}$ $\overline{Done}$

$C^+ = \bar{B}\bar{C}$ start $+ A\bar{B}\bar{C}$.

$en1 = \bar{A}C$

$en2 = \bar{A}B\bar{C}$

$en3 = \bar{A}\bar{B}\bar{C}$

$sel = \bar{A}\bar{B}C$

P4PCO .....