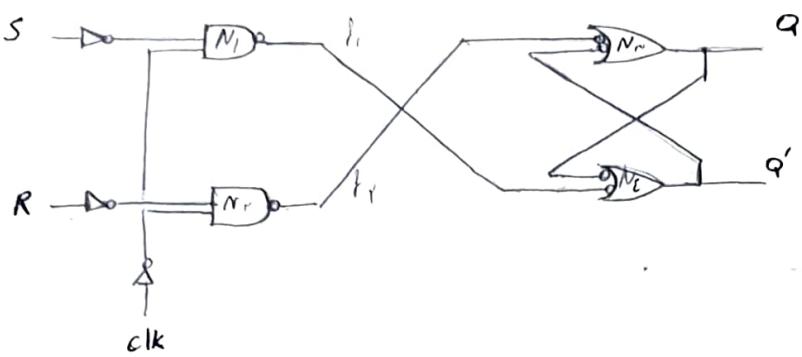
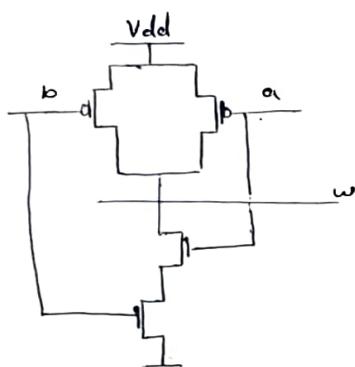


1. SRLatch



clk	S	R	Q'
1	-	-	Q
0	0	0	Q
0	0	1	1
0	1	0	0
0	1	1	-

X



$$\begin{aligned} \text{PMOS} &= 6 \text{ ns} \\ \text{NMOS} &= 4 \text{ ns} \end{aligned} \quad \left. \begin{array}{l} \text{to 1 delay} = 8 \text{ ns} \\ \text{to 0 delay} = 8 \text{ ns} \end{array} \right\}$$

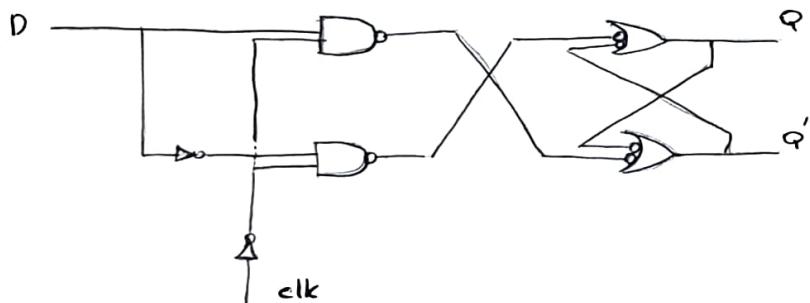


Inverter!

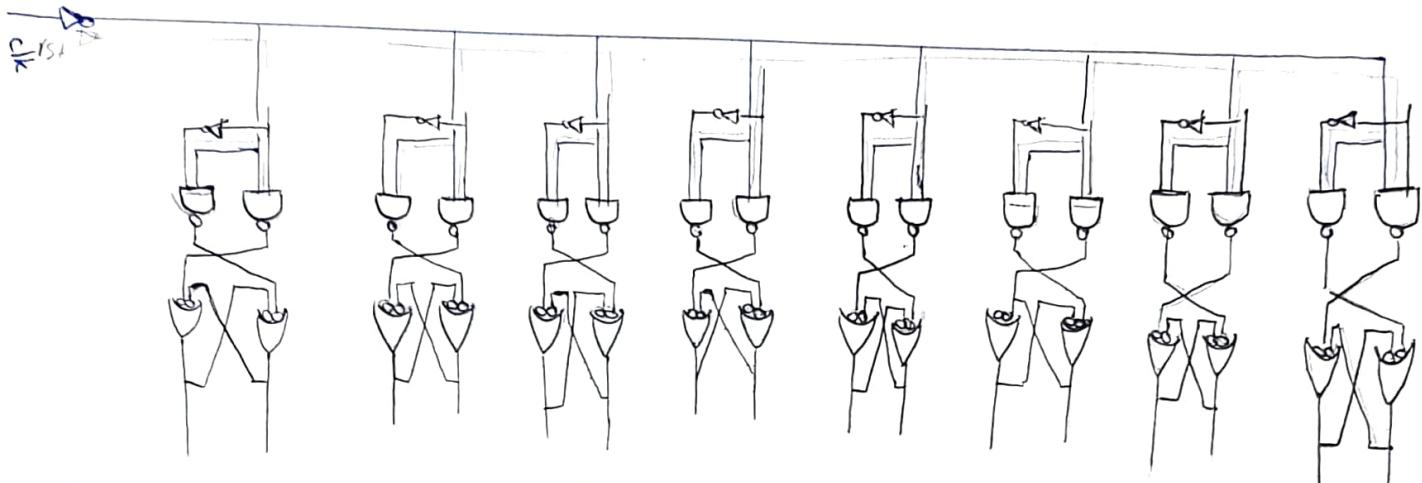
$$\begin{aligned} \text{with all Nands} \quad \left. \begin{array}{l} \text{to 0 delay} : 8 + 8 + 8 = 24 \text{ ns} \\ \text{to 1 delay} : 8 + 8 + 8 + 8 = 32 \text{ ns} \end{array} \right\} \end{aligned}$$

1. SRL-TB

1. DL 2

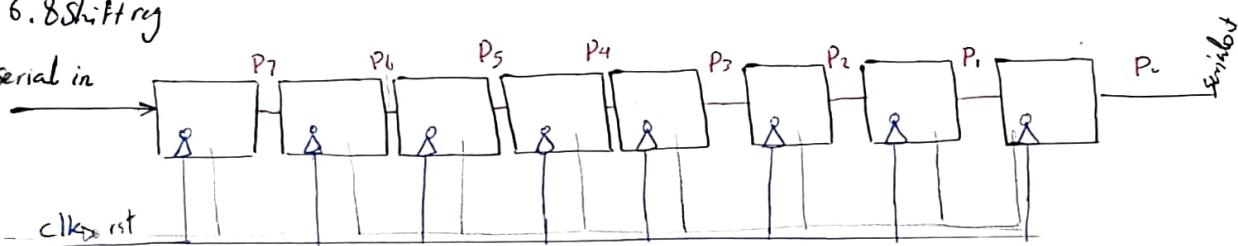


5. 8 Register



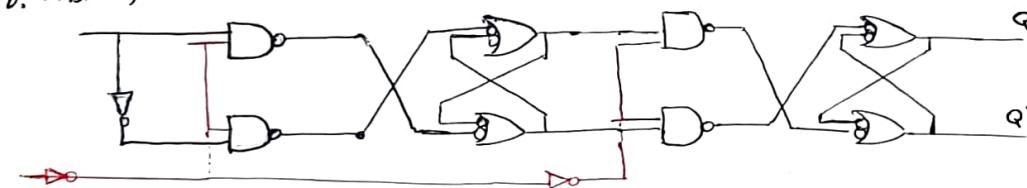
inputs are parallel-in $[7:\phi]$, outputs are parallel-out $[7:\phi]$

6. 8 Shift reg

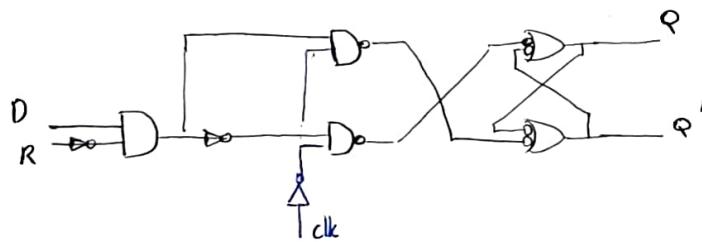


7. Shift Reg - TB

8. MSDFD, T-B



9. DL

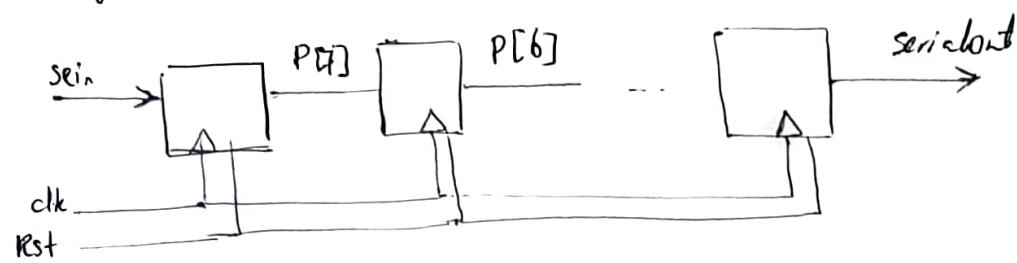


10. SR-MSDFF (shift)

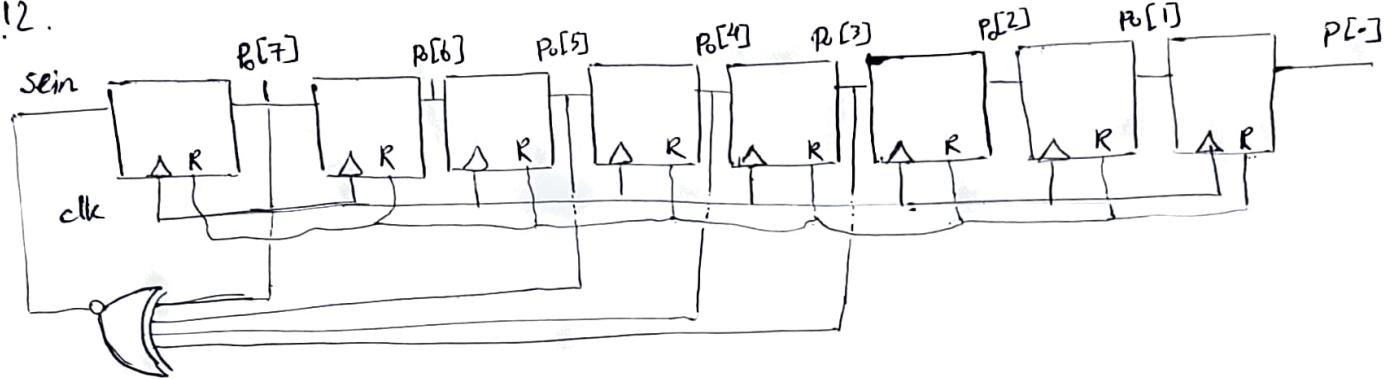
11. SR-MSDFF - TB

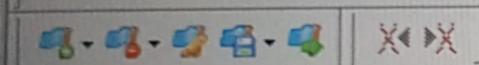
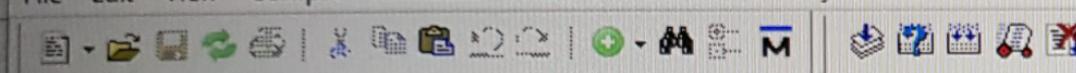
12. Reg 8 always

10. just like 6, but we have Flip Flop!



11.





Name	Status	Type	Order	Modified
SR-MSDFF-TB.v	✓	Verilog	14	01/08/2023 06:34:46 ...
SRL.v	✓	Verilog	11	01/06/2023 03:09:32 ...
SR-MSDFF.v	✓	Verilog	13	01/08/2023 06:37:52 ...
DL2.v	✓	Verilog	4	01/07/2023 06:22:10 ...
DL-TB.v	✓	Verilog	5	01/07/2023 06:15:04 ...
MSDFF-TB.v	✓	Verilog	9	01/07/2023 06:29:56 ...
SRL-TB.v	✓	Verilog	12	01/06/2023 03:10:14 ...
8Reg-always.v	✓	Verilog	0	01/08/2023 07:39:44 ...
8Register.v	✓	Verilog	1	01/07/2023 06:15:30 ...
LFSR.v	✓	Verilog	6	01/08/2023 07:58:42 ...
ShiftReg-TB.v	✓	Verilog	10	01/08/2023 12:46:12 ...
DL.v	✓	Verilog	3	01/07/2023 06:17:00 ...
MSDFF.v	✓	Verilog	8	01/07/2023 06:27:24 ...
8Shift-Reg.v	✓	Verilog	2	01/08/2023 12:46:44 ...
LFSR-TB.v	✓	Verilog	7	01/08/2023 07:53:40 ...

D:/SHAHZAD/00UT/sem3/Logic Circuits/proj4/DL2.v

```

Ln#           1   module DLatch2(input D,Clk,output Q);
                  wire dbar,s,r,clk_bar,Qbar;
                  not I1(clk_bar,Clk);
                  not I2(dbar,D);
                  nand N1(s,dbar,clk_bar);
                  nand N2(r,D,clk_bar);
                  nand N3(Qbar,Q,s);
                  nand N4(Q,Qbar,r);
endmodule

```

10

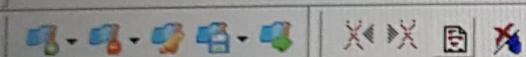
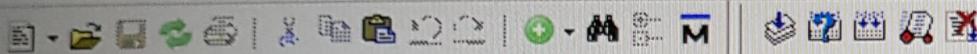
.v 8Shift-Reg.v 8Reg-always.v SR-MSDFF.v DL-TB.v SRegister.v MSDFF-TB.v

Project D:/SHAHZAD/0001/sem3/Logic Circuits/proj4/proj4

Name	Status	Type	Order	Modified
SR-MSDFF-TB.v	✓	Verilog	14	01/08/2023 06:34:46 ...
SRL.v	✓	Verilog	11	01/06/2023 03:09:32 ...
SR-MSDFF.v	✓	Verilog	13	01/08/2023 06:37:52 ...
DL2.v	✓	Verilog	4	01/07/2023 06:22:10 ...
DL-TB.v	✓	Verilog	5	01/07/2023 06:15:04 ...
MSDFF-TB.v	✓	Verilog	9	01/07/2023 06:29:56 ...
SRL-TB.v	✓	Verilog	12	01/06/2023 03:10:14 ...
8Reg-always.v	✓	Verilog	0	01/08/2023 07:39:44 ...
8Register.v	✓	Verilog	1	01/07/2023 06:15:30 ...
LFSR.v	✓	Verilog	6	01/08/2023 07:58:42 ...
ShiftReg-TB.v	✓	Verilog	10	01/08/2023 12:46:12 ...
DL.v	✓	Verilog	3	01/07/2023 06:17:00 ...
MSDFF.v	✓	Verilog	8	01/07/2023 06:27:24 ...
8Shift-Reg.v	✓	Verilog	2	01/08/2023 12:46:44 ...
LFSR-TB.v	✓	Verilog	7	01/08/2023 07:53:40 ...

D:/SHAHZAD/0001/sem3/Logic Circuits/proj4/SRL.v - Default

Ln#	
1	module SRLatch(<input type="text"/> S,R,Clk, <output type="text"></output> Q,Qbar);
2	wire s,r,clk_bar;
3	not I1(clk_bar,Clk);
4	nand N1(s,S,clk_bar);
5	nand N2(r,R,clk_bar);
6	nand N3(Qbar,Q,s);
7	nand N4(Q,Qbar,r);
8	endmodule
9	



Project - D:/SHAHZAD/00UT/sem3/Logic Circuits/proj4/proj4

D:/SHAHZAD/00UT/sem3/Logic Circuits/proj4/SR-MSDFF.v - Default

Name Status Type Order Modified

SR-MSDFF-TB.v	✓	Verilog	14	01/08/2023 06:34:46 ...
SRL.v	✓	Verilog	11	01/06/2023 03:09:32 ...
SR-MSDFF.v	✓	Verilog	13	01/08/2023 06:37:52 ...
DL2.v	✓	Verilog	4	01/07/2023 06:22:10 ...
DL-TB.v	✓	Verilog	5	01/07/2023 06:15:04 ...
MSDFF-TB.v	✓	Verilog	9	01/07/2023 06:29:56 ...
SRL-TB.v	✓	Verilog	12	01/06/2023 03:10:14 ...
8Reg-always.v	✓	Verilog	0	01/08/2023 07:39:44 ...
8Register.v	✓	Verilog	1	01/07/2023 06:15:30 ...
LFSR.v	✓	Verilog	6	01/08/2023 07:58:42 ...
ShiftReg-TB.v	✓	Verilog	10	01/08/2023 12:46:12 ...
DL.v	✓	Verilog	3	01/07/2023 06:17:00 ...
MSDFF.v	✓	Verilog	8	01/07/2023 06:27:24 ...
8Shift-Reg.v	✓	Verilog	2	01/08/2023 12:46:44 ...
LFSR-TB.v	✓	Verilog	7	01/08/2023 07:53:40 ...

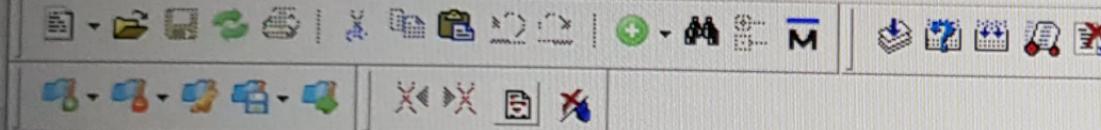
```
1 module SR_MSDFF(input clk,rst,sil,output [7:0]po,output sor);
2   wire [8:0]pol;
3   genvar i;
4   generate
5     for(i=8 ; i>0 ; i=i-1) begin
6       MSDFF DD(pol[i],clk, pol[i-1]);
7     end
8   endgenerate
9   assign pol[8]=sil;
10  assign po = rst ? 8'b0 : pol[7:0] ;
11  assign sor=rst ? 1'b0: pol[0];
12 endmodule
13
```

.v 8Shift-Reg.v 8Reg-always.v SR-MSDFF.v DL-TB.v 8Register.v MSDFF-TB.v

D:/SHAHZAD/00UT/sem3/Logic Circuits/proj4/SR-MSDFF-TB.v

Ln#

1 timescale 1ns/1ns



Project - D:/SHAHZAD/00UT/sem3/Logic Circuits/proj4/proj4

Name	Status	Type	Order	Modified
SR-MSDFF-TB.v	✓	Verilog	14	01/08/2023 06:34:46 ...
SRL.v	✓	Verilog	11	01/06/2023 03:09:32 ...
SR-MSDFF.v	✓	Verilog	13	01/08/2023 06:37:52 ...
DL2.v	✓	Verilog	4	01/07/2023 06:22:10 ...
DL-TB.v	✓	Verilog	5	01/07/2023 06:15:04 ...
MSDFF-TB.v	✓	Verilog	9	01/07/2023 06:29:56 ...
SRL-TB.v	✓	Verilog	12	01/06/2023 03:10:14 ...
8Reg-always.v	✓	Verilog	0	01/08/2023 07:39:44 ...
8Register.v	✓	Verilog	1	01/07/2023 06:15:30 ...
LFSR.v	✓	Verilog	6	01/08/2023 07:58:42 ...
ShiftReg-TB.v	✓	Verilog	10	01/08/2023 12:46:12 ...
DL.v	✓	Verilog	3	01/07/2023 06:17:00 ...
MSDFF.v	✓	Verilog	8	01/07/2023 06:27:24 ...
8Shift-Reg.v	✓	Verilog	2	01/08/2023 12:46:44 ...
LFSR-TB.v	✓	Verilog	7	01/08/2023 07:53:40 ...

D:/SHAHZAD/00UT/sem3/Logic Circuits/proj4/DL2.v - Default

```

Ln#           1  module DLatch2(input D,Clk,output Q);
              2      wire dbar,s,r,clk_bar,Qbar;
              3      not I1(clk_bar,Clk);
              4      not I2(dbar,D);
              5      nand N1(s,dbar,clk_bar);
              6      nand N2(r,D,clk_bar);
              7      nand N3(Qbar,Q,s);
              8      nand N4(Q,Qbar,r);
              9  endmodule
             10

```

Project - D:/SHAHZAD/00UT/sem3/Logic Circuits/proj4/proj4

Name	Status	Type	Order	Modified
SR-MSdff-TB.v	✓	Verilog	14	01/08/2023 06:34:46 ...
SRL.v	✓	Verilog	11	01/06/2023 03:09:32 ...
SR-MSdff.v	✓	Verilog	13	01/08/2023 06:37:52 ...
DL2.v	✓	Verilog	4	01/07/2023 06:22:10 ...
DL-TB.v	✓	Verilog	5	01/07/2023 06:15:04 ...
MSdff-TB.v	✓	Verilog	9	01/07/2023 06:29:56 ...
SRL-TB.v	✓	Verilog	12	01/06/2023 03:10:14 ...
8Reg-always.v	✓	Verilog	0	01/08/2023 07:39:44 ...
8Register.v	✓	Verilog	1	01/07/2023 06:15:30 ...
LFSR.v	✓	Verilog	6	01/08/2023 07:58:42 ...
ShiftReg-TB.v	✓	Verilog	10	01/08/2023 12:46:12 ...
DL.v	✓	Verilog	3	01/07/2023 06:17:00 ...
MSdff.v	✓	Verilog	8	01/07/2023 06:27:24 ...
8Shift-Reg.v	✓	Verilog	2	01/08/2023 12:46:44 ...
LFSR-TB.v	✓	Verilog	7	01/08/2023 07:53:40 ...

D:/SHAHZAD/00UT/sem3/Logic Circuits/proj4/DL2.v - Default

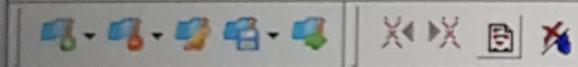
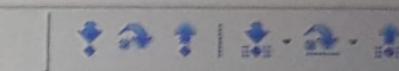
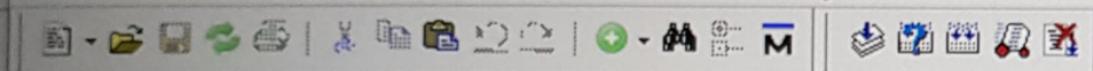
```

Ln# | 1 module DLatch2(input D,Clk,output Q);
      | 2     wire dbar,s,r,clk_bar,Qbar;
      | 3     not I1(clk_bar,Clk);
      | 4     not I2(dbar,D);
      | 5     nand N1(s,dbar,clk_bar);
      | 6     nand N2(r,D,clk_bar);
      | 7     nand N3(Qbar,Q,s);
      | 8     nand N4(Q,Qbar,r);
      | 9   endmodule
      | 10

```

F.v 8Shift-Reg.v 8Reg-always.v SR-MSdff.v DL-TB.v 8Register.v MSDdff-TB.v

D:/SHAHZAD/00UT/sem3/Logic Circuits/proj4/SR-MSdff-TB.v



Project - D:/SHAHZAD/00UT/sem3/Logic Circuits/proj4/proj4



Name	Status	Type	Order	Modified
SR-MSDFF-TB.v	✓	Verilog	14	01/08/2023 06:34:46 ...
SRL.v	✓	Verilog	11	01/06/2023 03:09:32 ...
SR-MSDFF.v	✓	Verilog	13	01/08/2023 06:37:52 ...
DL2.v	✓	Verilog	4	01/07/2023 06:22:10 ...
DL-TB.v	✓	Verilog	5	01/07/2023 06:15:04 ...
MSDFF-TB.v	✓	Verilog	9	01/07/2023 06:29:56 ...
SRL-TB.v	✓	Verilog	12	01/06/2023 03:10:14 ...
8Reg-always.v	✓	Verilog	0	01/08/2023 07:39:44 ...
8Register.v	✓	Verilog	1	01/07/2023 06:15:30 ...
LFSR.v	✓	Verilog	6	01/08/2023 07:58:42 ...
ShiftReg-TB.v	✓	Verilog	10	01/08/2023 12:46:12 ...
DL.v	✓	Verilog	3	01/07/2023 06:17:00 ...
MSDFF.v	✓	Verilog	8	01/07/2023 06:27:24 ...
8Shift-Reg.v	✓	Verilog	2	01/08/2023 12:46:44 ...
LFSR-TB.v	✓	Verilog	7	01/08/2023 07:53:40 ...

D:/SHAHZAD/00UT/sem3/Logic Circuits/proj4/MSDFF-TB.v - Default

Ln#

```

1 `timescale 1ns/1ns
2 module MSDFF_Tb();
3   reg d=1,c=1;
4   wire q;
5   MSDFF DLL(d,c,q);
6   initial begin
7     #100 d=0;
8     c=0;
9     #100 c=1;
10    #100 d=1;
11    c=0;
12    #100 d=0;
13    c=1;
14    #100 c=0;
15    #100 d=1;
16    c=1;
17    #100 d=0;
18    c=0;
19    #100 c=1;

```



Project - D:/SHAHZAD/00UT/sem3/Logic Circuits/proj4/proj4

Name	Status	Type	Order	Modified
SR-MSDFF-TB.v	✓	Verilog	14	01/08/2023 06:34:46 ...
SRL.v	✓	Verilog	11	01/06/2023 03:09:32 ...
SR-MSDFF.v	✓	Verilog	13	01/08/2023 06:37:52 ...
DL2.v	✓	Verilog	4	01/07/2023 06:22:10 ...
DL-TB.v	✓	Verilog	5	01/07/2023 06:15:04 ...
MSDFF-TB.v	✓	Verilog	9	01/07/2023 06:29:56 ...
SRL-TB.v	✓	Verilog	12	01/06/2023 03:10:14 ...
8Reg-always.v	✓	Verilog	0	01/08/2023 07:39:44 ...
8Register.v	✓	Verilog	1	01/07/2023 06:15:30 ...
LFSR.v	✓	Verilog	6	01/08/2023 07:58:42 ...
ShiftReg-TB.v	✓	Verilog	10	01/08/2023 12:46:12 ...
DL.v	✓	Verilog	3	01/07/2023 06:17:00 ...
MSDFF.v	✓	Verilog	8	01/07/2023 06:27:24 ...
8Shift-Reg.v	✓	Verilog	2	01/08/2023 12:46:44 ...
LFSR-TB.v	✓	Verilog	7	01/08/2023 07:53:40 ...

D:/SHAHZAD/00UT/sem3/Logic Circuits/proj4/SRL-TB.v - Default

```

Ln#          timescale 1ns/1ns
1           module SRTb();
2             reg ss=1,rr=1,c=1;
3             wire q,qbar;
4             SRLatch SR1(ss,rr,c,q,qbar);
5             initial begin
6               #100 ss=0;
7               #100 c=0;
8               #100 ss=1;
9               #100 rr=0;
10              #100 c=1;
11              #100 rr=1;
12              #100 ss=0;
13              rr=0;
14              c=0;
15              #100 ss=1;
16              c=1;
17              #100 ss=0;
18              #100 rr=1;
19

```

Project D:/SHAHZAD/000UT/sem3/Logic Circuits/proj4/proj4

Name	Status	Type	Order	Modified
SR-MSDFF-TB.v	✓	Verilog	14	01/08/2023 06:34:46 ...
SRL.v	✓	Verilog	11	01/06/2023 03:09:32 ...
SR-MSDFF.v	✓	Verilog	13	01/08/2023 06:37:52 ...
DL2.v	✓	Verilog	4	01/07/2023 06:22:10 ...
DL-TB.v	✓	Verilog	5	01/07/2023 06:15:04 ...
MSDFF-TB.v	✓	Verilog	9	01/07/2023 06:29:56 ...
SRL-TB.v	✓	Verilog	12	01/06/2023 03:10:14 ...
8Reg-always.v	✓	Verilog	0	01/08/2023 07:39:44 ...
8Register.v	✓	Verilog	1	01/07/2023 06:15:30 ...
LFSR.v	✓	Verilog	6	01/08/2023 07:58:42 ...
ShiftReg-TB.v	✓	Verilog	10	01/08/2023 12:46:12 ...
DL.v	✓	Verilog	3	01/07/2023 06:17:00 ...
MSDFF.v	✓	Verilog	8	01/07/2023 06:27:24 ...
8Shift-Reg.v	✓	Verilog	2	01/08/2023 12:46:44 ...
LFSR-TB.v	✓	Verilog	7	01/08/2023 07:53:40 ...

D:/SHAHZAD/000UT/sem3/Logic Circuits/proj4/8Reg-always.v - Default

```

Ln#
1  module Reg8_always (input sin,rst,clk,output reg[7:0] Q);
2
3  always @ (posedge clk,posedge rst) begin
4      if (rst)
5          Q <= 8'b00000000;
6      else
7          Q <= {sin,Q[7:1]};
8  end
9  endmodule

```

Name	Status	Type	Order	Modified
SR-MSDFF-TB.v	✓	Verilog	14	01/08/2023 06:34:46 ...
SRL.v	✓	Verilog	11	01/06/2023 03:09:32 ...
SR-MSDFF.v	✓	Verilog	13	01/08/2023 06:37:52 ...
DL2.v	✓	Verilog	4	01/07/2023 06:22:10 ...
DL-TB.v	✓	Verilog	5	01/07/2023 06:15:04 ...
MSDFF-TB.v	✓	Verilog	9	01/07/2023 06:29:56 ...
SRL-TB.v	✓	Verilog	12	01/06/2023 03:10:14 ...
8Reg-always.v	✓	Verilog	0	01/08/2023 07:39:44 ...
8Register.v	✓	Verilog	1	01/07/2023 06:15:30 ...
LFSR.v	✓	Verilog	6	01/08/2023 07:58:42 ...
ShiftReg-TB.v	✓	Verilog	10	01/08/2023 12:46:12 ...
DL.v	✓	Verilog	3	01/07/2023 06:17:00 ...
MSDFF.v	✓	Verilog	8	01/07/2023 06:27:24 ...
8Shift-Reg.v	✓	Verilog	2	01/08/2023 12:46:44 ...
LFSR-TB.v	✓	Verilog	7	01/08/2023 07:53:40 ...

D:/SHAHZAD/0001/sem3/Logic Circuits/proj4/8Register.v - Default

```

Ln#      1 module Register(input [7:0]Pi,input clk,rst,output [7:0]Po);
          2           genvar i;
          3           generate
          4           for(i=0;i<8;i=i+1) begin: DLatches
          5               DLatch DD(Pi[i],clk,rst,Po[i]);
          6           end
          7       endgenerate
          8   endmodule
          9

```

Project - D:/SHAHZAD/00UT/sem3/Logic Circuits/proj4/proj4

Name	Status	Type	Order	Modified
SR-MSDFF-TB.v	✓	Verilog	14	01/08/2023 06:34:46 ...
SRL.v	✓	Verilog	11	01/06/2023 03:09:32 ...
SR-MSDFF.v	✓	Verilog	13	01/08/2023 06:37:52 ...
DL2.v	✓	Verilog	4	01/07/2023 06:22:10 ...
DL-TB.v	✓	Verilog	5	01/07/2023 06:15:04 ...
MSDFF-TB.v	✓	Verilog	9	01/07/2023 06:29:56 ...
SRL-TB.v	✓	Verilog	12	01/06/2023 03:10:14 ...
8Reg-always.v	✓	Verilog	0	01/08/2023 07:39:44 ...
8Register.v	✓	Verilog	1	01/07/2023 06:15:30 ...
LFSR.v	✓	Verilog	6	01/08/2023 07:58:42 ...
ShiftReg-TB.v	✓	Verilog	10	01/08/2023 12:46:12 ...
DL.v	✓	Verilog	3	01/07/2023 06:17:00 ...
MSDFF.v	✓	Verilog	8	01/07/2023 06:27:24 ...
8Shift-Reg.v	✓	Verilog	2	01/08/2023 12:46:44 ...
LFSR-TB.v	✓	Verilog	7	01/08/2023 07:53:40 ...

D:/SHAHZAD/00UT/sem3/Logic Circuits/proj4/LFSR.v - Default

```

Ln# 1 module LFSR(input clk,rst,output reg[7:0] po);
2     wire tap=~(~~(po[7]^po[5])^po[4])^po[3]);
3     Reg8_always R1(tap,rst,clk,po);
4 endmodule

```

.v 8Shift-Reg.v 8Reg-always.v SR-MSDFF.v DL-TB.v 8Register.v MSDFF-TB.v LFSR.v

D:/SHAHZAD/00UT/sem3/Logic Circuits/proj4/SR-MSDFF-TB.v

Ln#
1 timescale 1ns/1ns
2 module ShiftReg2TB();
3 reg si=1,clk=1,rst=0;
4 wire so=

Name	Status	Type	Order	Modified
SR-MSDFF-TB.v	✓	Verilog	14	01/08/2023 06:34:46 ...
SRL.v	✓	Verilog	11	01/06/2023 03:09:32 ...
SR-MSDFF.v	✓	Verilog	13	01/08/2023 06:37:52 ...
DL2.v	✓	Verilog	4	01/07/2023 06:22:10 ...
DL-TB.v	✓	Verilog	5	01/07/2023 06:15:04 ...
MSDFF-TB.v	✓	Verilog	9	01/07/2023 06:29:56 ...
SRL-TB.v	✓	Verilog	12	01/06/2023 03:10:14 ...
8Reg-always.v	✓	Verilog	0	01/08/2023 07:39:44 ...
8Register.v	✓	Verilog	1	01/07/2023 06:15:30 ...
LFSR.v	✓	Verilog	6	01/08/2023 07:58:42 ...
ShiftReg-TB.v	✓	Verilog	10	01/08/2023 12:46:12 ...
DL.v	✓	Verilog	3	01/07/2023 06:17:00 ...
MSDFF.v	✓	Verilog	8	01/07/2023 06:27:24 ...
8ShiftReg.v	✓	Verilog	2	01/08/2023 12:46:44 ...
LFSR-TB.v	✓	Verilog	7	01/08/2023 07:53:40 ...

Ln #	
1	module ShiftRegTB();
2	reg si=1,clk=0,r=0;
3	wire so;
4	wire [7:0] parout;
5	ShiftRG U1(si,clk,r,so,parout);
6	initial begin
7	#100
8	si=0;
9	#100
10	clk=1;
11	#100
12	si=1;
13	clk=0;
14	#100 si=0;
15	#100 si=1;
16	#100;
17	end
18	endmodule