UNIVERSITY OF TEHRAN

Electrical and Computer Engineering Department

ECE 367, 894 – Fall 1401

Homework 2

***Transistor Switches***

| **Name:** | **Date:** |
|---|---|
| **Username:** | |

1. Show switch level CMOS structure for a 3-input NOR gate.
2. Considering 3 NS and 5 NS for the nMOS and pMOS transistors, calculate worst case *to1* and *to0* values for NOR gate of Problem 1.
3. For the gate of Problem 2, show waveform for *abc* inputs changing from 000 to 001 to 000, and to 100.
4. Write Verilog description of gate of Problem 2.
5. Write a Verilog testbench for the gate of Problem 4 to implement waveform of Problem 4.

6. A 2-to-1 multiplexer output expression is w = ~s&a | s&b. Using gates discussed in class and using 3 and 5 NS delays for nMOS and pMOS transistors, find worst-case delay values for the multiplexer.

7. Considering three delay values for nMOS and pMOS transistors, which values are never needed in calculating delays for CMOS structures? Explain the reason.

8. We can build a 3-input NAND gate out of 2-input NAND gates and inverters. For such a structure find the best and worst case delay values, assuming 3 and 5 NS for nMOS and pMOS transistors. Explain the differences and advantages and disadvantages of this implementation of a 3-input NAND gate versus a NAND gate that is built using a CMOS structure with 6 transistors.