UNIVERSITY OF TEHRAN

Electrical and Computer Engineering Department

Digital Logic Design, ECE 367, ECE 894, Fall 1401

Homework 2-4

CMOS, Boolean, K-Maps, Hazards

Name:	**Date:**
Username:	

1. Show the switch level design of a 3-input OAI (Or-And-Invert) implemented as a complex-gate structure. Using *nmos* #(2,3,6) and *pmos* #(4,5,8), show the Verilog model of this structure. Use a minimum number of transistors. Use inverters as needed.

2. Hand-calculate the worst-case delay values for To1 and To0 for the gate structure of Problem 1. Using *and*, *or*, and *not* primitives of Verilog, write a Verilog description of the OAI gate that only considers the To1 and To0 delays calculated here.

3. Write a testbench to test Verilog modules of Problems 1 and 2 simultaneously. Instantiate both modules at the same time, apply the same inputs and have two outputs that would represent the outputs of the two structures.

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4. Minimize function $f(a,b,c)$ using Karnaugh Maps.
   $f(a,b,c) = a'.b.c + a.b.c + b'.c'$

5. Write list of minterms of the following function:
   $f(a,b,c) = a'.b + a.c + b'.c'$

6. Write all alternative minimal realizations of the function shown below:
   $f(a,b,c) = \sum_m (2, 3, 4, 5, 7)$

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7. For the given circuit, A) list all potential static hazards, B) list the logical hazards including their duration, the time they occur and input transition causing them, C) of all logical hazards, list those that are also considered as electrical hazards, and D) if the output gate drives two gates similar to its own input, then which of the logical hazards also become electrical hazard?
   $$f(a,b,c,d) = \sum_m (2, 3, 4, 6, 8, 9, 12, 13)$$

8. Minimize the following function using NOT, 2-input and 3-input NAND gates. the delays of these gates are #6, #5, and #8 NS respectively. For the given circuit, A) list all potential static hazards, B) list the logical hazards including their duration, the time they occur and input transition causing them, C) of all logical hazards, list those that are also considered as electrical hazards, and D) if the output gate drives two gates similar to its own input, then which of the logical hazards also become electrical hazard?

   $$f(a,b,c,d) = \sum_m (2, 3, 4, 6, 8, 9, 12, 13)$$