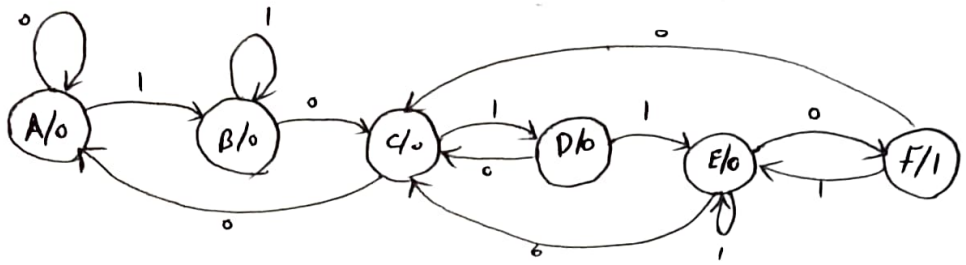
Shahzad Momayez , B10100272

MOORE

state diagram



	state	0	1	W
000	A	A	B	0
001	B	C	B	0
010	C	A	D	0
011	D	C	E	0
100	E	F	E	0
101	F	C	E	1
		state		

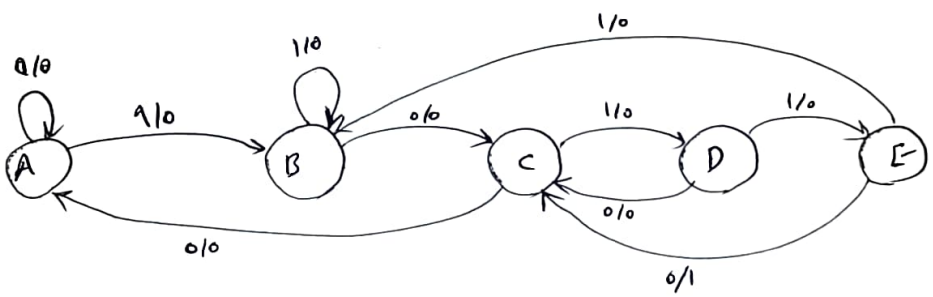
state table

PS: present state NS: next state

j : $S_{...}$

$Y_2 Y_1 Y_0$	0	1	W
000	000	001	0
001	010	010	0
010	000	011	0
011	010	100	0
100	101	100	0
101	010	100	1
	$Y_2^+ Y_1^+ Y_0^+$		

transition table



	state	0	1	W	
000	A	A	B	0	0
001	B	C	B	0	0
010	C	A	D	0	0
111	D	C	E	0	0
100	E	C	B	1	0

state table

⇒

	0	1	0	1
000	000	001	0	0
001	010	001	0	0
010	000	100	0	0
011	010	100	0	0
100	010	001	1	0
	$D_2 D_1 D_0$		W	

excitation table

C:/Users/LENOVO/Downloads/5-MooreVerilog.v - Default

```
Ln#
 1    `timescale 1ns/1ns
 2    module Moore(input clk,rst,j,output w);
 3            reg [2:0] ns,ps;
 4            always@(ps,j) begin
 5            ns=3'b000;
 6                    case(ps)
 7                            3'b000:ns=j?3'b001:3'b000;
 8                            3'b001:ns=j?3'b001:3'b010;
 9                            3'b010:ns=j?3'b011:3'b000;
10                            3'b011:ns=j?3'b100:3'b010;
11                            3'b100:ns=j?3'b001:3'b101;
12                            3'b101:ns=j?3'b011:3'b000;
13                            default:ns=3'b000;
14                    endcase
15            end
16            assign w=(ps==3'b101)?1'b1:1'b0;
17            always@(posedge clk,posedge rst) begin
18                    if(rst)
19                            ps<=3'b000;
```

SR-MSDFF.v | DL-TB.v | 8Register.v | MSDFF-TB.v | LFSR.v | LFSR-TB.v | DL.v | ShiftReg-TB.v | SRL.v | SRL-

C:/Users/LENOVO/Downloads/5-MooreTB.sv - Default

```
Ln#
 1      `timescale 1ns/1ns
 2    module MooreTB();
 3            logic clk=0,rst=0,j=0;
 4            wire w;
 5            Moore moore(clk,rst,j,w);
 6            always #5 clk = ~clk;
 7            initial begin
 8                    j = 0;
 9                    rst = 1;
10                    #30 rst = 0;
11                    #40 j = 1;
12                    #10 j = 0;
13                    #10 j = 1;
14                    #20 j = 0;
15                    #20 j = 1;
16                    #20 rst = 1;
17                    #20 j=0;
18                    #20 rst = 0;
19           $stop;
```

SR-MSDFF.v | DL-TB.v | 8Register.v | MSDFF-TB.v | LFSR.v | LFSR-TB.v