Mohammad Amanlou 810100084 Logical circuits Mr. Navabi

CA4

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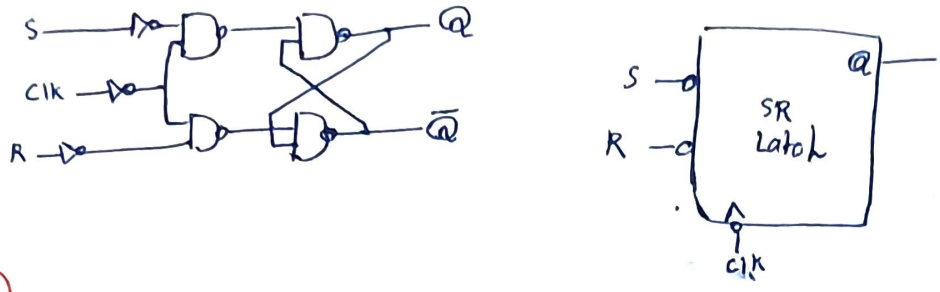
(1) SR Latch (active low)



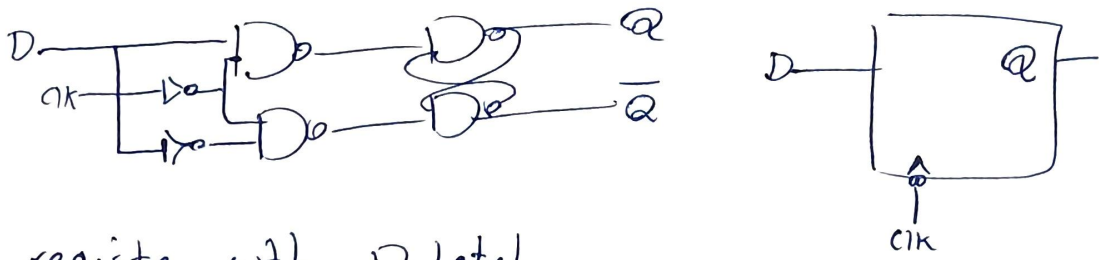
(2)

NAND → 4ns NMOS, 6ns PMOS → NAND delay = 2 * nmos delay = 2 * 4 = 8 ns

(Sw)

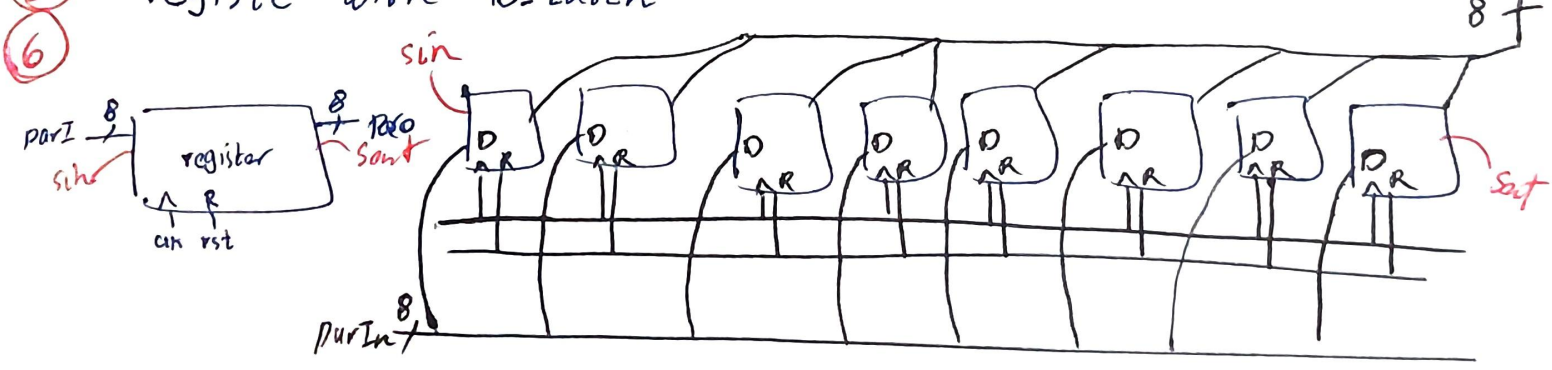
(3) simulation done (TB attached)

(4)



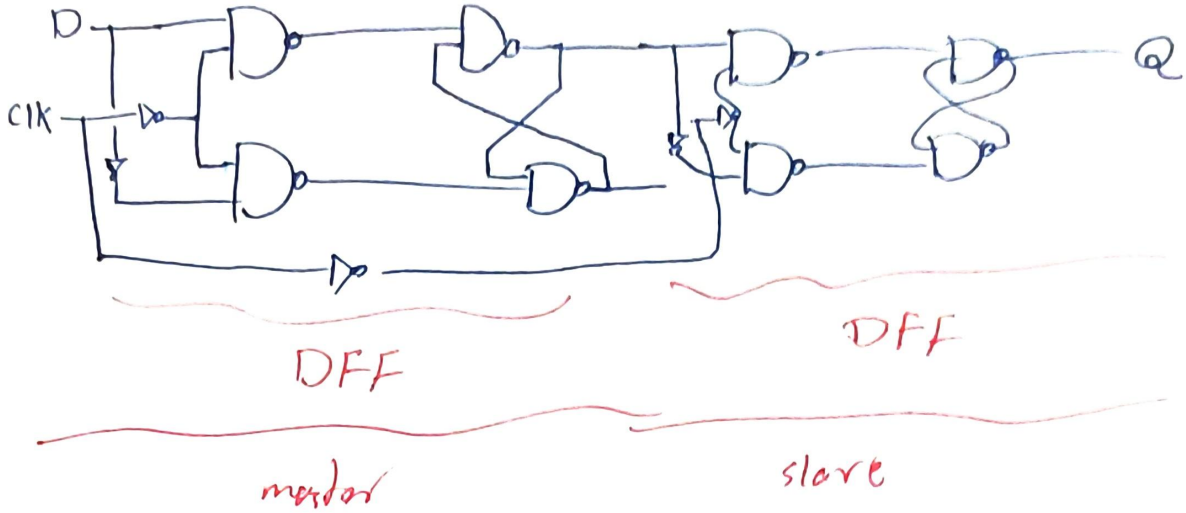
(5) registe with D-Latch

(6)



(7) it works not as expected because latches have transparency and in one clock cycle shift more than one bit number of bits depends on delay and clk time

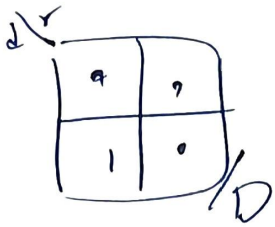
(8)

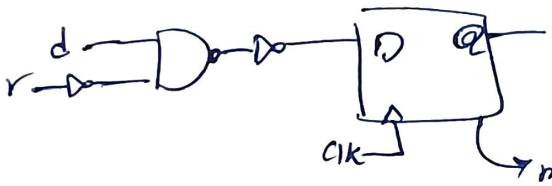


(9)

(10)

r	d	D
0	0	0
0	1	1
1	0	0
1	1	1

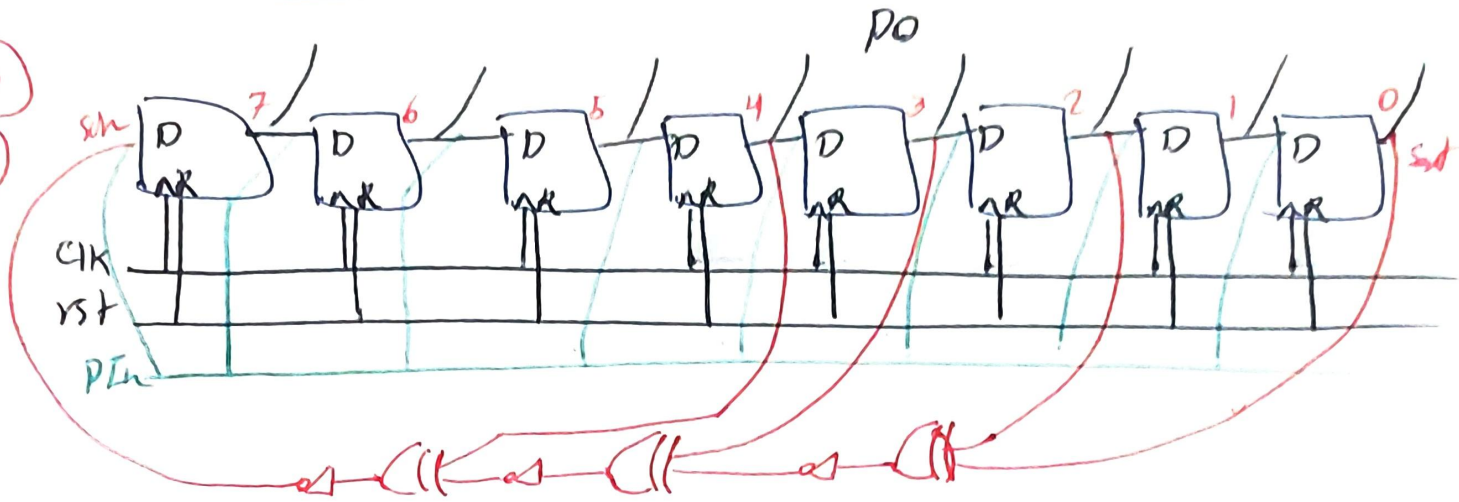




→ master slave DFF that we have seen in part 8

(11) it works as expected because we use MSDFF and it is garunteed that in every clk output just change 1 bit

(13)
(12)



8 FF → $2^8 - 1 = 255$

=> PI = 8'b10000000

each 255 clk cycle same numbers and pulses repeat

if we initialize with 8'b00000001 case 8'b00000000 doesn't happen because in xors we have 1 or in numbers we have 1