UNIVERSITY OF TEHRAN

Electrical and Computer Engineering Department

Digital Logic Design, ECE 367, ECE 894, Fall 1401

Homework 1

Logic Minimization, Karnaugh Maps

Name:	**Date:**
Username:	

1. Minimize the following function using 4-variable Karnaugh Maps.

   $f(a, b, c, d) = \Sigma_m(0, 2, 4, 6, 12, 15)$

2. Minimize the following function using 4-variable Karnaugh Maps.

   $f(a, b, c, d) = \Sigma_m(0, 1, 3, 4, 5, 6, 7, 9) + d(8, 10, 14)$

3. Show minimal realization of function $f(a, b, c, d) = \Pi_M(5, 7, 8, 9, 10, 12) + d(1, 4, 6)$ using 2- or 3-input NOR gates. Write all possible alternative implementation of this function.

4. Write Verilog gate level implementation of function of Problem 3. Use #(5,6) for gate delay, and include these parameters for instantiation of Verilog primitives. Arrange gates for a lowest worst case delay, and calculate this delay. Find the input transition that yields the worst-case delay of the circuit.

5. Write Verilog gate level implementation of function of Problem 3. Use assign statement and calculate the worst-case delay from gate level implementation of this circuit from Problem 4.

6. Show minimal realization of $f(a, b, c, d) = \Sigma_m(0, 1, 3, 4, 5, 6, 10) + d(9, 12, 15)$ using 2- and 3-input NAND gates. Arrange gates for the lowest worst-case delay.