12/5/24

Labs sessions for VSD workshop

Linux commands in Terminal

1) ↳ cd Desktop.
2) ↳ cd work/tools/
3) ↳ ls -ltr
   // all the related files gets opened, listed

↳ ls --help
   list all the switches
↳ clear → Clears

4 ↳ cd openlane_working_dir.
↳ ls -ltr // all the files in openlane are listed
↳ cd pdks
↳ ls -ltr // lists file in pdks

by skywater

Process design kits.

→ Open_PDKs
Can be compatible with Open Source EDA tools.

→ Sky-130A

Steps to invoke the tool.

(1) terminal

↳ cd Desktop
↳ cd work/tools/openlane_working_dir/openlane.
↳ docker
=) bash-4.2 $ ls -ltr
↳ ./flow.tcl -interactive

Open a new terminal

% package require openlane 0.9
% prep -design picorv32a
// prep after preparation complete

Type (2) terminal
↳ cd Desktop
↳ cd work/tools/
↳ cd Openlane_working_dir
↳ cd openlane
↳ cd design
↳ ls -ltr
↳ cd picorv32a
↳ ls -ltr
↳ cd src
↳ ls -ltr
↳ cd ../
↳ less config.tcl
Click q.
↳ less sky130A_sky130_fd_sc_hd_config.tcl.
a window gets opened
Click q

fanout 6
clock_period 24.73
core_UTIL 35

↳ cd runs
↳ ls -ltr
executed date will be displayed.

↳ the present date which was displayed
cd 12-05_08-28
↳ ls -ltr // list of files will be opened
↳ cd tmp
↳ ls -ltr → list of files
↳ less merged.lef
Press 'q'

↳ cd ../
↳ ls -ltr // list of files
↳ cd results
↳ ls -ltr // list of files
↳ cd Synthesis
↳ ls
↳ cd ../
↳ cd reports
↳ ls -ltr
↳ cd Synthesis
↳ ls
↳ cd ../
↳ ls
↳ less config.tcl

continue

↳ cd results

→ continuation.

↳ cd results
↳ ls -ltr
↳ cd Synthesis
↳ ls -ltr
↳ less picorv32a.Synthesis.v
↳ cd ../
↳ cd ../
↳ cd reports
↳ ls -ltr
↳ cd Synthesis
↳ ls -ltr
↳ less 1-yosys_4.stat.rpt → Stats report gets displayed.
↳ less 2-Openstar.rpt

After Synthesis Steps.

→ Flop ratio

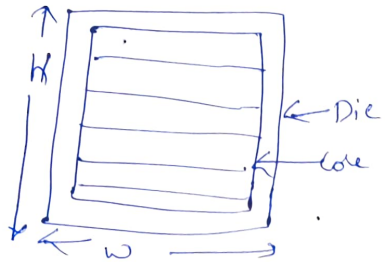
→ No of Dflip - 1613
→ No of Cells - 14876

Flop ratio → $\frac{1613}{14876} = 0.108422 \times 100$

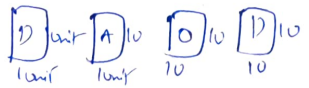
$= 10.84$

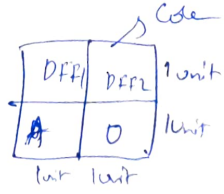
Day-2

→ Define width & height of core and die



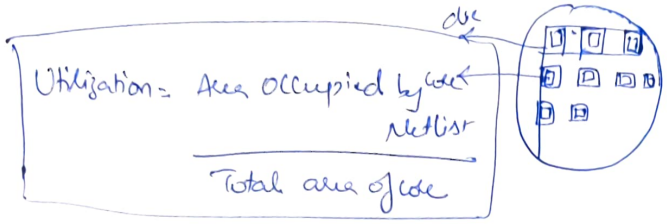
1) 

2) 



Core area = 4 Sq unit

→ If the logic cells occupies the complete area of the core → 100% Utilization



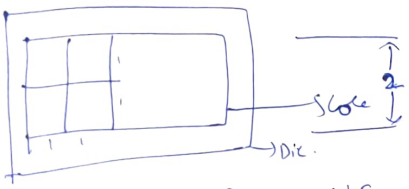
Ex-1 UF = $\frac{4 \times 1 \text{ Sq}}{2 \times 2 \text{ Sq}} = 1$.

Each cell of Net list 1 unit
4 units Net list

→ Aspect ration = $\frac{\text{hight}}{\text{width}} = \frac{2 \text{ units}}{2 \text{ units}}$ = 1.

Area occupied = No. of Net list × area of each Net list.

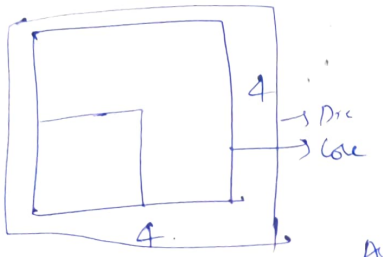
→ Ex-2



UF = $\frac{2 \times 2}{4 \times 2} = \frac{4}{8} = 0.5$

Aspect ration = $\frac{2}{4} = \frac{1}{2} = 0.5$

→



UF = $\frac{4 \text{ Sq}}{4 \times 4}$

= $\frac{4}{16} = 0.25$

As = $\frac{4}{4} = 1$.

→ Define location of preplaced cells.

→ Few ASICs implemented once but instantiated n-number of times are termed as Pre-placed cells

→ They are placed before placement & routing these are called as Pre-placed cells

→ Preplaced cells.

Day-2

Terminal - (2).

→ Steps to run floor planning. using openlane

After Synthesis is successfull.

→ Open a new terminal (3)

↳ CD Desktop
↳ CD work/tools/
↳ CD openlane_working_dir
↳ CD openlane
↳ CD configuration
↳ Pwd.
↳ ls -ltr
↳ less README.md
~~Press~~ q
↳ less floorplan.tcl.

floorplan defaults

→ Vertical - 3.
Horizontal - 4.
→ Core utility - 50
Aspect ratio - 1.
Core Margin - 0.

→ Another Terminal (4)

↳ ~~cat~~ CD Desktop/work/tools/openlane_working_dir/
↳ Pwd openlane/designs/picorv32a
↳ ls -ltr

↳ less config.tcl → | Clock period - 5.000

→ In terminal ① after run_synthesis command
→ after run successful
↳ run_floorplan.

↳ Continue in terminal ④.

↳ cd runs
↳ ls -ltr → files with present date gets opened.
↳ cd 18-05_03-21
↳ ls -ltr
↳ less config.tcl.
↳ cd logs/floorplan/
↳ ls -ltr (list of floorplan files
↳ less 4-ioplacer.log
↳ cd ../
↳ cd ../
↳ ls -ltr
↳ less config.tcl.
↳ cd ~~logs~~ cd results/floorplan/
↳ ls -ltr
↳ less picorv32a.floorplan.def
↳ ~~bma~~.

→ continued

Def file in
unit distance Microns 1000
Die area (0 0) (660685) (671405)

Dimensions of chip in um $\frac{660685}{1000}$ = 660.685 um

→ $\frac{671405}{1000}$ = 671.405 um

Continued

↳ ~~magic -T /home/nickson/Desktop/work/tools/open openlane_working_dir/pdks/sky130A/libs.tech/magic/sky130A.tech lef read ../../~~

↳ magic -T /home/nickson/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.floorplan.def &

↳ Floorplan gets opened.

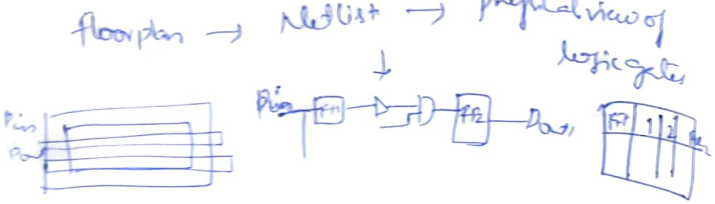
↳ In floorplan window select 's' to select the floor plan
→ select 'v' to move fit to window
→ To zoom in → left right 'z'.
→ Zoom out 'shift+z'
→ place the mouse cursor on required block and select 's'.

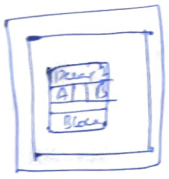
20/5/

→ 1) Bind netlist with physical cells.

→ Placement:

floorplan → Netlist → physical view of logic gates





→ Estimation of wire lengths

→ If the distance between i/p pin and blocks are too long, buffers are added in btw them.

→

Need for characterisation

→ Conversion of RTL (functionality) to Legal hardware is in the form of code termed as Logic Synthesis

→ o/p logic Synthesis is Gates.

→ next step floorplanning, we import netlist of logic synthesis outside the core and die size

→ Next step is placement

→ CTS → Clock Tree Synthesis

all the FFs should receive the clock synchronously. Zero Skew

→ Routing

→ Static Timing analysis 1) hold time
2) Slack time
3)

Steps to run placement

↳ type run_placement in terminal (1) after run_floorplan

↳ In terminal (4)

→ OpenLane_flow/designs/picorv32a/runs/20-05_11-34/results/placement/picorv32a.placement.def.

↳ after magic -T - - - - command.

↳ Desktop/work/tools/OpenLane_working_dir/OpenLane/designs/picorv32a/runs/20_05_11-34/results/placement

↳ ls

↳ magic -T /home/nickson/Desktop/work/tools/OpenLane_working_dir/pdks/sky130A/libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.placement.def &

Placement window opens.

Steps to change I/o ~~distance~~ pins.

After the run floor plan in terminal ①.

In new terminal

↳ CD Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs

↳ ls -ltr

↳ cd 20-05_11-34/results/floorplan/

↳ ls

↳ magic -T .... picorv32a.floorplan.def &

↳

| run once again floorplan

| we could observe equidistant floor plan.

In terminal ④ after run floor plan.

~~type set ::env(FP_IO_MODE) 2~~ → This command is available in CD Desktop/work/tools/openlane_working_dir/openlane/configuration

type set ::(FP_IO_MODE) 2

↳ pwd

↳ less floorplan.tcl.

Then again run floorplan. and run magic -T ---

// we can observe the floor plan has a I/o of distant 2

Cell design flow is the flow of standard cells design.

i/ps
PDKs (Process design kits):
Tech files ← DRC & LVS rules, spice models, → equations
Library & user-defined spec

↓

Design steps
Circuit design, layout design, characterization

o/p
circuit description language (CDL).
GDSII, LEF, extracted spice netlist (.cir)

New terminal ⑤. Day-3 labs.

Cloning the inverter file through github.

↳ CD Desktop/work/tools/openlane_working_dir/openlane

↳ git clone https://github.com/nickson-jose/vsdstdcelldesign.git

↳ ls -ltr

↳ cd vsdstdcelldesign

↳ ls -ltr

↳ pwd. → continued

In new terminal copy 'sky130A.tech' file to vsdstdcelldes

↳ CD Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/magic

↳ cp sky130A.tech /home/vsdusca/Desktop/workshop/openlane_working_dir/openlane/vsdstdcelldesign

↳ after pwd .... continued.

↳ ls -ltr

↳ magic -T sky130A.tech sky130_inv.mag &

[Magic window with inverter layout opens and tkcon window (logfile) gets opened.

// *

↳ ~~select on~~ place the cursor on inv layout and click 's'.

↳ Now go to tkcon window and type 'pwd'.

↳ "extract all"

↳ Now Go to terminal (5) and press type

↳ ls -ltr // New file sky130_inv.ext is observed.

⇒ In tkcon window

type ↳ ~~extract~~ ↳ ext2spice cthresh 0 rthresh 0

↳ ext2spice.

⇒ In terminal (5)

↳ ls -ltr

↳ Vim sky130_inv.ext // Spice file opens.