Name : P. Shailesh Roll no : EE20B100

I. Fill in the blanks

1. Data flow

2. It may cause short circuit (or) Burn if there are different values

3. To avoid short circuit. (or) To multiple gates with same output lines.

4. (i) Multiple FF's outputs

   (ii) READ AND WRITE ENABLE

   (iii) Read from one FF and write into another FF.

5. (i) 4 bits

   (ii) 8 bits

6. (i) MOV , LDI

   (ii) ADD

   (iii) -

7. (i) Control which operation to be performed.

   (ii) Control unit

8. 1024

9. (i) 0010 1011 1001

   (ii) 697

10. SRAM , DRAM

11. SRAM

II. Answer the following :

1. Ans. (a) A memory chip with 8 data pins means at each location it has 8 bits of data with in the chip.

So, The organisation $= \left(\frac{\text{Capacity}}{\text{No. of data pins}}\right) \times 8 = \left(\frac{512k}{8}\right) \times 8$

[$\because$ Organisation for this chip = 64k x 8] .

(b) No. of address lines $= \log_2(64 \times 2^{10}) = \log_2(2^{16}) = 16$

[$\because$ 16 Address lines] .

2. Ans : (a) Total amount of memory (bytes) = Total no. of addresses

$= 0 \times (9FFFF - 10000) + 1$

$= 0 \times (8FFFF) + 1$

Ans = 5,8 9,824 bytes

(b) Byte addressable memory means 8 bits.

Word length = 16 bits.

(c) Size of address bus = $\log_2(589824)$ = $\log_2(589824) + 1$

= 19 + 1

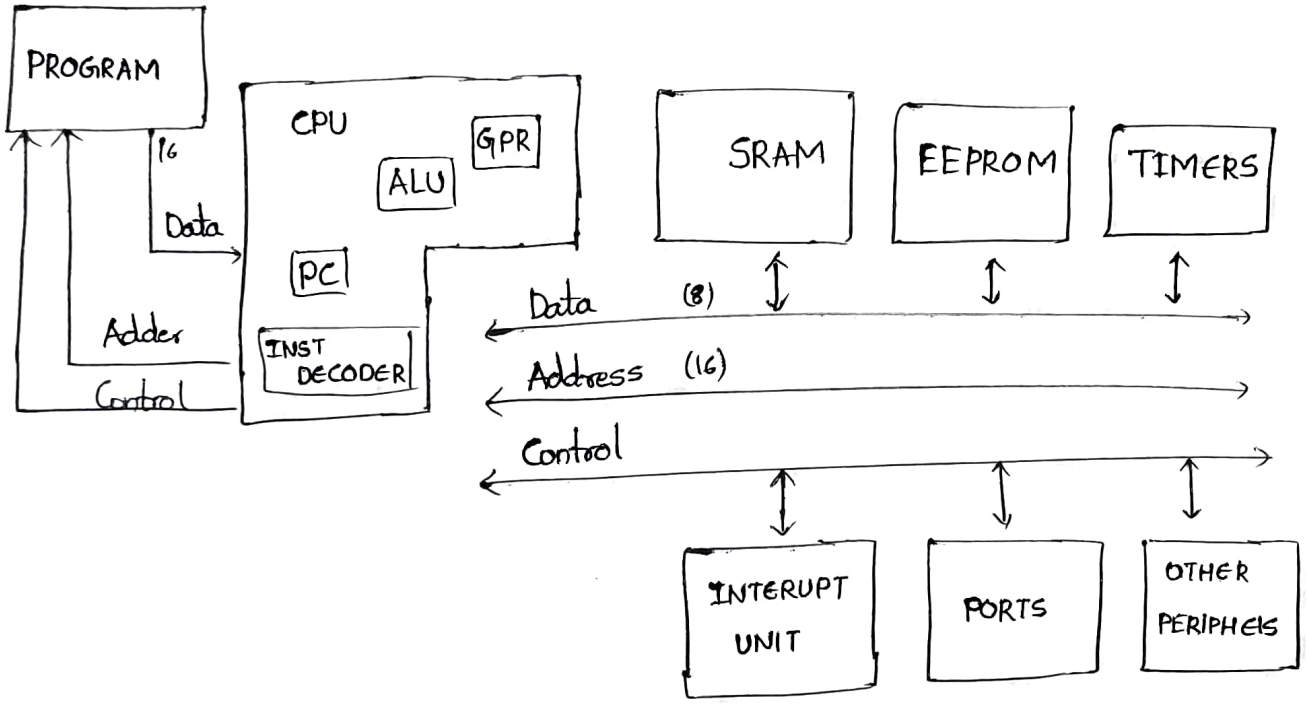
$[\cdot] = GIF$

Ans = 20 bits

(d) Size of data bus = 8 bits

3. Ans.

(a) Block diagram



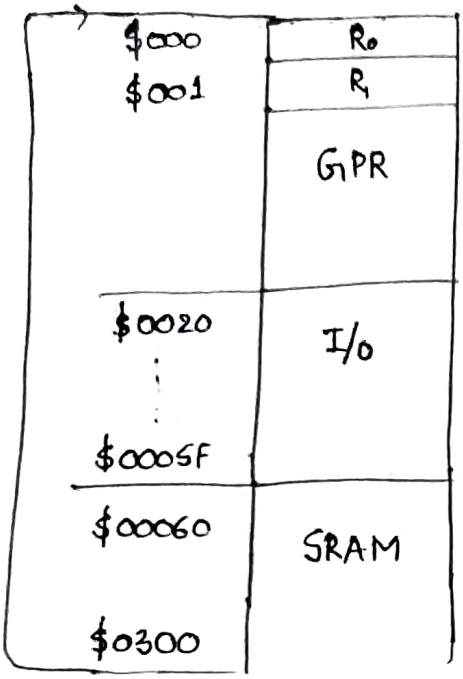
(b) Size of Data bus = 8 bits

Size of address bus = 16 bits

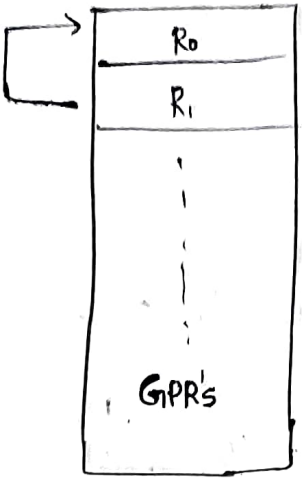
World length = 16 bits

(c) i) LDS R_0, 0x0300

ii) MOV R_0, R_1



(i)



(ii)

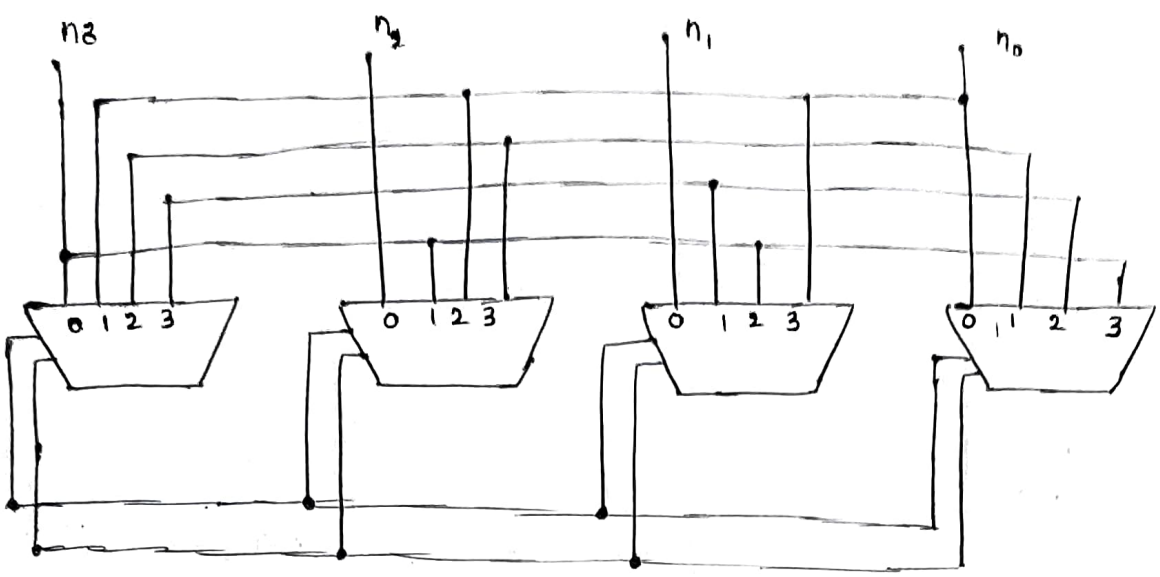
4.

Ans.

	ACTIVE - HIGH LOGIC	
S_3 S_2 S_1 S_0	LOGIC (M=1)	ARITHMETIC (M=0) (G=1)
0 0 0 1	A + B	A+B
0 1 1 0	A ⊕ B	A−B
1 0 0 1	$(A \oplus B)'$	A+B
1 1 0 0	1	A+A

$A = A_3 A_2 A_1 A_0$

$B = B_3 B_2 B_1 B_0$



S_0	S_1	Shirt
0	0	0 - shirt
0	1	1 - shirt
1	0	2 - shirt
1	1	3 - shirt

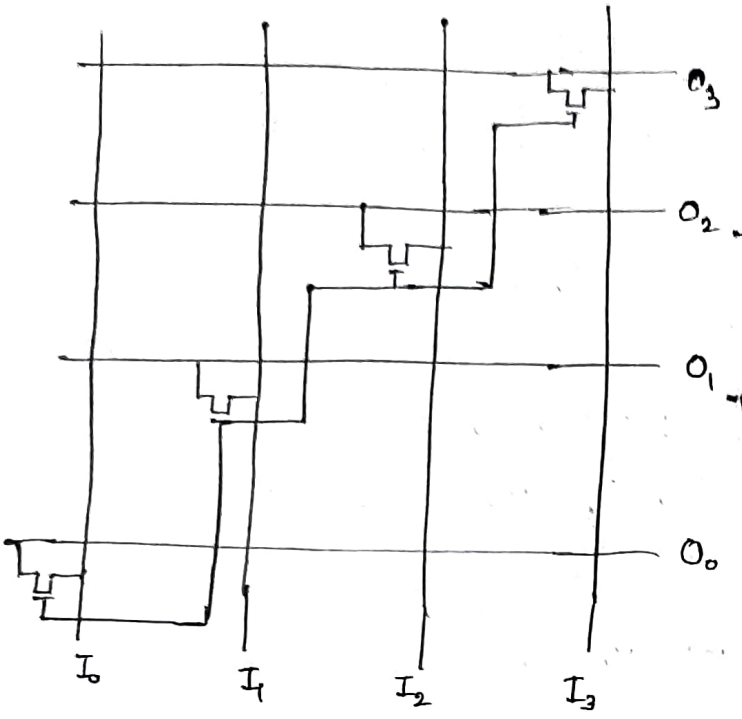
(b) The 4-bit FF takes 3-clock cycles for 3-bit shift whereas shirt takes 1-clock cycle.

5. Ans.

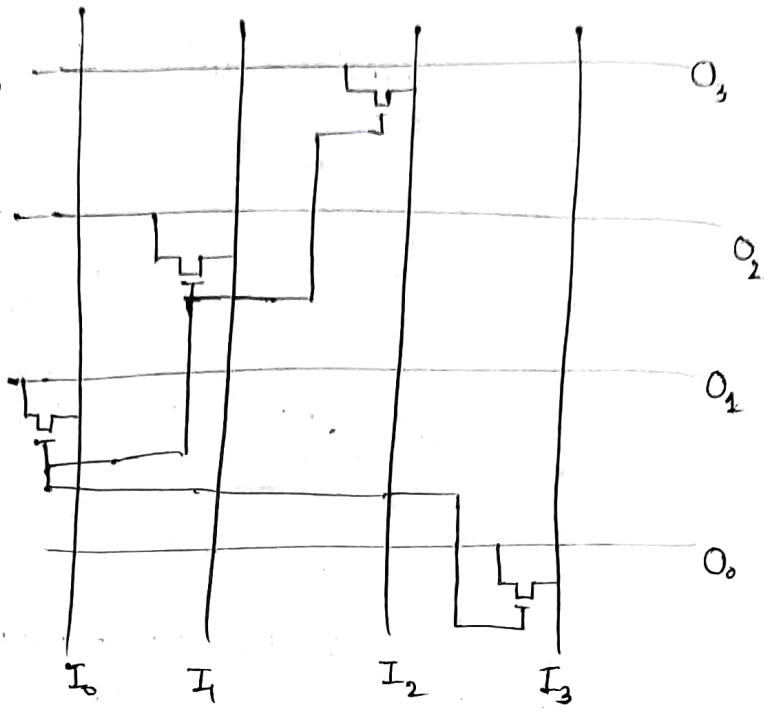
(a) 4X4 Barrel shifter

Shift	O_0	O_1	O_2	O_3
0	I_0	I_1	I_2	I_3
1	I_3	I_0	I_1	I_2
2	I_2	I_3	I_0	I_1
3	I_1	I_2	I_3	I_0

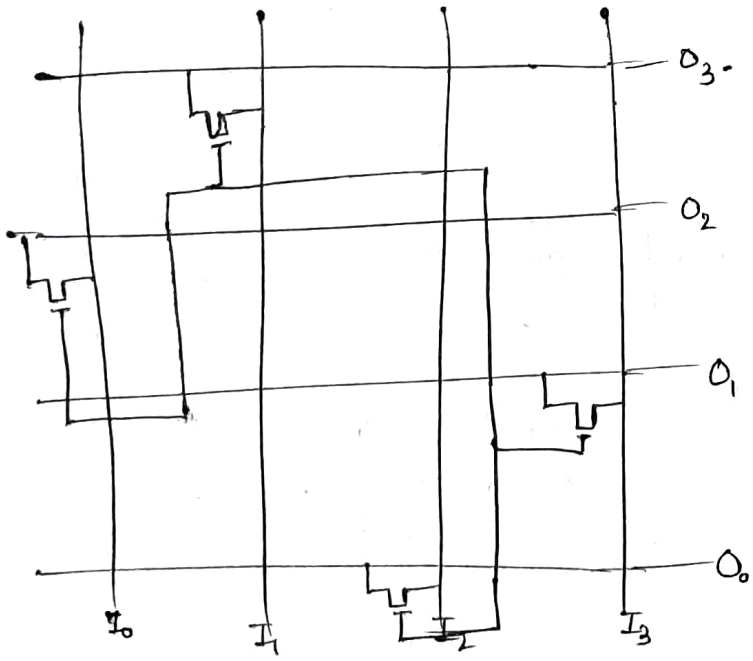
Shift zero bit :



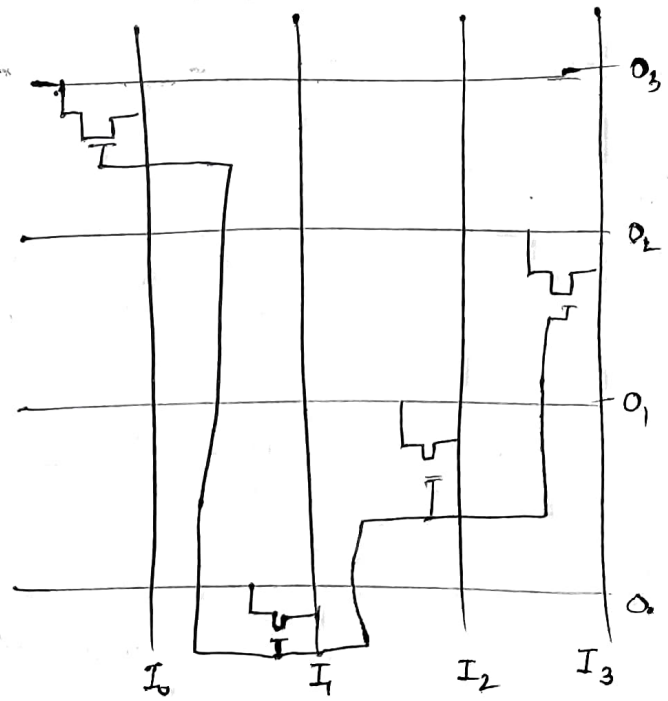
Shift 1 bit :



Shift 2 bit



Shift 3 bit



(b) A barrel shifter is able to complete the 3-bit shifter in single clock cycle, But a 4 bit FF shifter will take 3 clock cycles to shift 3-bits.

6. (a) The value of 7 points to the address of operard

Ans. 0XD3 in the array

(b) $R_0 = 0X32$; $R_1 = 0X5F$

(c) 0XD3 and 0X5F are inputs.

(d) Addition of 2 hexadecimal numbers and storing the result and carry in SRAM at address.

(e) 0X32 is stored in SRAM or address 0X60 and 0X01 is stored at 0X61.