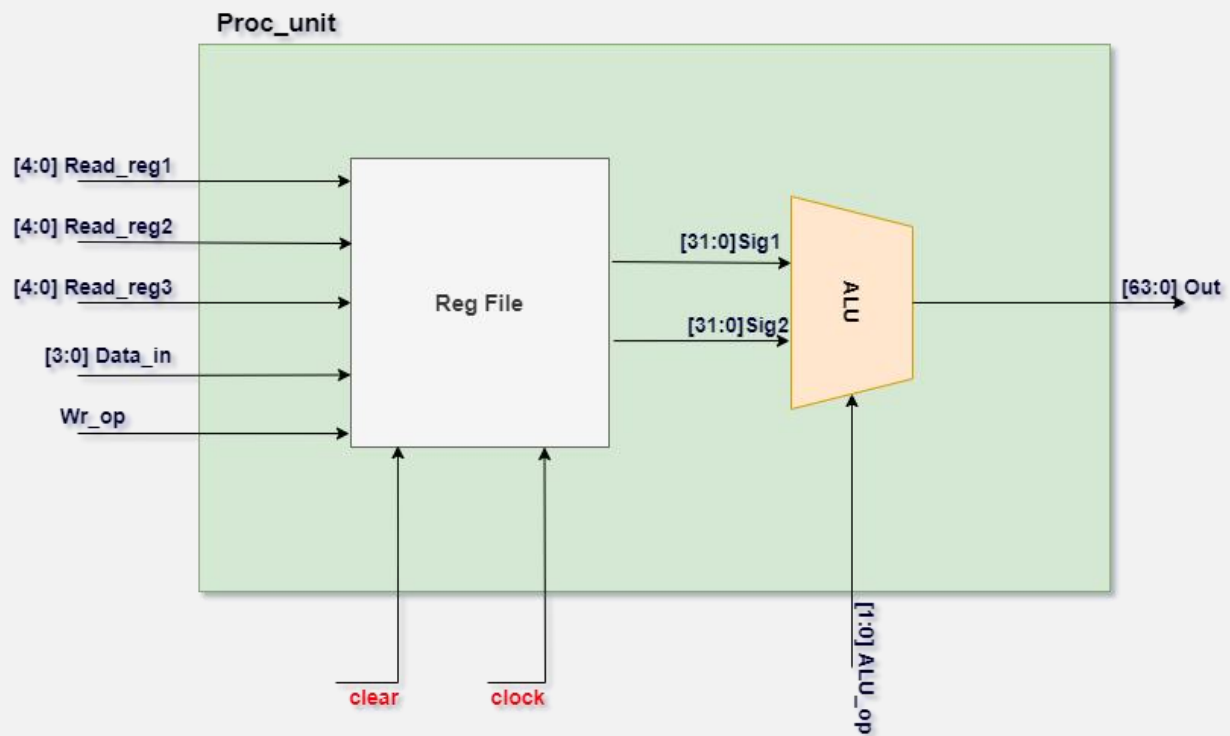


Name: Shaista Rasool Cheema

Project : Design and verify a register file integrated with ALU module.



CODE

The screenshot displays the edaplayground.com web interface. The browser address bar shows the URL `edaplayground.com/x/ZjR`. The page features a navigation bar with the 'EDA playground' logo, buttons for 'Run', 'Save', and 'Copy', and a 'KnowHow WEBINARS' banner. The main content area is divided into a left sidebar and a central code editor.

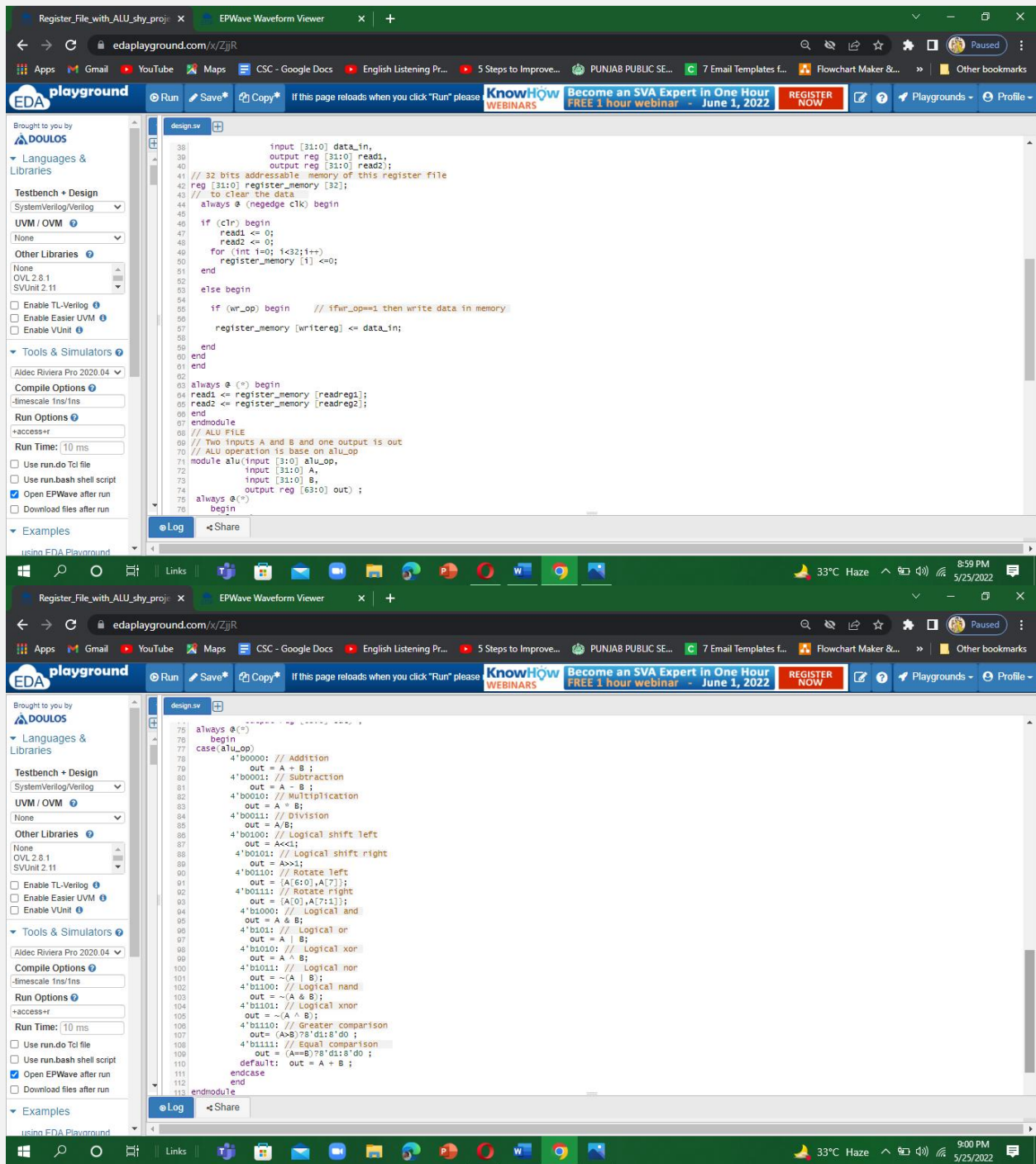
Left Sidebar:

- Testbench + Design:** Includes dropdowns for 'SystemVerilog/Verilog', 'UVM / OVM', and 'None'. It also lists 'Other Libraries' with 'None', 'OVL 2.8.1', and 'SVUnit 2.11'.
- Tools & Simulators:** Includes a dropdown for 'Aldec Riviera Pro 2020.04' and 'Compile Options' with a 'timescale 1ns/1ns' field.
- Run Options:** Includes a 'Run Time: 10 ms' field and checkboxes for 'Use run.do Tcl file', 'Use run.bash shell script', 'Open EPWave after run' (checked), and 'Download files after run'.
- Examples:** A section for additional code examples.

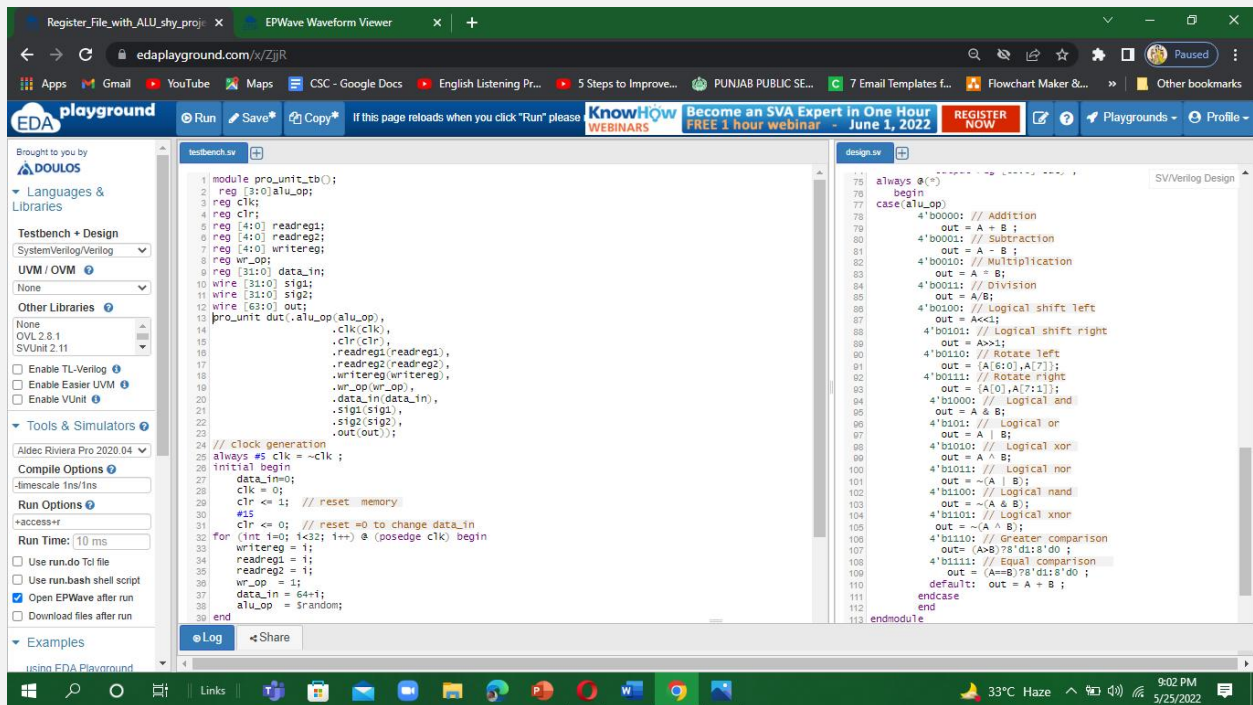
Central Code Editor:

```
1 // PROJECT: Design and verify a register file integrated with ALU module
2 ///////////////////////////////////////////////////////////////////
3 // NAME: SHAISTA RASOOL CHEHA
4 ///////////////////////////////////////////////////////////////////
5 module pro_unit(input [3:0] alu_op,
6                 input clk,
7                 input clr,
8                 input [4:0] readreg1,
9                 input [4:0] readreg2,
10                input [4:0] writereg,
11                input wr_op,
12                input [31:0] data_in,
13                output [31:0] sig1,
14                output [31:0] sig2,
15                output reg [63:0] out);
16 // Instantiation ALU File
17 alu alu_inst(.alu_op(alu_op),
18             .A(sig1),
19             .B(sig2),
20             .out(out));
21 // Instantiation of Reg File
22 register reg_inst(.clk(clk),
23                 .clr(clr),
24                 .readreg1(readreg1),
25                 .readreg2(readreg2),
26                 .writereg(writereg),
27                 .wr_op(wr_op),
28                 .data_in(data_in),
29                 .read1(sig1),
30                 .read2(sig2));
31 endmodule
32 module register(input clk,
33                input clr,
34                input [4:0] readreg1,
35                input [4:0] readreg2,
36                input [4:0] writereg,
37                input wr_op,
38                input [31:0] data_in,
39                output reg [31:0] read1,
```

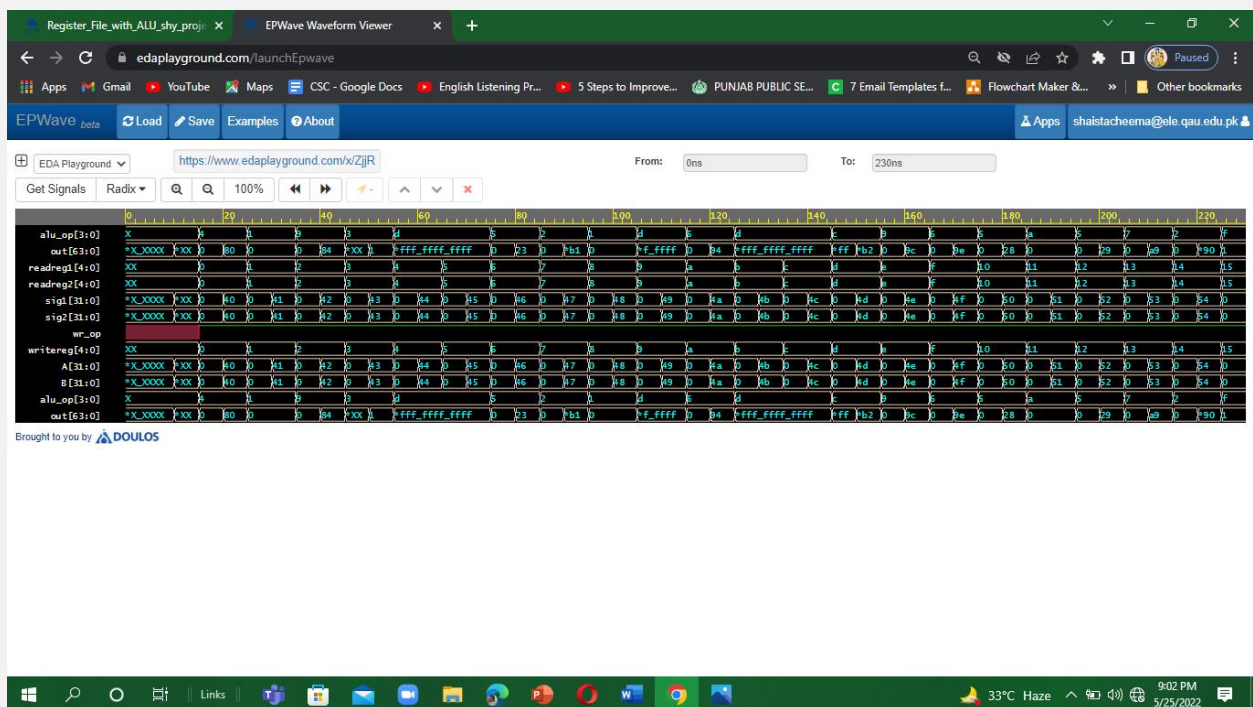
Bottom Taskbar: Shows the Windows taskbar with various application icons and a system tray indicating '40°C Haze' and the time '7:09 PM 5/25/2022'.



Testbench Code



RESULTS



<https://www.edaplayground.com/x/ZjjR>