

# Lab: 06

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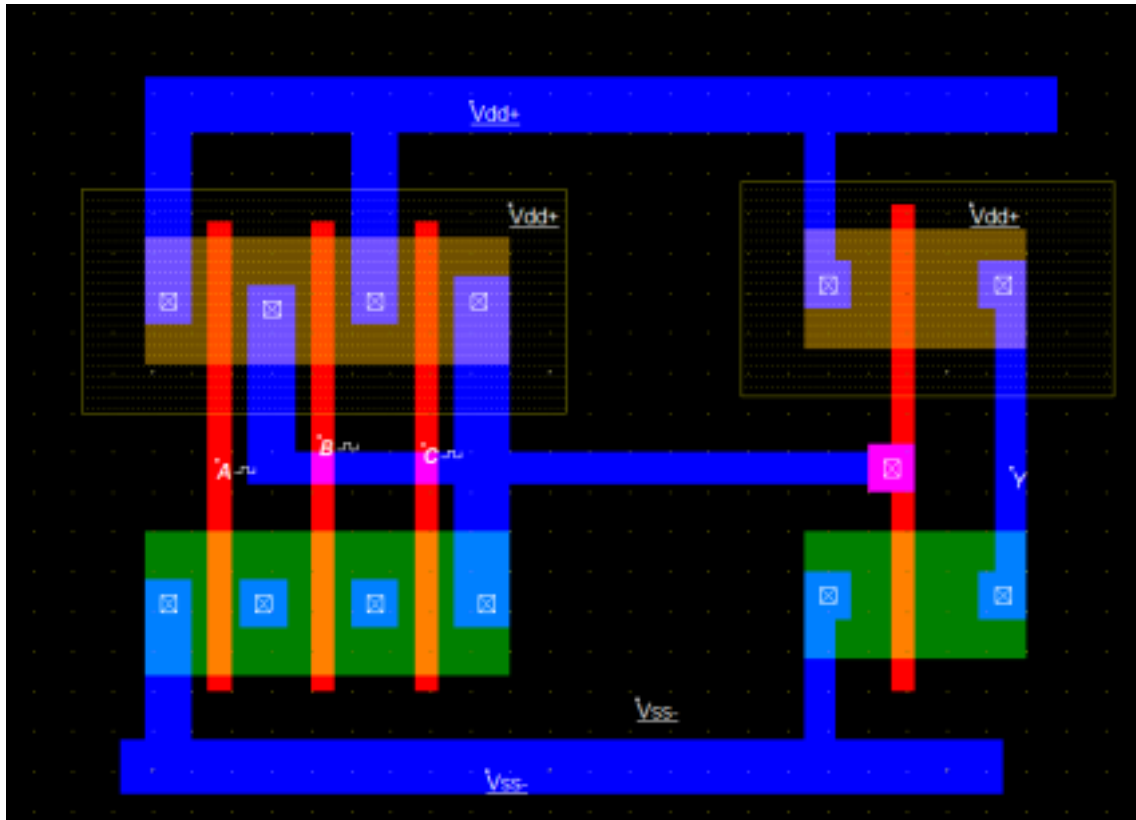
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Section: 05

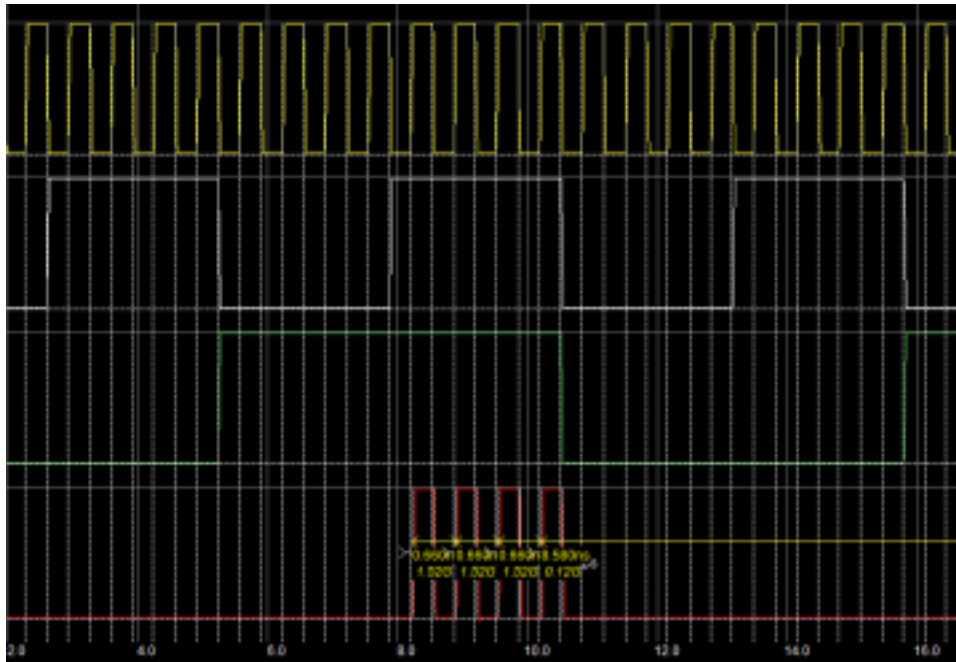
Truth Table:

A	B	C	$Y = A.B.C$
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

### Screenshot of Layout:



### Screenshot of Timing Diagram:



## Discussion:

When all three inputs are 1, which satisfies the truth table of the three input AND gate, we can see 1 in the output on the timing diagram. On the other hand, we can infer from the timing diagram that for all other input combinations, even when there are two 1s, we still produce 0 in the output, satisfying the truth table. In essence, it indicates that regardless of the values of the other two inputs, we will always receive 0 as an output if any input has a value of 0.