CSE460 - LAB 01

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Section: 05

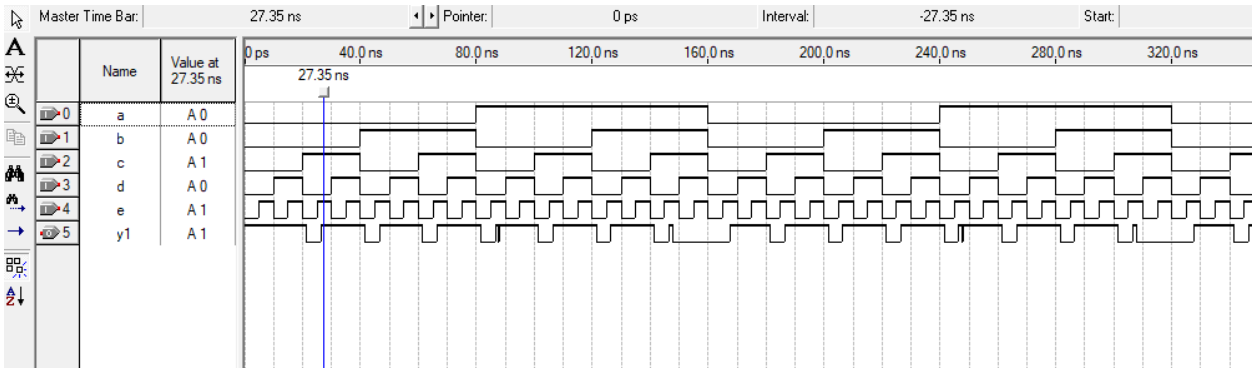
Problem statement: Write a Verilog code to implement the AOI-32 gate and verify it with the timing diagram in Quartus.

Code:

```
module aoi32(a, b, c, d, e, y1);
        input a, b, c, d, e;
        output y1;
        assign y1 = ~((a & b & c) | (d & e));
endmodule
```

Simulation report:

Waveform we will get when we set the clock of e to 10ns, d to 20ns, c to 40ns, b to 80ns and a to 160ns:

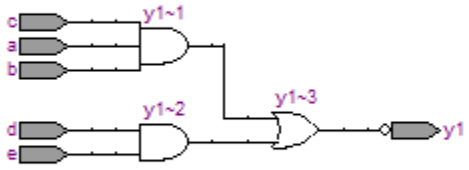


Truth table:

a	b	c	d	e	$a.b.c$	$d.e$	$a.b.c + d.e$	$\overline{a.b.c + d.e}$
0	0	0	0	0	0	0	0	1
0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	0	0	1
0	0	0	1	1	0	1	1	0
0	0	1	0	0	0	0	0	1
0	0	1	0	1	0	0	0	1

0	0	1	1	0	0	0	0	1
0	0	1	1	1	0	1	1	0
0	1	0	0	0	0	0	0	1
0	1	0	0	1	0	0	0	1
0	1	0	1	0	0	0	0	1
0	1	0	1	1	0	1	1	0
0	1	1	0	0	0	0	0	1
0	1	1	0	1	0	0	0	1
0	1	1	1	0	0	0	0	1
0	1	1	1	1	0	1	1	0
1	0	0	0	0	0	0	0	1
1	0	0	0	1	0	0	0	1
1	0	0	1	0	0	0	0	1
1	0	0	1	1	0	1	1	0
1	0	1	0	0	0	0	0	1
1	0	1	0	1	0	0	0	1
1	0	1	1	0	0	0	0	1
1	0	1	1	1	0	1	1	0
1	1	0	0	0	0	0	0	1
1	1	0	0	1	0	0	0	1
1	1	0	1	0	0	0	0	1
1	1	0	1	1	0	1	1	0
1	1	1	0	0	1	0	1	0
1	1	1	0	1	1	0	1	0
1	1	1	1	0	1	0	1	0
1	1	1	1	1	1	1	1	0

RTL view:



Discussion: From the simulation report we can see that when we set all the input to 0, or when we get 0 from both of our AND gates, we will get output as 1. If we get 1 as an output from either of the AND gates then the output will be 0 as well as for any other combinations the output will be 0. Thus, the experiment is correct as it satisfies the truth table of AOI-32 gate.