

# CSE460: VLSI Design

Lecture 11 + 12 ( 13+14)

Week 06/07

# CMOS Transistor Theory

# Contents

- Introduction
- MOS Capacitor
- nMOS I-V Characteristics
- pMOS I-V Characteristics
- Gate and Diffusion Capacitance

Reading List : [weste & Harris]

- 2·1 Introduction
- 2·2 Long channel I-V characteristics .
- Example 2·1
- 2·3·1 Simple MOS capacitance (Follow video)

# Introduction

So far, we have treated transistors as ideal switches

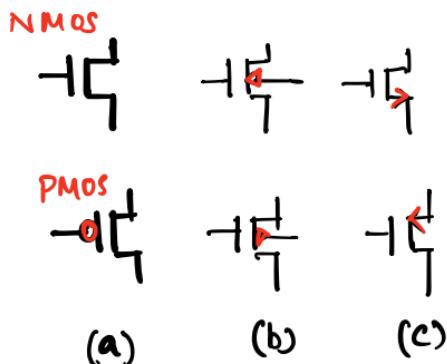
An ON transistor passes a finite amount of current

- Depends on terminal voltages
- Derive current-voltage (I-V) relationships

# Transistor gate, source, drain all have capacitance

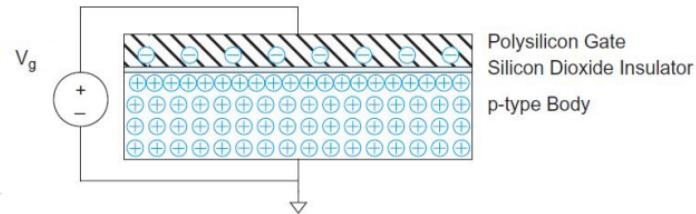
- $I = C (\Delta V / \Delta t) \rightarrow \Delta t = (C/I) \Delta V$  ↴
- Capacitance and current determine speed

MOS TRANSISTOR  
SYMBOLS



# MOS Capacitor

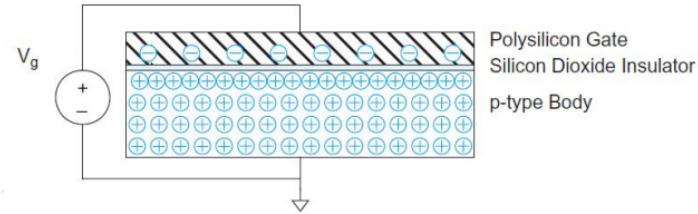
- The MOS transistor is a majority-carrier device
- Current in a conducting channel between the source and drain is controlled by a voltage applied to the gate
  - nMOS majority carriers are electrons
  - pMOS majority carriers are holes
- First, let's examine an isolated MOS structure (of an nMOS) with a gate and body, but no source or drain
- **MOSFET has gate capacitance (Oxide) & parasitic capacitance (Reversed bias p-n junction between S/D to body creates junction parasitic capacitances).**



# MOS Capacitor: Operating Modes

## MOS Structure

- Top layer: Gate
  - A Good conductor, metal or polysilicon
- Middle layer: Oxide
  - Silicon dioxide, good insulator
- Bottom layer: Silicon (doped)
  - nMOS: p-type, pMOS: n-type



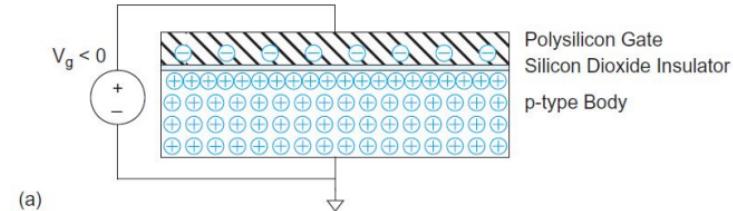
Lets ground the body, connect a voltage source  $Vg$  between the gate and body

Value of  $Vg$  decides one of three MOS operating modes: (a) Accumulation, (b) Depletion & (c) Inversion

# MOS Capacitor: Accumulation Mode

Case (a):  $V_g < 0$

- a negative voltage is applied to the gate
- there is negative charge on the gate
- The mobile positively charged holes are attracted to the region beneath the gate

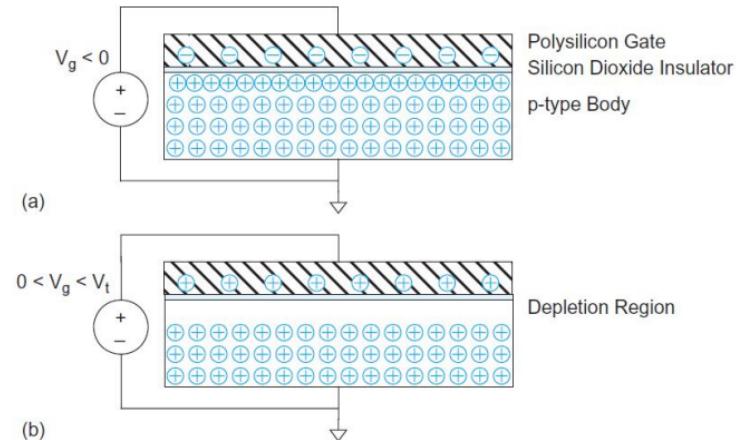


This is called the *accumulation* mode

# MOS Capacitor: Depletion Mode

Case (b):  $0 < V_g < V_t$

- a small positive voltage is applied to the gate
- resulting in some positive charge on the gate
- The holes in the body are repelled from the region directly beneath the gate, resulting in a *depletion* region forming below the gate



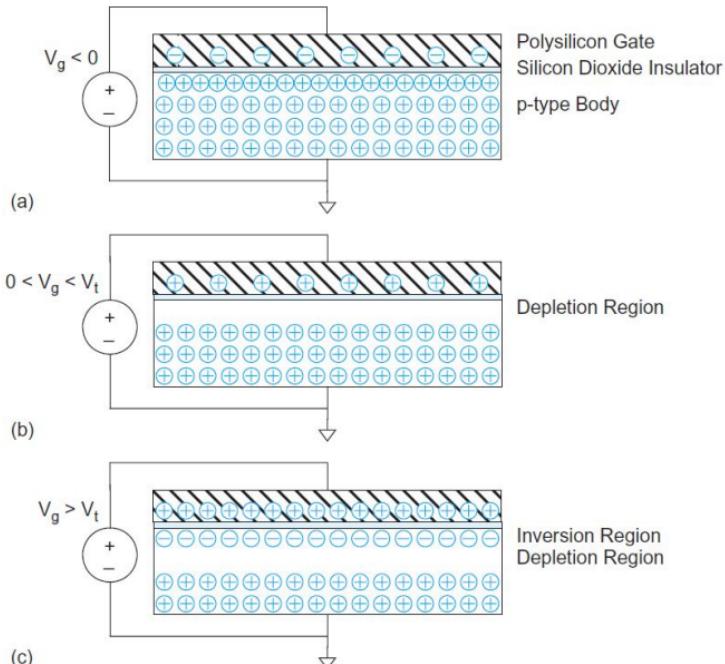
This is called the *depletion* mode

# MOS Capacitor: Inversion Mode

Case (c):  $V_g > V_t$

- a higher positive potential exceeding a critical threshold voltage  $V_t$  is applied
- more positive charge at the gate
- the holes are repelled further
- some free electrons in the body are attracted to the region beneath the gate
- this conductive layer of electrons in the p-type body is called the *inversion* layer

This is called the *inversion* mode



# MOS Capacitor: Inversion Mode

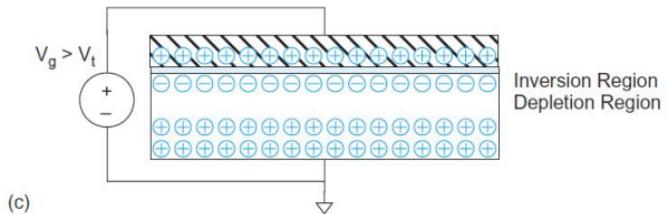
## Observation

- To conduct current we need a channel between source and drain
- An inversion channel is formed only in the inversion mode when  $V_g > V_t$
- $V_t$  is called threshold voltage ( $V_t > 0$ )

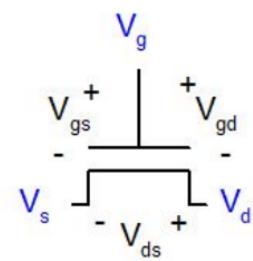
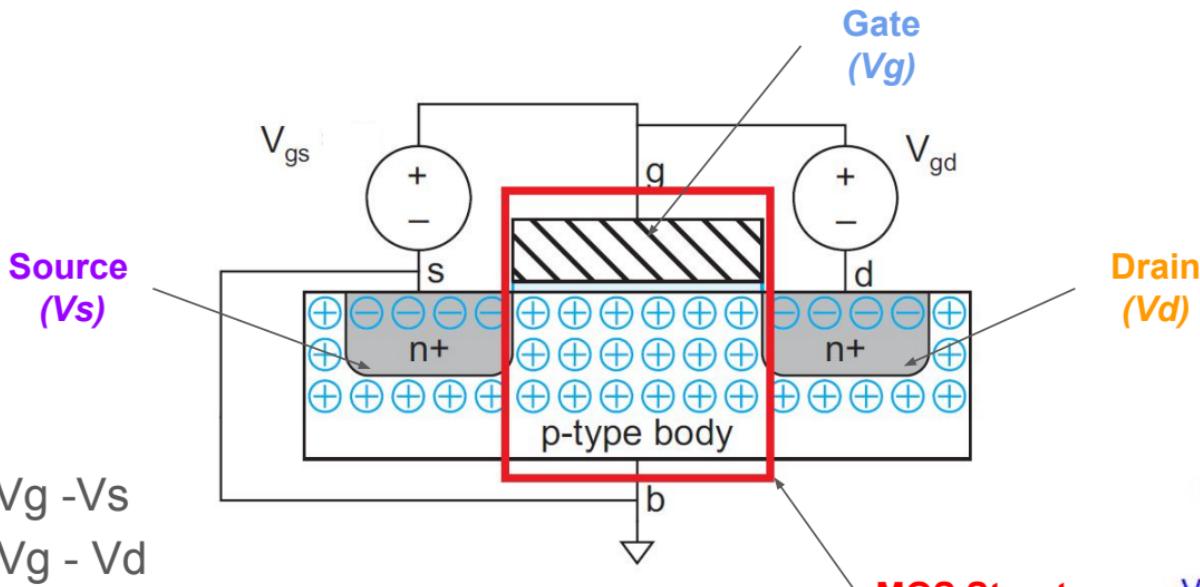
Channel exists in **Inversion mode** ( $V_g > V_t$ )

No channel exists in **Accumulation or Depletion mode** ( $V_g < V_t$ )

- The threshold voltage depends on the number of dopants in the body and thickness of the Oxide ( $t_{ox}$ ).



# nMOS Transistor



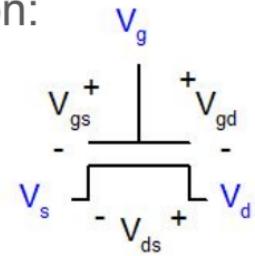
# nMOS Transistor

The gate voltage  $V_g$  merely sets up the conduction path (inversion layer) in the body of the transistor underneath the gate, i.e. it is now ready to conduct current if a voltage is set up across the conducting path, between the source and drain.

The nMOS mode of operation hence depends on all three terminal voltages & the threshold voltage of the transistor:  $V_g$ ,  $V_d$ ,  $V_s$  &  $V_t$

The source and drain are symmetric diffusion terminals. By convention:

- nMOS source is at lower voltage than drain while conducting
- Or,  $V_d \geq V_s \Rightarrow V_d - V_s \geq 0 \Rightarrow V_{ds} \geq 0$
- nMOS body is grounded



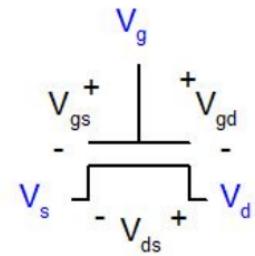
# nMOS Transistor: Operating Regions

Depending on the terminal voltage and their differences, nMOS transistor could be operating in one of the following 3 regions:

1. **Cutoff** (No current flows)
2. **Linear** (Current flows & is *proportional* to the applied voltage)
3. **Saturation** (Current flows & is *independent* of the applied voltage)

We will develop the I-V characteristics for an nMOS transistor

Similar result can be obtained from analysis of a pMOS transistor.



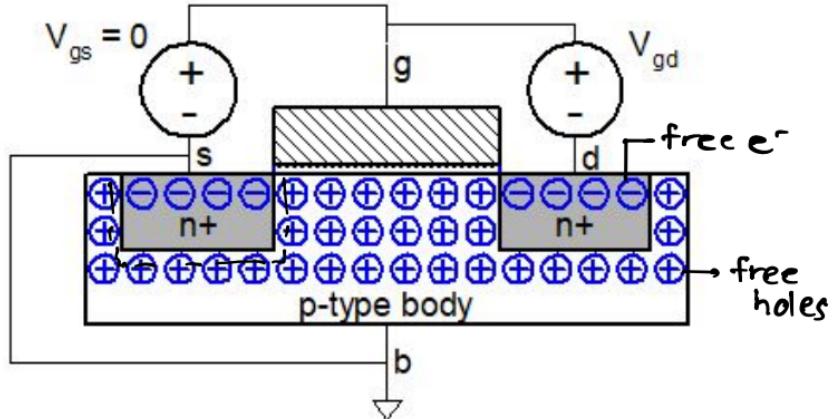
# nMOS Transistor: Cutoff

Conditions:

- $V_{gs} < V_t$
- $V_{ds}$  (doesn't matter)

Results:

- No channel, hence no current
- $I_{ds} \approx 0$  independent of  $V_{ds}$ 
  - I. Junction between body & S/D are reverse biased, so almost 0 current flows.



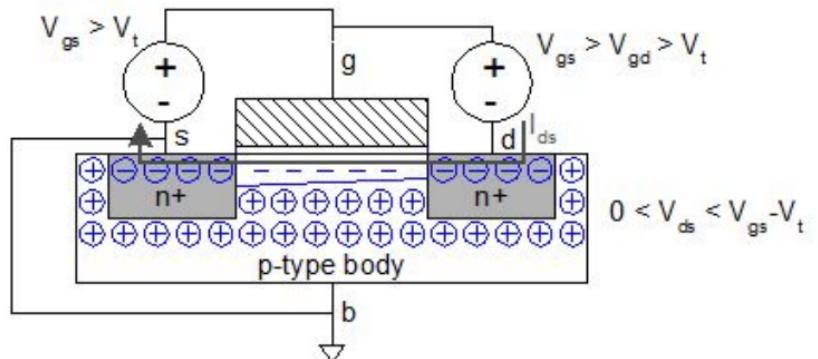
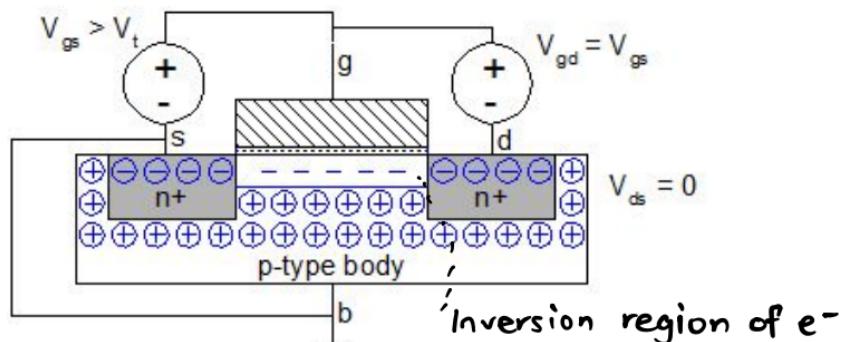
# nMOS Transistor: Linear

Conditions:

- $V_{gs} > V_t$
- $0 \leq V_{ds} < V_{gs} - V_t$

Results:

- Channel forms hence current flows
- $I_{ds} > 0$
- $I_{ds}$  increases with  $V_{ds}$
- Similar to a linear resistor
- $V_{ds} = V_{gs} - V_{gd}$
- if  $V_{ds} = 0 \Rightarrow V_{gs} = V_{gd} \rightarrow$  No electric field to push current from Drain to S.
- $V_{ds}$  is positive ;  $V_{gs} > V_{gd} \rightarrow$  current  $I_{ds}$  flows linearly. from drain to source.



from drain to S.

# nMOS Transistor: Saturation

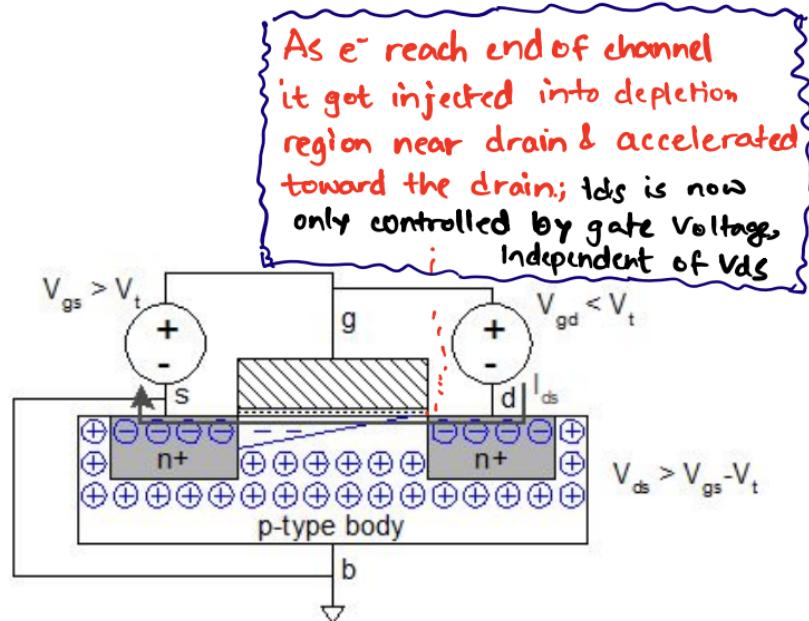
Conditions:

- $V_{gs} \geq V_t$
- $V_{ds} \geq V_{gs} - V_t$

•  $I_{ds}$  increases due to both drain & gate voltages.

Results:

- Channel forms, hence current flows
- $I_{ds} > 0$
- But channel is pinched off near the drain terminal,  $I_{ds}$  saturates
- $I_{ds}$  is independent of  $V_{ds}$
- Similar to a current source
- If  $V_{ds}$  larger than  $V_{gd} < V_t$ , channel is not inverted anymore rather pinched off near drain.



# nMOS Transistor Operating Regions: Summary

$V_t$ : nMOS threshold voltage,  $V_t > 0$  (nMOS device property)

$V_{gs}$ : gate to source voltage,  $V_{gs} = V_g - V_s$

$V_{ds}$ : drain to source voltage,  $V_{ds} = V_d - V_s$

	$V_{gs} < V_t$	$V_{gs} \geq V_t$
$0 < V_{ds} < V_{ds(\text{sat})}$	Cutoff	Linear
$V_{ds} \geq V_{ds(\text{sat})}$	Cutoff	Saturation

## First order ideal Shockley model

- When a transistor turns ON ( $V_{gs} > V_t$ ), the gate attracts carriers (electrons) to form a channel.
- The electrons drift from source to drain at a rate proportional to the electric field between these regions.
- Thus, we can compute currents if we know the amount of charge in the channel and the rate at which it moves.
- We know that the charge on each plate of a capacitor is  $Q = CV$ . Thus, the charge in the channel  $Q_{\text{channel}}$  is

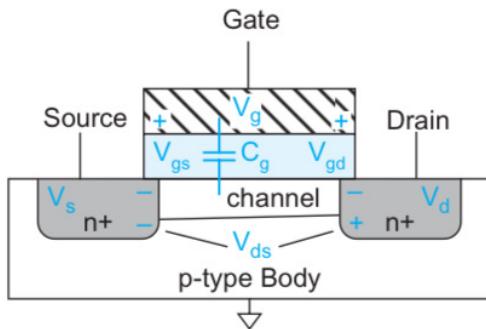
$\rightarrow \text{charge in channel, } Q_{\text{channel}} = C_g (V_{gc} - V_t)$   
 $C_g = \text{gate to channel capacitance.}$

Cut off,  $\&=0$

Linear/Saturation  
 $Q \neq 0]$

$V_{gc} - V_t = \text{Amount of voltage attracting charge to the channel beyond the minimum required to invert from p-n.}$

- If the source is at  $V_s$  and the drain is at  $V_d$ , the average is  $V_c = (V_s + V_d)/2 = V_s + V_{ds}/2$ .
- Therefore, the mean difference between the gate and channel potentials  $V_{gc}$  is  $V_g - V_c = V_{gs} - V_{ds}/2$ .



Average gate to channel potential:

$$V_{gc} = (V_{gs} + V_{gd})/2 = V_{gs} - V_{ds}/2$$

FIGURE 2.5 Average gate to channel voltage

- We can model the gate as a parallel plate capacitor with capacitance proportional to area over thickness. If the gate has length  $L$  and width  $W$  and the oxide thickness is  $t_{\text{ox}}$ , the capacitance is

$$C_g = k_{\text{ox}} \epsilon_0 \frac{WL}{t_{\text{ox}}} = \epsilon_{\text{ox}} \frac{WL}{t_{\text{ox}}} = C_{\text{ox}} WL \quad (2.2)$$

where  $\epsilon_0$  is the permittivity of free space,  $8.85 \times 10^{-14}$  F/cm, and the permittivity of  $\text{SiO}_2$  is  $k_{\text{ox}} = 3.9$  times as great. Often, the  $\epsilon_{\text{ox}}/t_{\text{ox}}$  term is called  $C_{\text{ox}}$ , the capacitance per unit area of the gate oxide.

Some nanometer processes use a different gate dielectric with a higher dielectric constant. In these processes, we call  $t_{\text{ox}}$  the *equivalent oxide thickness* (EOT), the thickness of a layer of  $\text{SiO}_2$  that has the same  $C_{\text{ox}}$ . In this case,  $t_{\text{ox}}$  is thinner than the actual dielectric.

Each carrier in the channel is accelerated to an average velocity,  $v$ , proportional to the lateral electric field, i.e., the field between source and drain. The constant of proportionality  $\mu$  is called the *mobility*.

$$v = \mu E \quad (2.3)$$

A typical value of  $\mu$  for electrons in an nMOS transistor with low electric fields is 500–700  $\text{cm}^2/\text{V}\cdot\text{s}$ . However, most transistors today operate at far higher fields where the mobility is severely curtailed (see Section 2.4.1).

The electric field  $E$  is the voltage difference between drain and source  $V_{ds}$  divided by the channel length

$$E = \frac{V_{ds}}{L} \quad (2.4)$$

The time required for carriers to cross the channel is the channel length divided by the carrier velocity:  $L/v$ . Therefore, the current between source and drain is the total amount of charge in the channel divided by the time required to cross

$$\begin{aligned} I_{ds} &= \frac{Q_{\text{channel}}}{L/v} \\ &= \mu C_{\text{ox}} \frac{W}{L} (V_{gs} - V_t - V_{ds}/2) V_{ds} \\ &= \beta (V_{GT} - V_{ds}/2) V_{ds} \end{aligned} \quad (2.5)$$

where

$$\beta = \mu C_{\text{ox}} \frac{W}{L}; \boxed{V_{GT} = V_{gs} - V_t} \quad (2.6)$$

The term  $V_{gs} - V_t$  arises so often that it is convenient to abbreviate it as  $V_{GT}$ . EQ (2.5) describes the linear region of operation, for  $V_{gs} > V_t$ , but  $V_{ds}$  relatively small. It is called *linear* or *resistive* because when  $V_{ds} \ll V_{GT}$ ,  $I_{ds}$  increases almost linearly with  $V_{ds}$ , just like an ideal resistor. The geometry and technology-dependent parameters are sometimes merged into a single factor  $\beta$ . Do not confuse this use of  $\beta$  with the same symbol used for the ratio of collector-to-base current in a bipolar transistor. Some texts [Gray01] lump the technology-dependent parameters alone into a constant called “ $k$  prime.”<sup>3</sup>

$$k' = \mu C_{\text{ox}} \quad (2.7)$$

If  $V_{ds} > V_{\text{dsat}} \equiv V_{GT}$ , the channel is no longer inverted in the vicinity of the drain; we say it is pinched off. Beyond this point, called the *drain saturation voltage*, increasing the drain voltage has no further effect on current. Substituting  $V_{ds} = V_{\text{dsat}}$  at this point of maximum current into EQ (2.5), we find an expression for the saturation current that is independent of  $V_{ds}$ .

$$I_{ds} = \frac{\beta}{2} V_{GT}^2 \quad (2.8)$$

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<sup>3</sup>Other sources (e.g., MOSIS) define  $k' = \frac{\mu C_{\text{ox}}}{2}$ ; check the definition before using quoted data.

This expression is valid for  $V_{gs} > V_t$  and  $V_{ds} > V_{dsat}$ . Thus, long-channel MOS transistors are said to exhibit *square-law behavior* in saturation.

Two key figures of merit for a transistor are  $I_{on}$  and  $I_{off}$ .  $I_{on}$  (also called  $I_{dsat}$ ) is the ON current,  $I_{ds}$ , when  $V_{gs} = V_{ds} = V_{DD}$ .  $I_{off}$  is the OFF current when  $V_{gs} = 0$  and  $V_{ds} = V_{DD}$ . According to the long-channel model,  $I_{off} = 0$  and

$$I_{on} = \frac{\beta}{2}(V_{DD} - V_t) \quad (2.9)$$

EQ(2.10) summarizes the current in the three regions:

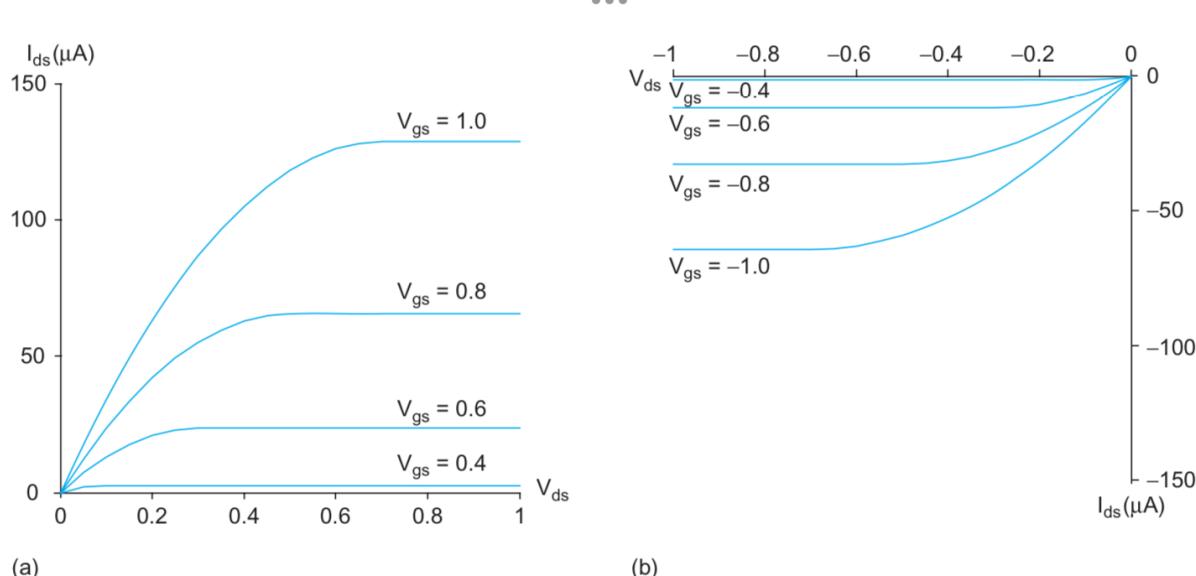
$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \\ \beta(V_{GT} - V_{ds}/2)V_{ds} & V_{ds} < V_{dsat} \\ \frac{\beta}{2}V_{GT}^2 & V_{ds} > V_{dsat} \end{cases} \quad \begin{matrix} \text{Cutoff} \\ \text{Linear} \\ \text{Saturation} \end{matrix} \quad (2.10)$$

### Example 2.1

Consider an nMOS transistor in a 65 nm process with a minimum drawn channel length of 50 nm ( $\lambda = 25$  nm). Let  $W/L = 4/2\lambda$  (i.e., 0.1/0.05  $\mu\text{m}$ ). In this process, the gate oxide thickness is 10.5 Å. Estimate the high-field mobility of electrons to be 80  $\text{cm}^2/\text{V}\cdot\text{s}$  at 70 °C. The threshold voltage is 0.3 V. Plot  $I_{ds}$  vs.  $V_{ds}$  for  $V_{gs} = 0, 0.2, 0.4, 0.6, 0.8$ , and 1.0 V using the long-channel model.

**SOLUTION:** We first calculate  $\beta$ .

$$\beta = \mu C_{ox} \frac{W}{L} = \left(80 \frac{\text{cm}^2}{\text{V}\cdot\text{s}}\right) \left(\frac{3.9 \times 8.85 \times 10^{-14} \frac{\text{F}}{\text{cm}}}{10.5 \times 10^{-8} \text{cm}}\right) \left(\frac{W}{L}\right) = 262 \frac{W}{L} \frac{\text{A}}{\text{V}^2} \quad (2.11)$$



(a)

(b)

**FIGURE 2.7** I-V characteristics of ideal 4/2  $\lambda$  (a) nMOS and (b) pMOS transistors

# nMOS Transistor: I-V Summary

$$I_{ds} = \begin{cases} 0 & \text{if } V_{gs} < V_t \text{ (Cutoff)} \\ \beta(V_{gs} - V_t - \frac{V_{ds}}{2})V_{ds} & \text{if } V_{ds} < V_{ds(sat)} \text{ (Linear)} \\ \frac{\beta}{2}(V_{gs} - V_t)^2 & \text{if } V_{ds} \geq V_{ds(sat)} \text{ (Saturation)} \end{cases}$$

Where  $\beta = \mu_n C_{ox} W/L$  &  $V_{ds(sat)} = V_{gs} - V_t$

# pMOS Transistor Operating Regions: Summary

Exactly opposite of NMOS

$V_{tp}$ : pMOS threshold voltage,  $V_{tp} < 0$  (pMOS device property)

$V_{sg}$ : source to gate voltage,  $V_{sg} = V_s - V_g$

$V_{sd}$ : source to drain voltage,  $V_{sd} = V_s - V_d$

	$V_{sg} <  V_{tp} $	$V_{sg} \geq  V_{tp} $
$0 < V_{sd} < V_{sd(\text{sat})}$	Cutoff	Linear
$V_{sd} \geq V_{sd(\text{sat})}$	Cutoff	Saturation

# pMOS Transistor: I-V Summary

$$I_{sd} = \begin{cases} 0 & \text{if } V_{sg} < |V_{tp}| \text{ (Cutoff)} \\ \beta_p(V_{sg} - |V_{tp}| - \frac{V_{sd}}{2})V_{sd} & \text{if } V_{sd} < V_{sd(sat)} \text{ (Linear)} \\ \frac{\beta_p}{2}(V_{sg} - |V_{tp}|)^2 & \text{if } V_{sd} \geq V_{sd(sat)} \text{ (Saturation)} \end{cases}$$

Where  $\beta_p = \mu_p C_{ox} W/L$  &  $V_{sd(sat)} = V_{sg} - |V_{tp}|$

# MOSFET Capacitance

Any two conductors separated by an insulator have capacitance

Gate to channel capacitor is very important (**gate capacitance:**  $C_g$ )

- Creates channel charge necessary for operation

Source and drain have capacitance to body (**diffusion capacitance:**  $C_{sb}$ ,  $C_{db}$ )

- Across reverse-biased diodes
- Called diffusion capacitance because it is associated with source/drain diffusion
- Remember that nMOS body is connected to ground and pMOS body is connected to supply (Vdd)

## 2.3 C-V Characteristics

Each terminal of an MOS transistor has capacitance to the other terminals. In general, these capacitances are nonlinear and voltage dependent (C-V); however, they can be approximated as simple capacitors when their behavior is averaged across the switching voltages of a logic gate. This section first presents simple models of each capacitance suitable for estimating delay and power consumption of transistors. It then explores more detailed models used for circuit simulation. The more detailed models may be skipped on a first reading.

### 2.3.1 Simple MOS Capacitance Models

The gate of an MOS transistor is a good capacitor. Indeed, its capacitance is necessary to attract charge to invert the channel, so high gate capacitance is required to obtain high  $I_{ds}$ . As seen in Section 2.2, the gate capacitor can be viewed as a parallel plate capacitor with the gate on top and channel on bottom with the thin oxide dielectric between. Therefore, the capacitance is

$$C_g = C_{\text{ox}}WL \quad (2.12)$$

The bottom plate of the capacitor is the channel, which is not one of the transistor's terminals. When the transistor is on, the channel extends from the source (and reaches the drain if the transistor is unsaturated, or stops short in saturation). Thus, we often approximate the gate capacitance as terminating at the source and call the capacitance  $C_{gs}$ .

Most transistors used in logic are of minimum manufacturable length because this results in greatest speed and lowest dynamic power consumption.<sup>4</sup> Thus, taking this mini-

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<sup>4</sup>Some designs use slightly longer than minimum transistors that have higher thresholds because of the short-channel effect (see Sections 2.4.3.3 and 5.3.3). This avoids the cost of an extra mask step for high- $V_t$  transistors. The change in channel length is small (~5–10%), so the change in gate capacitance is minor.

•••

mum  $L$  as a constant for a particular process, we can define

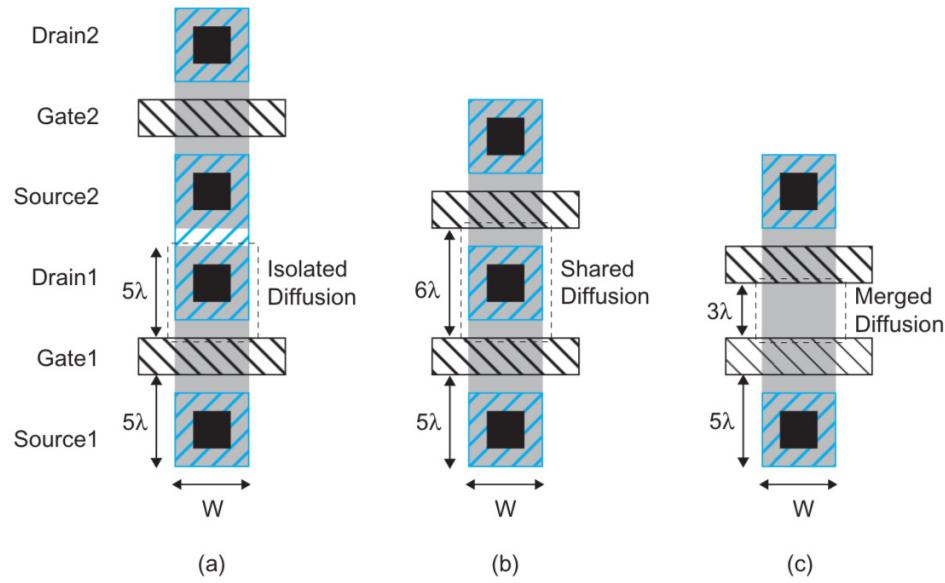
$$C_g = C_{\text{permicron}} \times W \quad (2.13)$$

where

$$C_{\text{permicron}} = C_{\text{ox}} L = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}} L \quad (2.14)$$

Notice that if we develop a more advanced manufacturing process in which both the channel length and oxide thickness are reduced by the same factor,  $C_{\text{permicron}}$  remains unchanged. This relationship is handy for quick calculations but not exact;  $C_{\text{permicron}}$  has fallen from about  $2 \text{ fF}/\mu\text{m}$  in old processes to about  $1 \text{ fF}/\mu\text{m}$  at the 90 and 65 nm nodes. Table 8.5 lists gate capacitance for a variety of processes.

In addition to the gate, the source and drain also have capacitances. These capacitances are not fundamental to operation of the devices, but do impact circuit performance and hence are called *parasitic* capacitors. The source and drain capacitances arise from the p–n junctions between the source or drain diffusion and the body and hence are also called *diffusion*<sup>5</sup> capacitance  $C_{sb}$  and  $C_{db}$ . A *depletion region* with no free carriers forms along the junction. The depletion region acts as an insulator between the conducting p- and n-type regions, creating capacitance across the junction. The capacitance of these junctions depends on the area and perimeter of the source and drain diffusion, the depth of the diffusion, the doping levels, and the voltage. As diffusion has both high capacitance and high resistance, it is generally made as small as possible in the layout. Three types of diffusion regions are frequently seen, illustrated by the two series transistors in Figure 2.8. In Figure



**FIGURE 2.8** Diffusion region geometries

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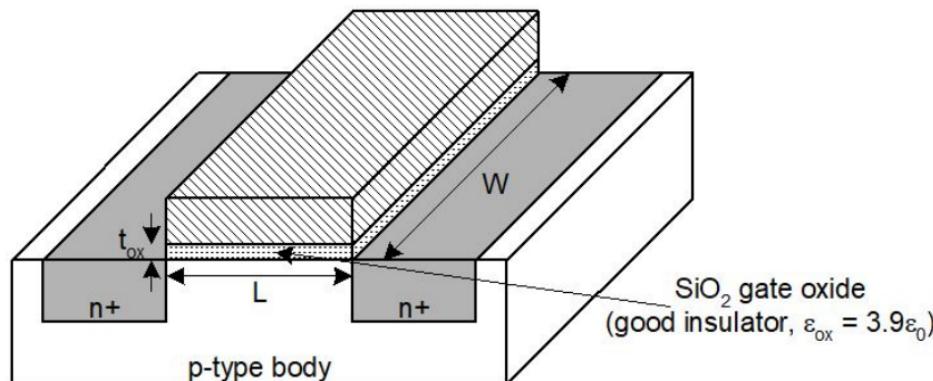
<sup>5</sup>Device engineers more properly call this *depletion* capacitance, but the term *diffusion* capacitance is widely used by circuit designers.

# Gate Capacitance

$C_g$  = Gate capacitance

$$C_g = \epsilon_{ox} WL/t_{ox} = C_{ox} WL = C_{permicron} W$$

$C_{permicron}$  is typically about 2 fF/mm



# Diffusion Capacitance

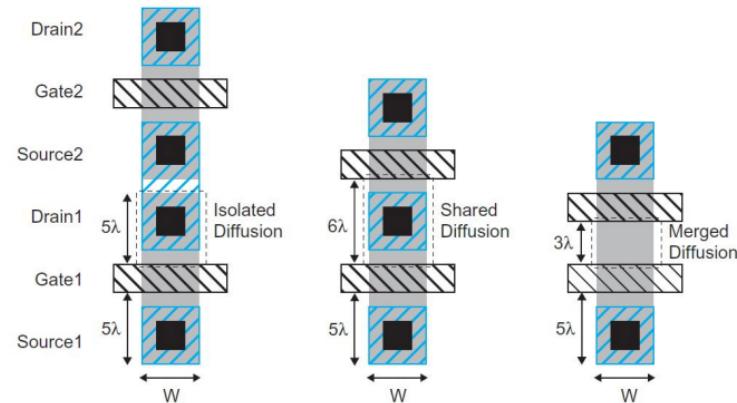
$C_{sb}$  = Source to body capacitance

$C_{db}$  = Drain to body capacitance

Undesirable, called parasitic capacitance

Capacitance depends on area and perimeter

- Use small diffusion nodes
- Comparable to  $C_g$  for contacted diff
- $\frac{1}{2} C_g$  for uncontacted
- Varies with process

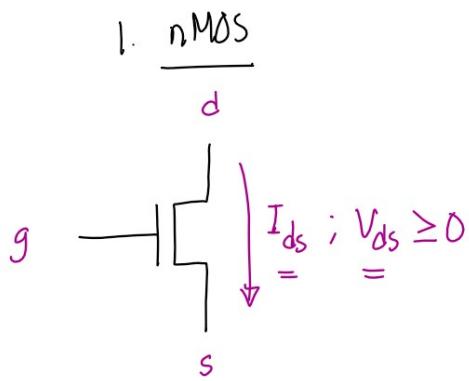


# MOSFET I-V Summary & Examples

Tuesday, July 27, 2021 1:11 AM

I-V characteristics of MOSFET devices:

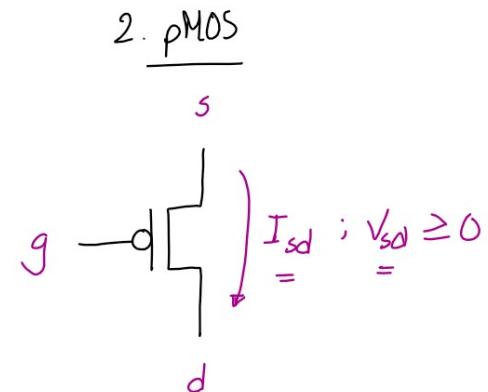
Current & Voltage



$V_t$ : Threshold voltage  $V_t > 0$

$$\beta = \mu_n \frac{E_{ox}}{t_{ox}} \left( \frac{W}{L} \right)_n$$

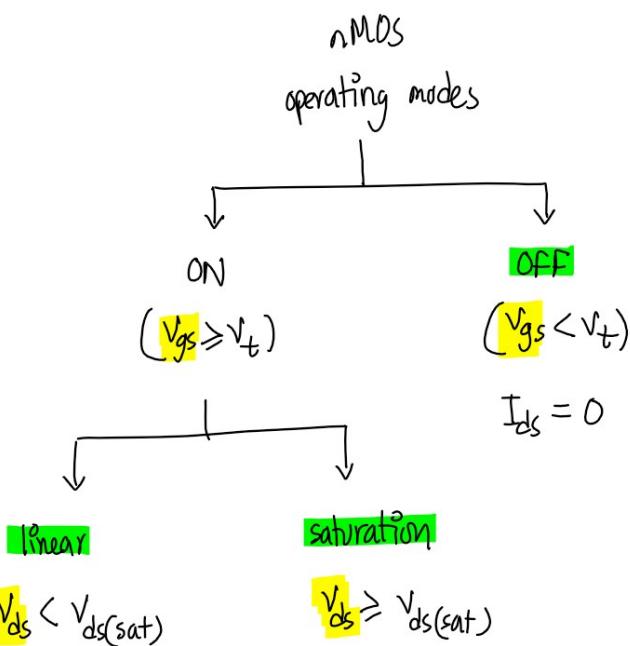
$$V_{ds(\text{sat})} = V_{gs} - V_t$$



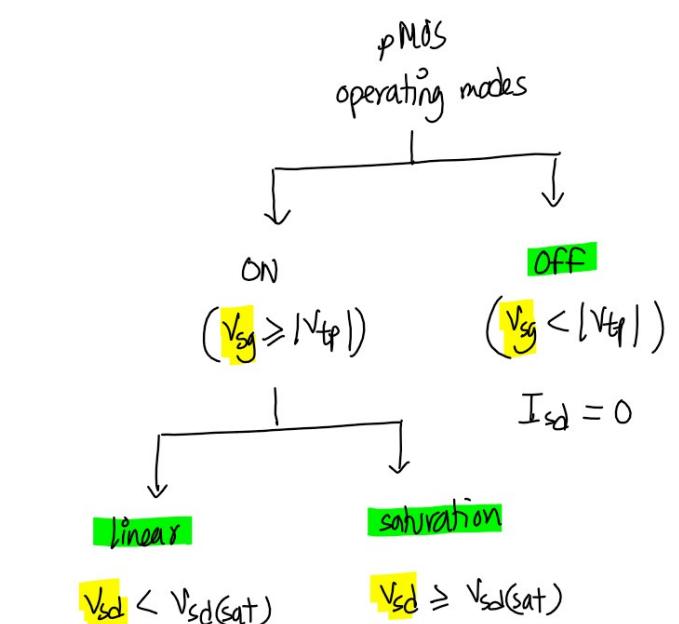
$V_{tp}$ : Threshold voltage  $V_{tp} < 0$

$$\beta_p = \mu_p \frac{E_{ox}}{t_{ox}} \left( \frac{W}{L} \right)_p$$

$$V_{sd(\text{sat})} = V_{sg} - |V_{tp}|$$



$$I_{ds} = \beta \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} \quad I_{ds} = \frac{\beta}{2} \left( V_{gs} - V_t \right)^2$$



$$I_{sd} = \beta_p \left( |V_{sg}| - |V_{tp}| - \frac{|V_{sd}|}{2} \right) V_{sd} \quad I_{ds} = \frac{\beta_p}{2} (V_{sg} - |V_{tp}|)^2$$

	$V_{gs} < V_t$	$V_{gs} \geq V_t$
$V_{ds} < V_{ds(\text{sat})}$	Cutoff	Linear
$V_{ds} \geq V_{ds(\text{sat})}$	Cutoff	Saturation

	$V_{sg} <  V_{tp} $	$V_{sg} \geq  V_{tp} $
$V_{sd} < V_{sd(\text{sat})}$	Cutoff	Linear
$V_{sd} \geq V_{sd(\text{sat})}$	Cutoff	Saturation

$$I_{ds} = \begin{cases} 0 & \xrightarrow{\text{cutoff}} \\ \beta \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} & \xrightarrow{\text{linear}} \\ \frac{\beta}{2} (V_{gs} - V_t)^2 & \xrightarrow{\text{saturation}} \end{cases}$$

$$I_{sd} = \begin{cases} 0 & \xrightarrow{\text{cutoff}} \\ \beta_p \left( V_{sg} - |V_{tp}| - \frac{V_{sd}}{2} \right) V_{sd} & \xrightarrow{\text{linear}} \\ \frac{\beta_p}{2} (V_{sg} - |V_{tp}|)^2 & \xrightarrow{\text{saturation}} \end{cases}$$

## # Problem 1

→ nMOS.

Consider an n-channel MOSFET with the following parameters:

$V_t = 0.4$  V,  $W = 20$  μm,  $L = 0.8$  μm,  $\mu_n = 650$  cm<sup>2</sup>/V-s,  $t_{ox} = 200$  Å, and  $\epsilon_{ox} = (3.9)(8.85 \times 10^{-14})$  F/cm.

Calculate  $\beta$ . Then determine the operating mode and the current through the transistor ( $I_{ds}$ ) for the following cases:

(a)  $V_{gs} = 0.8$  V &  $V_{ds} = 0.2$  V

(b)  $V_{gs} = 1.6$  V &  $V_{ds} = 2.0$  V

$$\beta = \mu_n \frac{\epsilon_{ox}}{t_{ox}} \frac{W}{L} = 650 \times \frac{3.9 \times 8.854 \times 10^{-14}}{200 \times 10^{-8}} \times \frac{20}{0.8} \quad \frac{\text{cm}^2}{\text{V}\cdot\text{s}} \times \frac{\text{A}}{\text{cm}^2} \cdot \frac{1}{\text{cm}} \times \frac{\text{A}}{\text{cm}}$$

$$= 0.0027105 \frac{\text{A}}{\text{V}^2} = 2.7105 \frac{\text{mA}}{\text{V}^2} \quad t_{ox} = 200 \text{ Å} \quad 1 \text{ Å} = 10^{-10} \text{ m} \\ = 10^{-8} \text{ cm}$$

(a)  $V_{gs} = 0.8$  V     $V_t = 0.4$  V     $V_{gs} > V_t \Rightarrow \text{ON mode}$

$$V_{ds(\text{sat})} = V_{gs} - V_t = (0.8 - 0.4) \text{ V} = 0.4 \text{ V} \quad V_{ds} = 0.2 \text{ V} < V_{ds(\text{sat})} = 0.4 \text{ V} \Rightarrow \text{linear}$$

$$I_{ds} = \beta \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} = 0.0027105 \times \left( 0.8 - 0.4 - \frac{0.2}{2} \right) \times 0.2 \quad \frac{\text{A}}{\text{V}^2} \times \text{V}^2$$

$$= 0.00016263 \text{ A} = 0.16263 \text{ mA. } \blacksquare$$

(b)  $V_{gs} = 1.6$  V     $V_t = 0.4$  V     $V_{gs} > V_t \Rightarrow \text{ON mode}$

$$V_{ds(\text{sat})} = V_{gs} - V_t = (1.6 - 0.4) \text{ V} = 1.2 \text{ V} \quad V_{ds} = 2 \text{ V} \quad V_{ds} > V_{ds(\text{sat})} \Rightarrow \text{saturation}$$

$$I_{ds} = \frac{\beta}{2} \left( V_{gs} - V_t \right)^2 = \frac{0.0027105}{2} \times (1.6 - 0.4)^2 \quad \frac{\text{A}}{\text{V}^2} \times \text{V}^2$$

$$= 0.001952 \text{ A} = 1.952 \text{ mA} \quad \blacksquare$$

↑ This value was wrongly calculated in book 1

→ This value was wrongly calculated in box 1

## # Problem 2

For a 0.8- $\mu\text{m}$  process technology,  $t_{\text{ox}} = 15 \text{ nm}$ ,  $\mu = 275 \text{ cm}^2/\text{V}\cdot\text{s}$ ,  $\epsilon_{\text{ox}} = (3.9)(8.85 \times 10^{-14}) \text{ F/cm}$  and  $V_t = -0.7 \text{ V}$ .

(a) Judging from the value of  $V_t$  and  $\mu$ , comment on whether the MOSFET is NMOS or PMOS

(b) Calculate  $C_{\text{ox}}$

(c) For a MOSFET with  $W/L = 20$  calculate the values of  $\beta$ ,  $V_{\text{sg}}$  and  $V_{\text{sd(min)}}$  needed to operate the transistor in the saturation region with a dc current of  $I_d = 0.1 \text{ mA}$

(a) since  $V_t = -0.7 \text{ V}$ ;  $V_t < 0 \Rightarrow \text{pMOS}$ .  $\mu = 275$

$$(b) C_{\text{ox}} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}} = \frac{3.9 \times 8.854 \times 10^{-14}}{15 \times 10^{-8}} \frac{\text{F}/\text{cm}}{\text{cm}} = 0.000002302 \text{ F} = 2.302 \times 10^{-6} \text{ F}$$

$$(c) \beta = \mu \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}} \frac{W}{L} = 275 \times 2.302 \times 10^{-6} \times 20 \frac{\text{A}}{\sqrt{\text{V}}} = 0.012661 \frac{\text{A}}{\sqrt{\text{V}}}$$

saturation region condition for pMOS :  $V_{\text{sd}} \geq V_{\text{sd}(\text{sat})} (= V_{\text{gs}} - |V_t|)$

$$V_{\text{sd}(\text{min})} = V_{\text{sg}} - |V_t| = 0.82568 - 0.7 \text{ V} = 0.1278 \text{ V} \quad V_{\text{sg}} = 0.82568 \text{ V}$$

$$\begin{aligned} V_{\text{sd}(\text{min})} &= V_{\text{sg}} - |V_t| \\ \text{in sat' reg'DN, } I_d &= \frac{\beta}{2} (V_{\text{sg}} - |V_t|)^2 \\ V_{\text{sg}} &= \sqrt{\frac{2I_d}{\beta}} + |V_t| \\ &= \sqrt{\frac{2 \times 0.1 \times 10^{-3}}{0.012661}} + 0.7 \\ &= 0.82568 \text{ V} \end{aligned}$$

## # Problem 3

$$V_t = 0.3 \text{ V}$$

Consider an nMOS transistor in a 65 nm process with a minimum drawn channel length of 50 nm ( $\lambda = 25 \text{ nm}$ ). Let  $W/L = 4/2\lambda$  (i.e.,  $0.1/0.05 \mu\text{m}$ ). In this process, the gate oxide thickness is  $10.5 \text{ \AA}$ . Estimate the high-field mobility of electrons to be  $80 \text{ cm}^2/\text{V}\cdot\text{s}$  at  $70^\circ\text{C}$ . The threshold voltage is  $0.3 \text{ V}$ . Plot  $I_{ds}$  vs.  $V_{ds}$  for  $V_{\text{gs}} = 0, 0.2, 0.4, 0.6, 0.8$ , and  $1.0 \text{ V}$  using the long-channel model.

$$V_{\text{gs}} = 0 \rightarrow V_{\text{gs}} < V_t \rightarrow \text{off} \rightarrow I_{ds} = 0$$

$$V_{\text{gs}} = 0.2 \text{ V} \rightarrow V_{\text{gs}} < V_t \rightarrow \text{off} \rightarrow I_{ds} = 0$$

$$V_{\text{gs}} = 0.4 \text{ V} \rightarrow V_{\text{gs}} > V_t \rightarrow \text{ON} \quad \text{if } I_{ds} \neq 0 : V_{ds(\text{sat})} = V_{\text{gs}} - V_t = 0.1 \text{ V}$$

$$V_{ds} < 0.1 \quad I_{ds} = \beta \left( V_{\text{gs}} - V_t - \frac{V_{ds}}{2} \right) V_{ds}$$

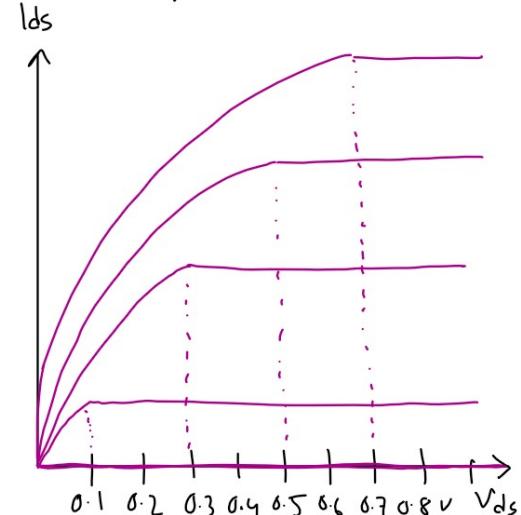
$$V_{ds} \geq 0.1 \quad I_{ds} = \beta/2 (V_{\text{gs}} - V_t)$$

$$V_{\text{gs}} = 0.6 \rightarrow V_{\text{gs}} > V_t \rightarrow \text{ON} \rightarrow V_{ds(\text{sat})} = 0.6 - 0.3 = 0.3$$

$$V_{\text{gs}} = 0.8 \rightarrow V_{ds(\text{sat})} = 0.8 - 0.3 \rightarrow 0.5 \text{ V} \quad V_{\text{gs}} = 1 \text{ V} ; V_{ds(\text{sat})} = 1 - 0.3 - 0.7 \text{ V}$$

$$\beta = 80 \times \frac{3.9 \times 8.854 \times 10^{-14}}{10.5 \times 10^{-8}} \times \frac{4}{2} \frac{\text{A}}{\text{V}^2}$$

$$= 526 \frac{\text{mA}}{\text{V}^2}$$



Homework: try for pMOS

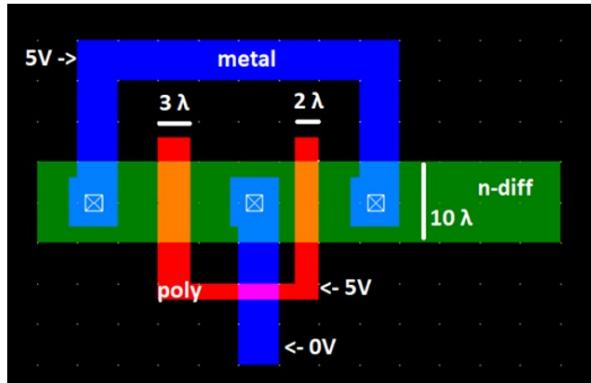
## # Problem 4

Concept: polysilicon crossing diffusion creates transistors ✓

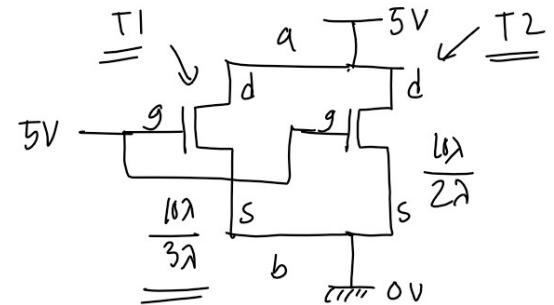
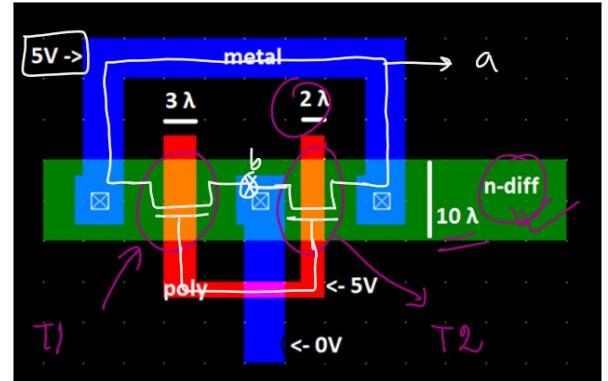
Using the figure given below, answer the following questions:

transistors ✓

Using the figure given below, answer the following questions:



- a. Draw the schematic diagram of the circuit (that results in this layout) and then clearly mark the length and width of each of the transistors.  
 b. Find the current flowing through each of the transistors, if  $\mu_n C_{ox} = 120 \mu A/V^2$ ,  $V_t = 1 V$



$$(b) \quad T1 \quad V_t = 1V \quad \mu_n C_{ox} = 120 \mu A/V^2$$

$$V_{gs} = 5V - 0V = 5V > V_t \quad \underline{\text{ON}}$$

$$V_{ds(\text{sat})} = V_{gs} - V_t = 5 - 1V = 4V$$

$$V_{ds} = 5 - 0V = 5V > V_{ds(\text{sat})} \Rightarrow \text{Saturation}$$

$$\begin{aligned} I_{ds} &= \frac{\rho}{2} (V_{gs} - V_t)^2 \\ &= \frac{1}{2} \cdot \underline{\mu_n C_{ox}} \frac{W}{L} (V_{gs} - V_t)^2 \\ &= \frac{1}{2} \times 120 \times \frac{10}{3} (5-1)^2 \\ &= 60 \times \frac{10}{3} \times 16 \end{aligned}$$

$$\begin{aligned} &= 3200 \mu A \\ &= 3.2 \text{ mA} \quad \checkmark \end{aligned}$$

$$I_{ds} = \frac{\rho}{2} (V_{gs} - V_t)^2$$

$$= \frac{1}{2} \times 120 \times \frac{W}{L} \times (V_{gs} - V_t)^2$$

$$= \frac{1}{2} \times 120 \times \frac{10}{2} \times 16 \mu A$$

$$= 4800 \mu A = 4.8 \text{ mA. } \checkmark$$