BRAC University
Department of Computer Science and Engineering
CSE-350
EXP-4

Name of the Experiment: Analysis of the binary weighted and R/2R ladder D/A converters.

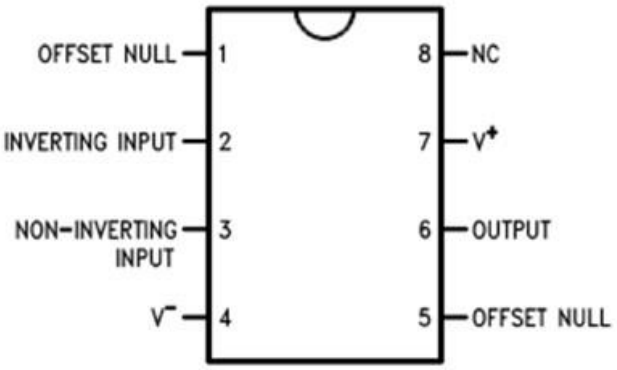
Objective:

The objective of this experiment is to construct two different D/A converter and to verify that digital signal is converted into proportional analog signal.

Equipment:

Resistance = 10K, 20K, 5K, 2.5K, 1.25K
Dc source
Operational Amplifier
Multimeter

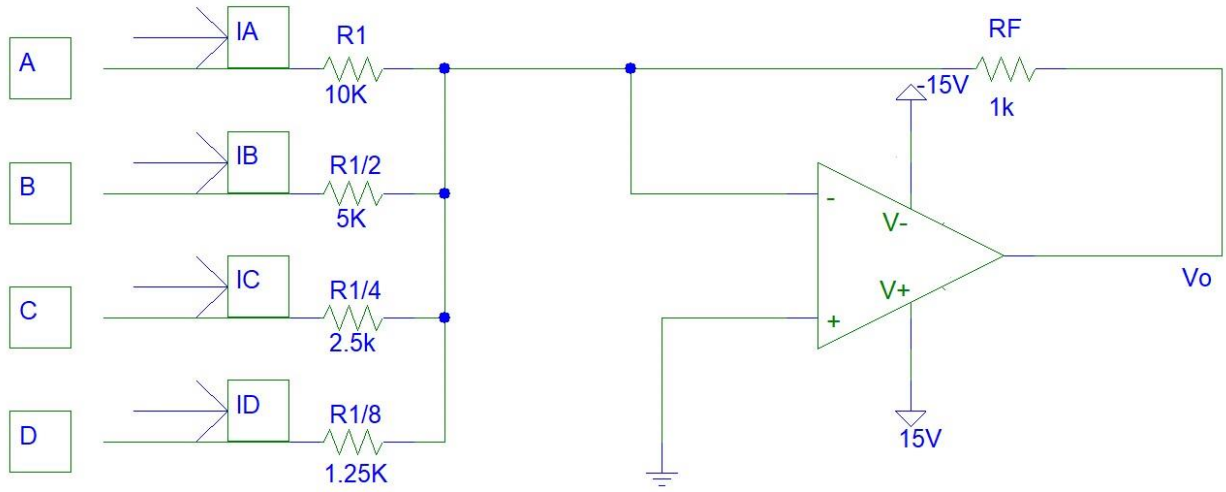
Op-Amp Device:



In case of biasing the operational op-amp, sort out the positive and negative terminals of two different DC sources. Then connect the rest positive terminal to positive biasing(+V) and the rest negative terminal to negative biasing terminal (-V). The sorted terminal is the ground of the whole circuit. The biasing voltages should be set to +- 15V.

Circuit Diagram 1:

Digital to Analog Converter using Binary-Weighted Resistors



Theory:

A four bit converter will have $2^4 = 16$ input combinations. Consequently, the converter will show 16 different output analog voltage levels for 16 of the different combinations.

Working Principle:

Case 1: A=1 and B=C=D=0:

The voltage across R1 is 5V. So, the current through R1 is IA=0.5mA. Since the current into the op-amp input terminals are negligible, this 0.5mA current will flow through the RF resistance. Hence, the voltage across the resistance RF is,

$$V_{RF} = 0.5mA * 1K = 0.5V$$

Consequently, the output voltage is at -0.5V.

Case 2: B=1 and A=C=D=0:

The voltage across R1/2 is 5V. So, the current through R1/2 is IB=1mA. Since the current into the op-amp input terminals are negligible, this 1mA current will flow through the RF resistance. Hence, the voltage across the resistance RF is,

$$V_{RF} = 1mA * 1K = 1V$$

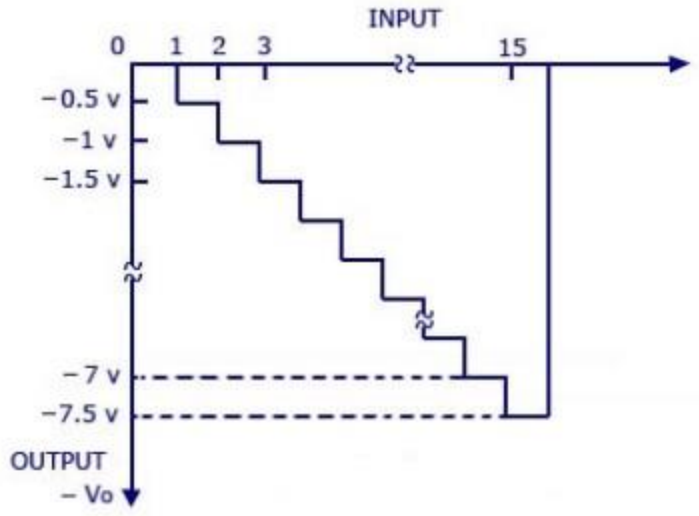
Consequently, the output voltage is at -1V.

Case 3: A=B=1 and C=D=0:

The voltage across R1 is 5V and the voltage across R1/2 is 5V. The current through R1 is IA=0.5mA and the current through R1/2 is IB=1mA. So, the total current through the resistance RF is 1.5mA. Hence, the voltage across the resistance RF is,

$$V_{RF} = 1.5mA * 1K = 1.5V$$

Similarly, consider other cases where all possible cases are experimented. The output voltage levels corresponding to input voltage levels are varying as in the figure.

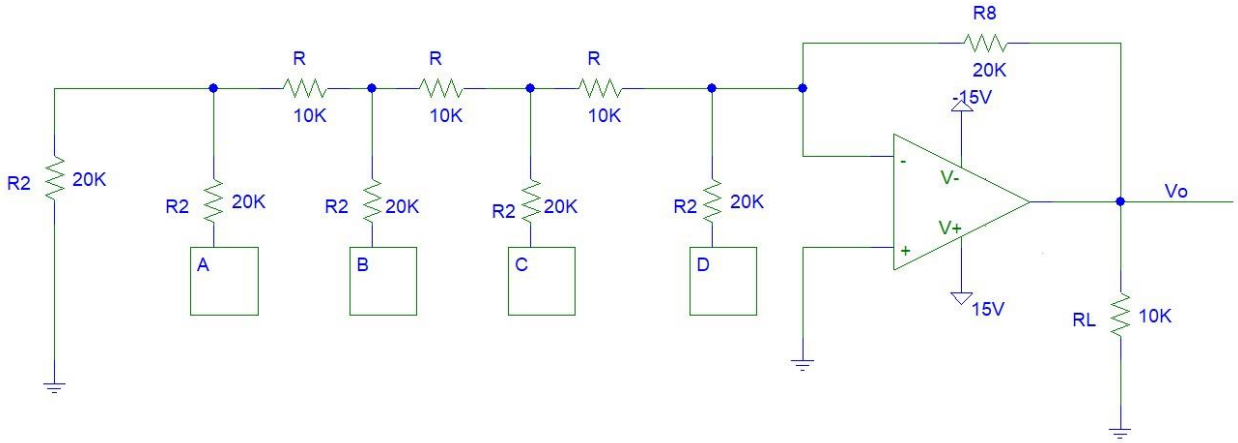


The output is a negative going staircase waveform with 15 steps of -0.5V each. In practice, due to the variations in the logic HIGH voltage levels, all the steps will not have the same size. The value of the feedback resistor RF changes the size of the steps. Thus, a desired size for a step can be obtained by connecting the appropriate feedback resistor. The only condition to look out for is that the maximum output voltage should not exceed the saturation levels of the op-amp.

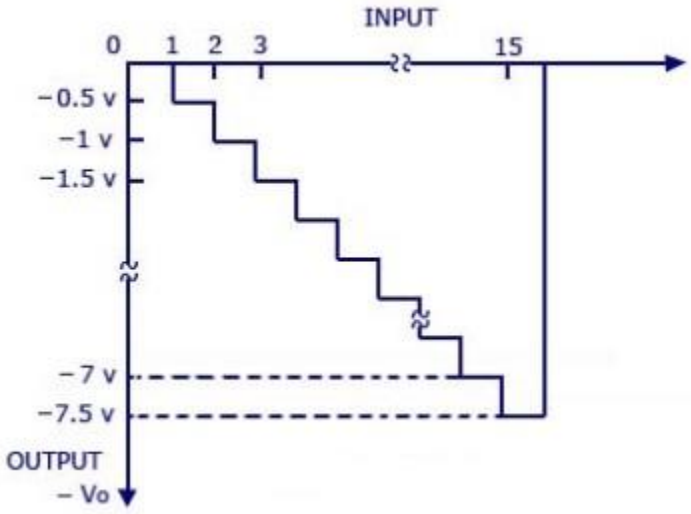
Circuit Diagram 2:

Digital to Analog Converter with R and 2R Resistors

A D/A converter with R and 2R resistors is shown in the figure below. As in the binary-weighted resistors method, the binary inputs are simulated by the switches A-D and the output is proportional to the binary inputs. Binary inputs can be either in the HIGH (+5V) or LOW (0V) state.



The circuit can be solved using thevenin theorem. The graph with the analog outputs versus possible combinations of inputs is shown below.



Procedure:

1. Construct the circuits on the Proteus. Supply +15V and –15V to the opamp.
2. The High input is 5V and the low input is 0V.
3. Use multimeter to measure the output magnitude varied with the input signals. This is the analog signal output. Make a table and take data for all possible combinations.

Report:

1. Explain how you get the analog output voltage of R2R D2A converters. Select one dataentry and validate the data with necessary circuits and calculations.

2. What will be the analog output for the above circuit (you can use either of the D2Aconverters) if the high input voltage is the sum of the last two digits of your Student ID number and the low input is zero? Draw a table and fill up it for all possible input combinations. (If your last two digits are zero, then use the first two digits)

3. Find the full step output and resolution for both D2A converters.

4. What happens to the step size if we increase or decrease the value of RF (feedbackresistance)?

5. How can you get output lower than -15V in the above D2A converters?

(reports must include input output graphs of both D2A converters)

Datasheet for circuit 1:

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Input Configuration	D	C	B	A	Output Voltage, Vo (V)
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					

Datasheet for circuit 2:

Input Configuration	D	C	B	A	Output Voltage, Vo (V)
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					