

CSE350
Digital Electronics & Pulse Techniques
Summer 2022

Final Exam Review
Week-4, 5, 6, 7 and 8

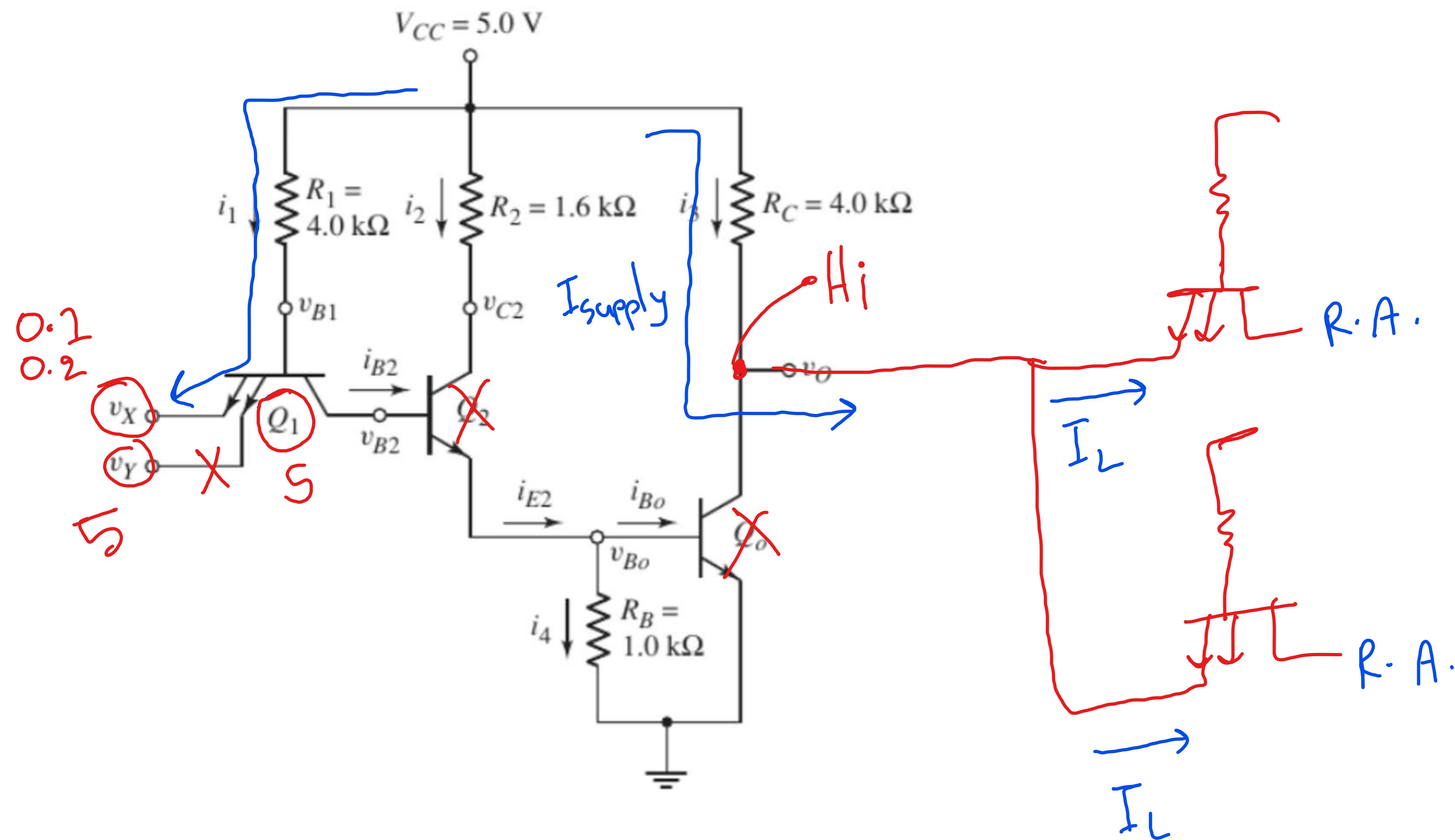
Note: I may have missed some topics/circuits. Please study all the examples and topics in Class Lectures and BUX HomeWorks

Week-4

TTL Circuits

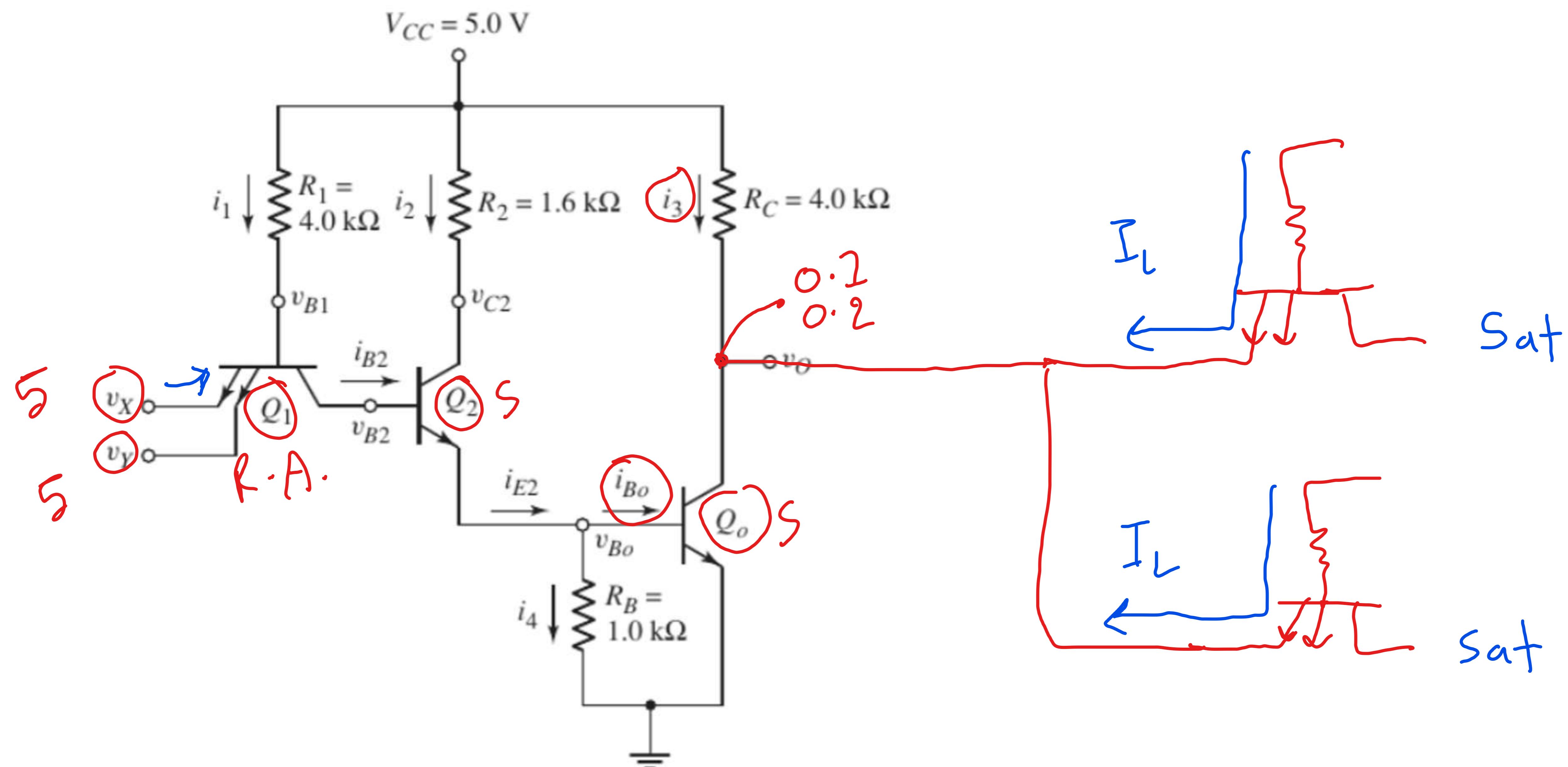
Basic TTL NAND Gate

Case 01: At least one input Low



$$\text{Fanout} \rightarrow I_{\text{Supply}} = N * I_L$$

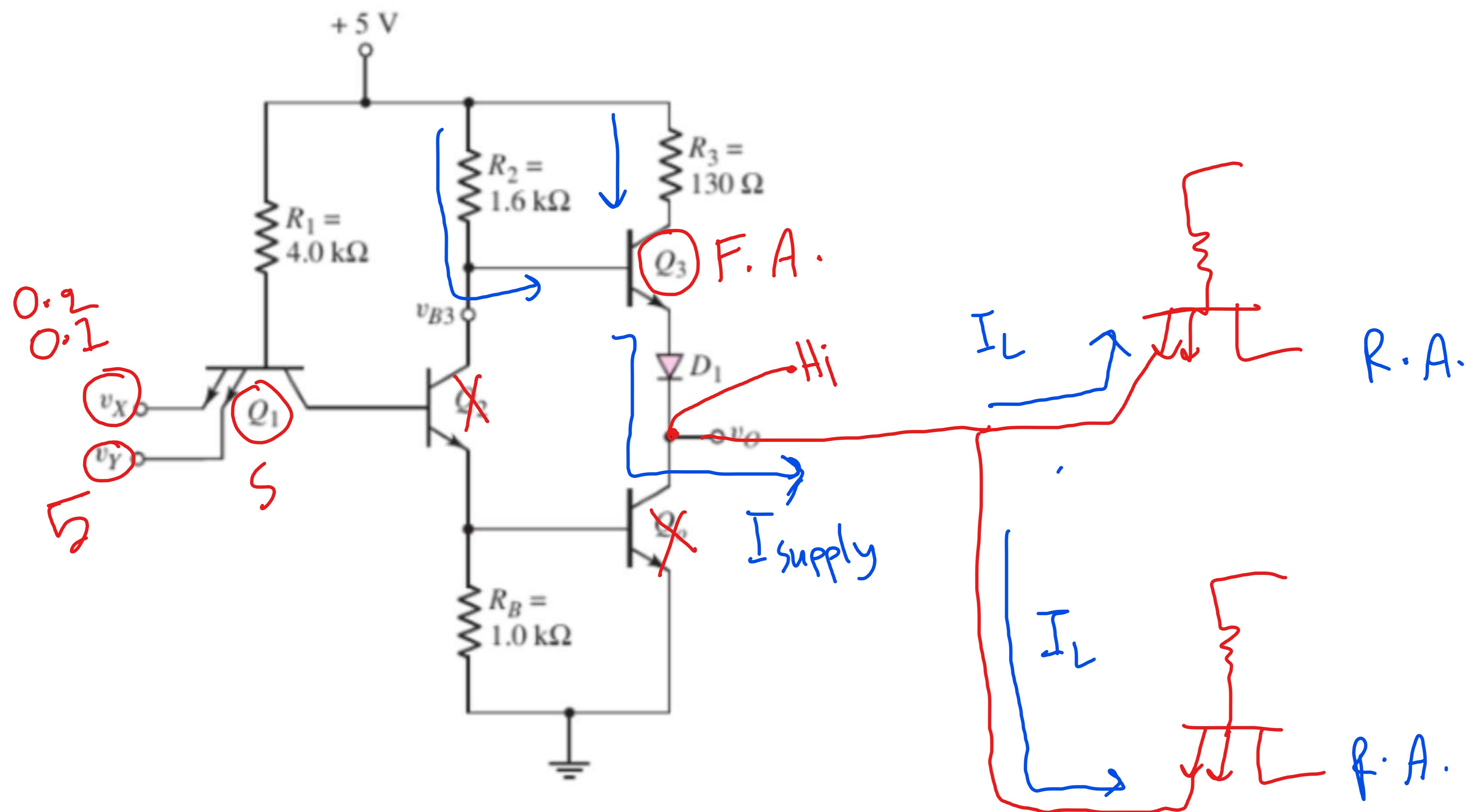
Case 02: All inputs High



$$\text{Fanout} \rightarrow I_3 + N * I_L$$

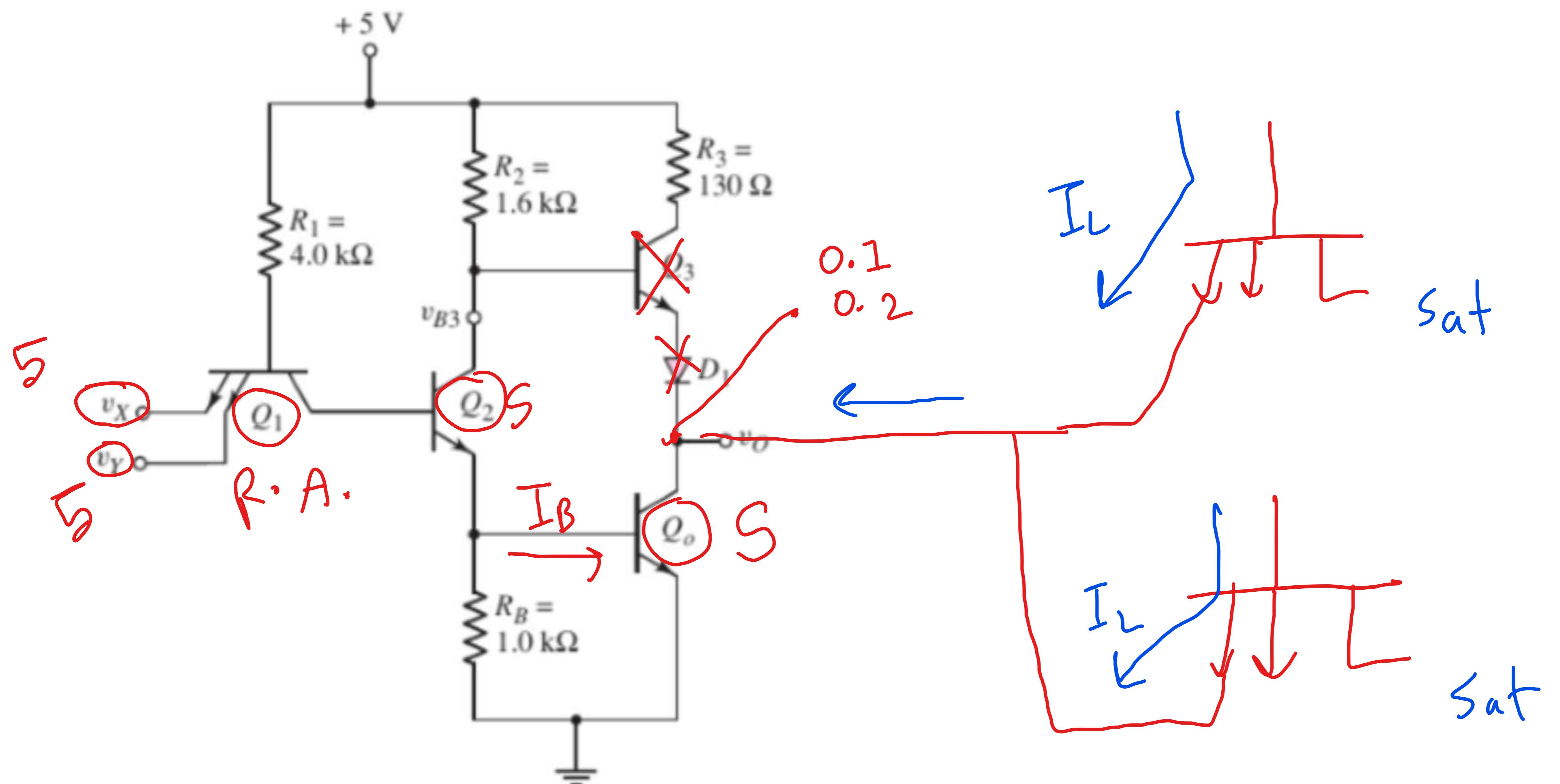
TTL Totem Pole NAND Gate

Case 01: At least one input Low



$$\text{Fanout} \rightarrow I_{\text{Supply}} = N * I_L$$

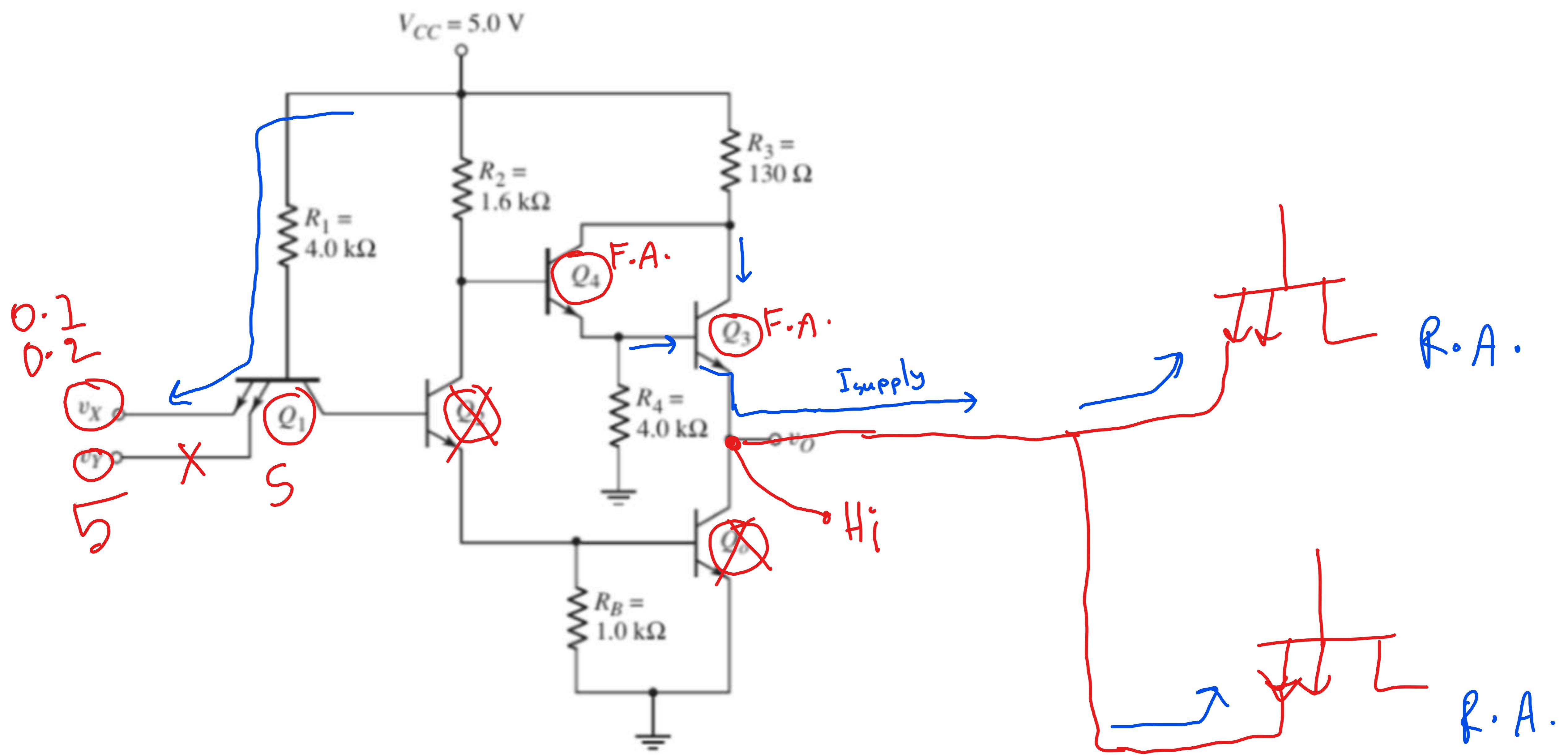
Case 02: All inputs High



$$\text{Fanout} \rightarrow \frac{N * I_L}{I_B} < \beta_F$$

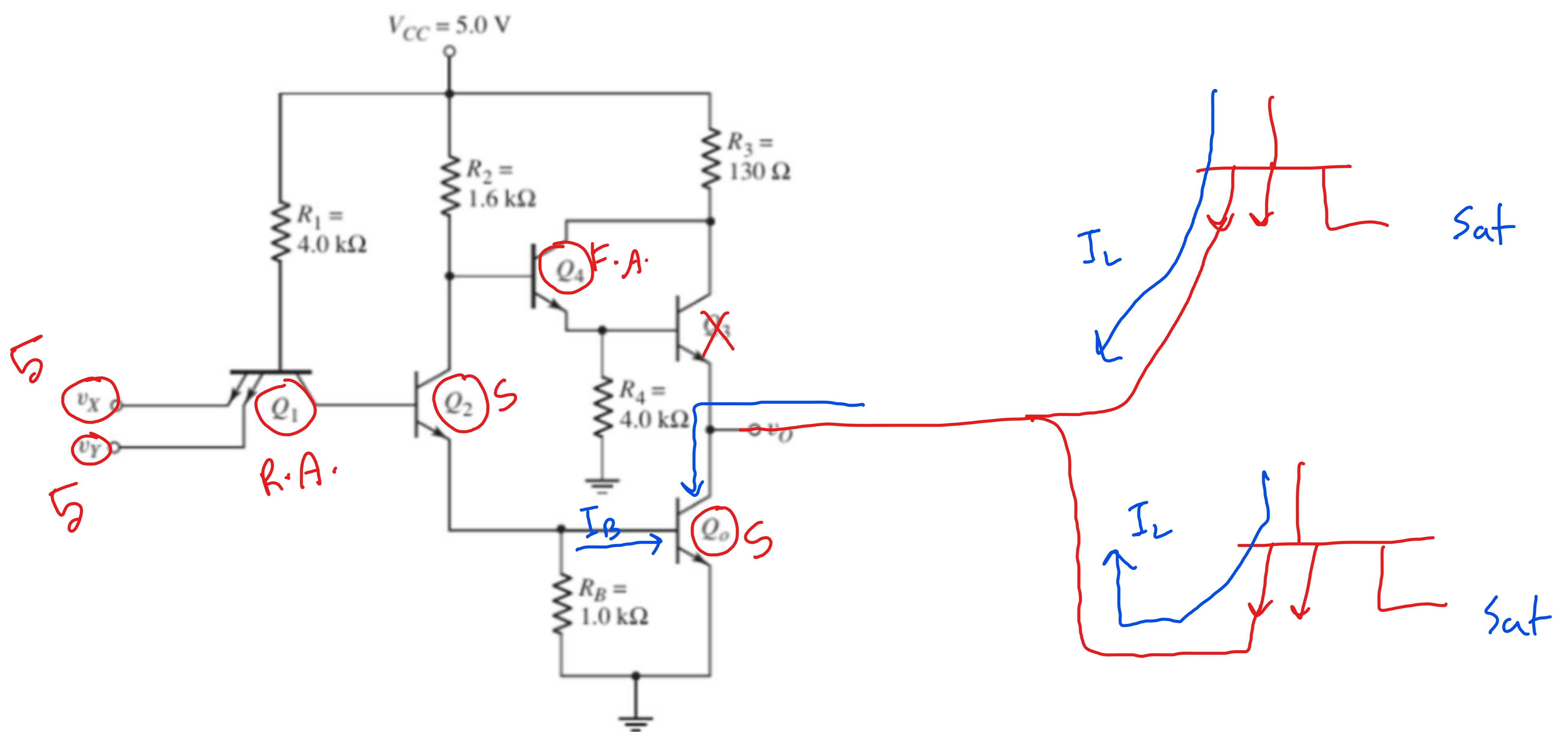
Modified Totem Pole NAND Gate

Case 01: At least one input Low



$$\text{Fanout} \rightarrow I_{\text{Supply}} = N * I_L$$

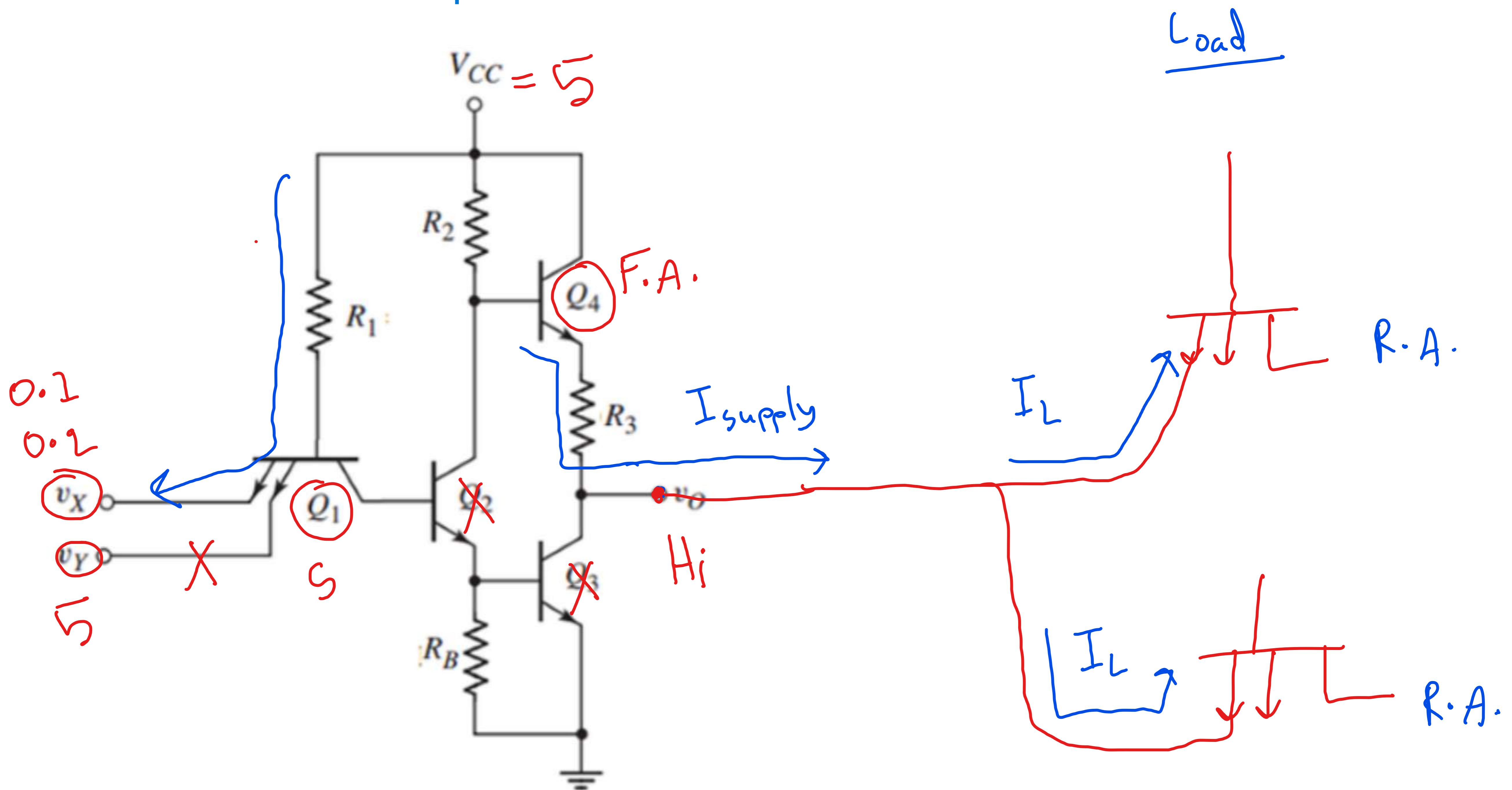
Case 02: All inputs High



$$\text{Fanout} \rightarrow \frac{N * I_L}{I_B} < \beta_F$$

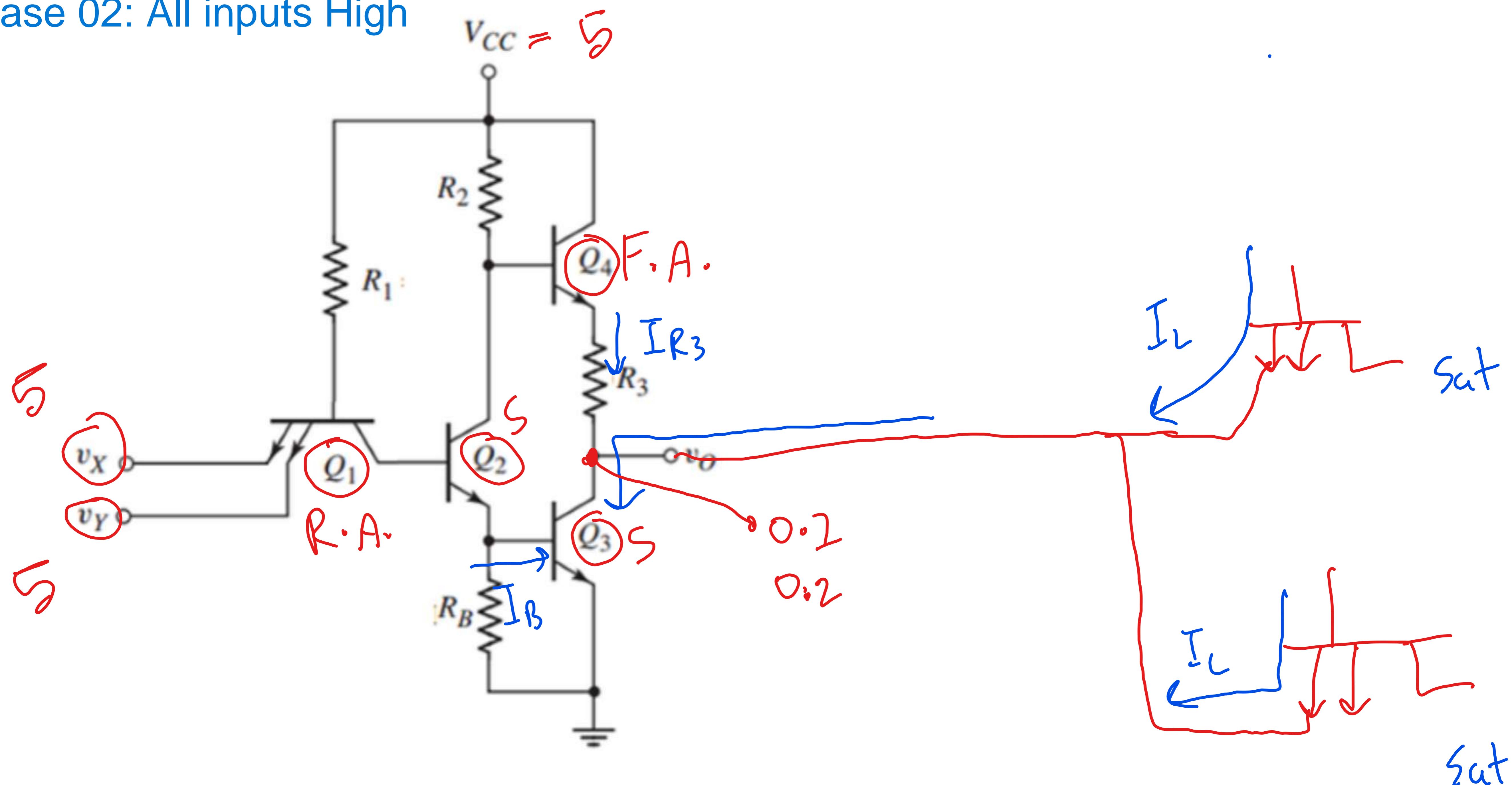
Home Work 4.5

Case 01: At least one input Low



$$\text{Fanout} \rightarrow I_{Supply} = N * I_L$$

Case 02: All inputs High

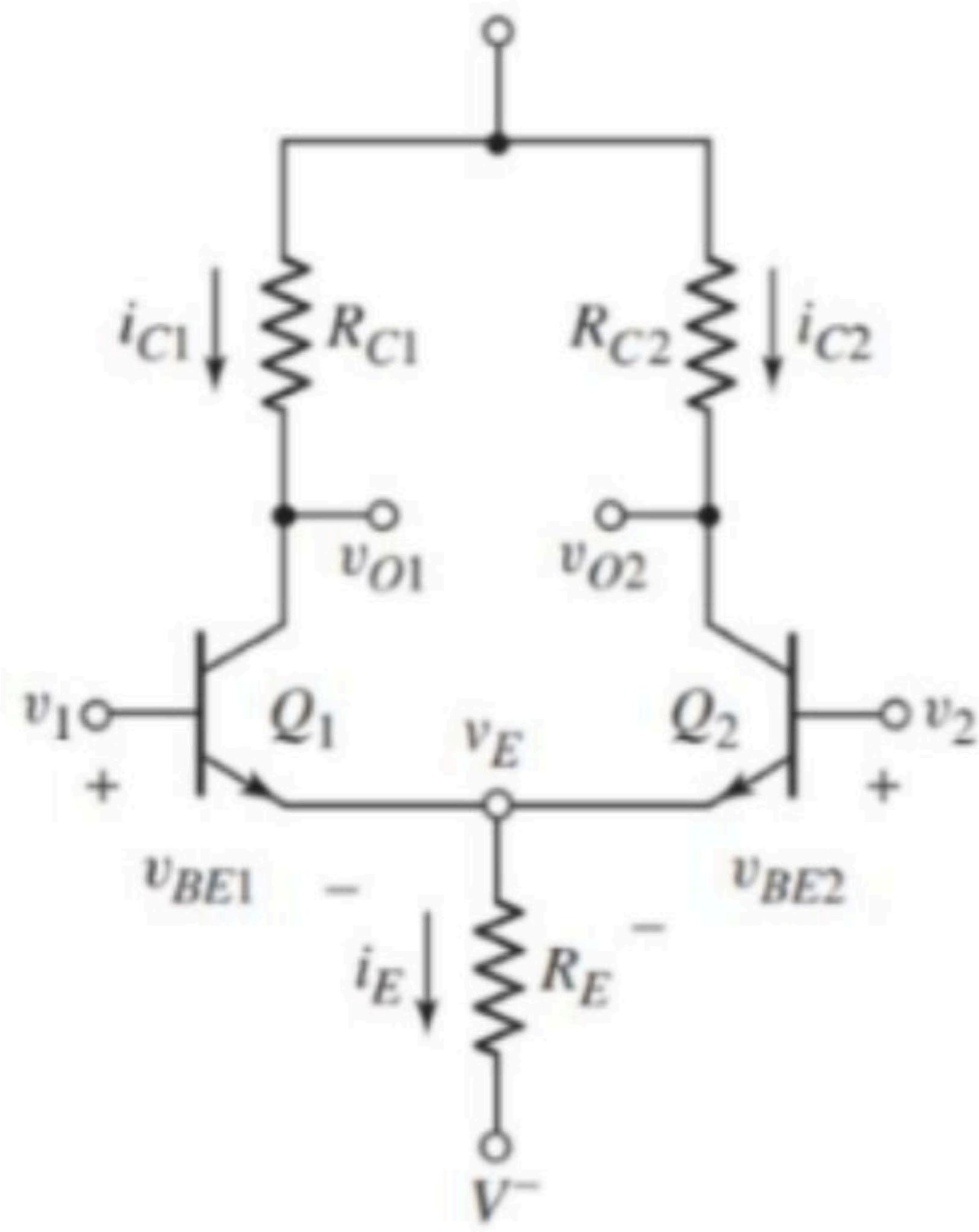


$$\text{Fanout} \rightarrow \frac{I_{R3} + N * I_L}{I_B} < \beta_F$$

Week-5

ECL Circuits

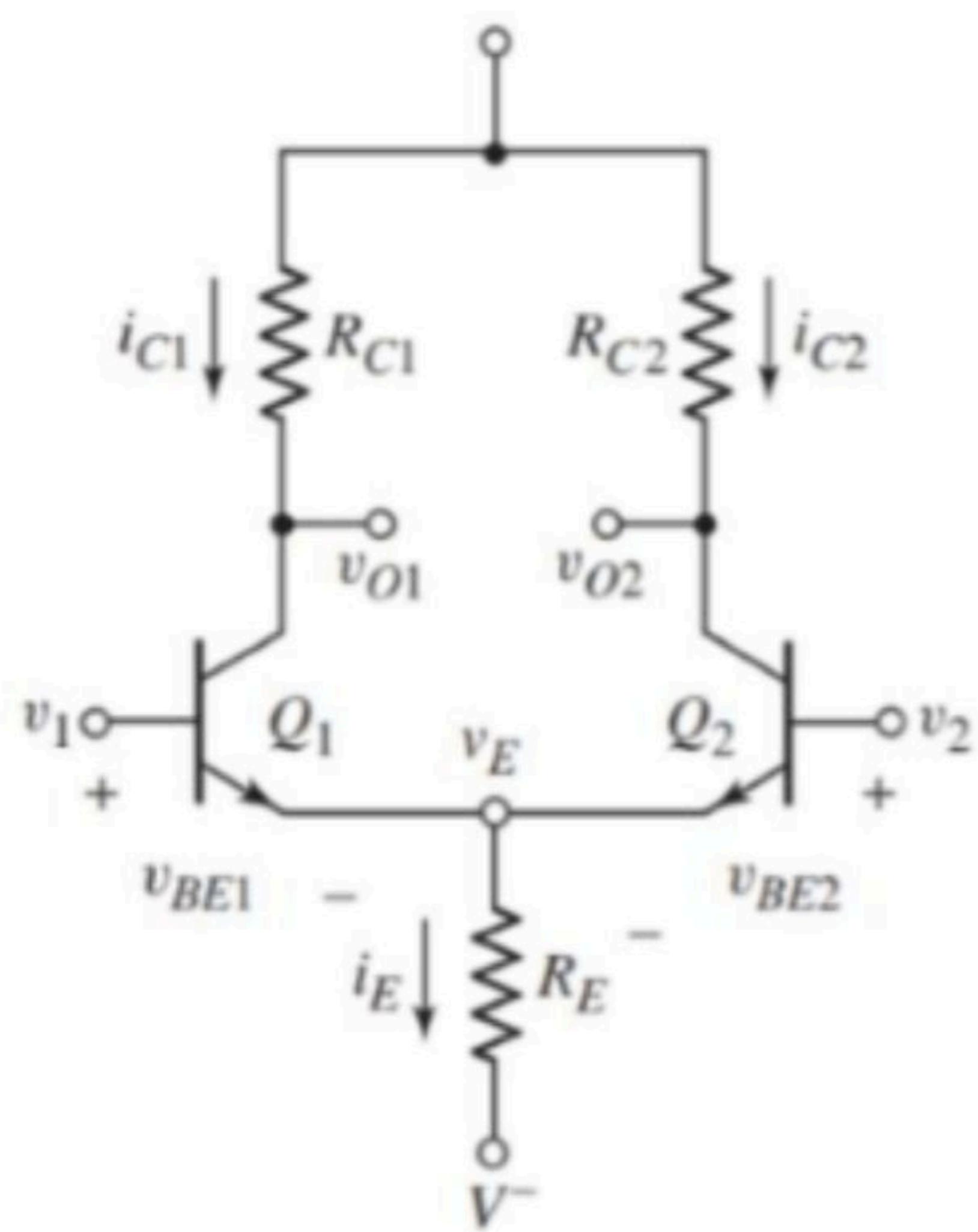
Basic Differential Amplifier



$$V_1 \geq V_2 + 0.12 \rightarrow Q_2 \text{ off}, Q_1 \text{ active}$$

$$V_2 \geq V_1 + 0.12 \rightarrow Q_2 \text{ active}, Q_1 \text{ off}$$

$$|V_1 - V_2| < 0.12 \rightarrow V_1 = V_2 \rightarrow \text{active}$$

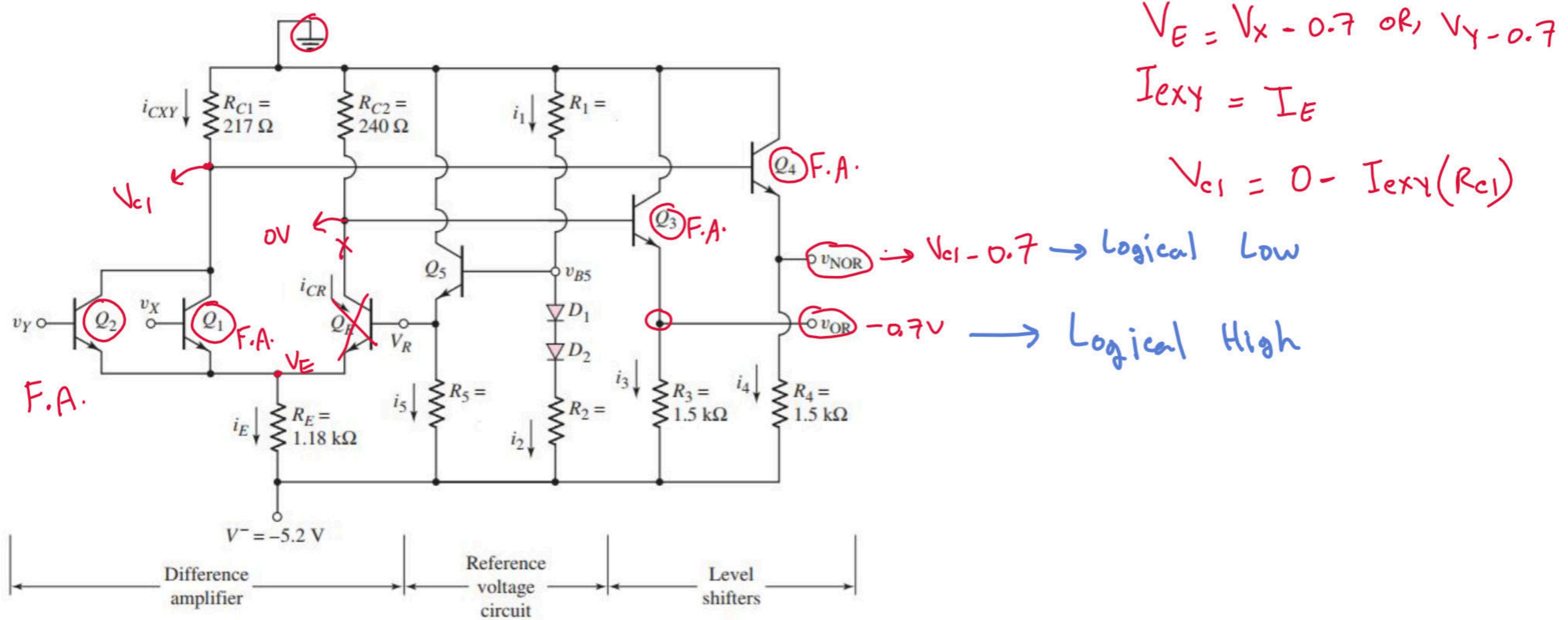


$$I_{C1} = I_{E1} = I_s \exp\left(\frac{V_{BE1}}{V_T}\right)$$

$$I_{C2} = I_{E2} = I_s \exp\left(\frac{V_{BE2}}{V_T}\right)$$

ECL Logic with Reference voltage circuit

Case 1: at least one of V_x, V_y is High

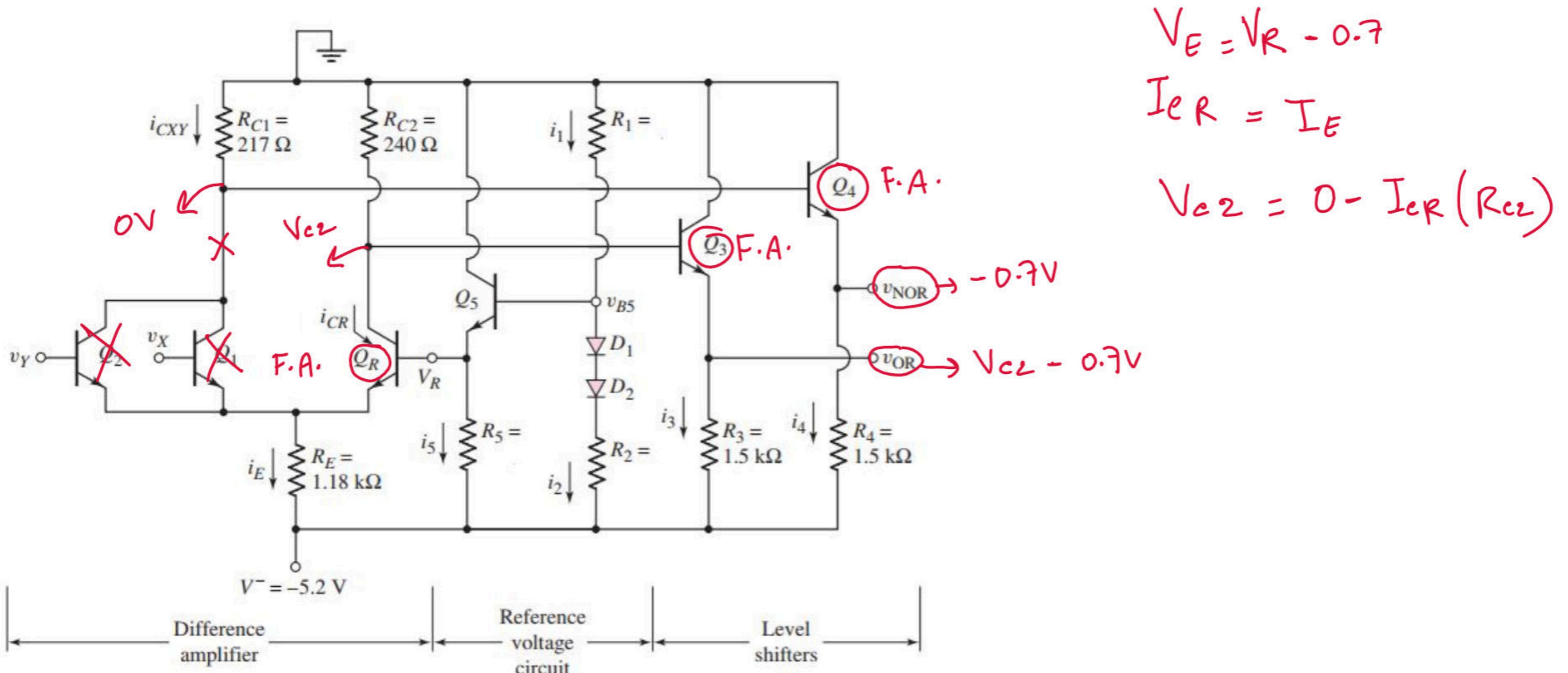


$$0 - \frac{v_{BS}}{R_1} = \frac{V_{BS} - (2 \times 0.7) - (-5.2)}{R_2}$$

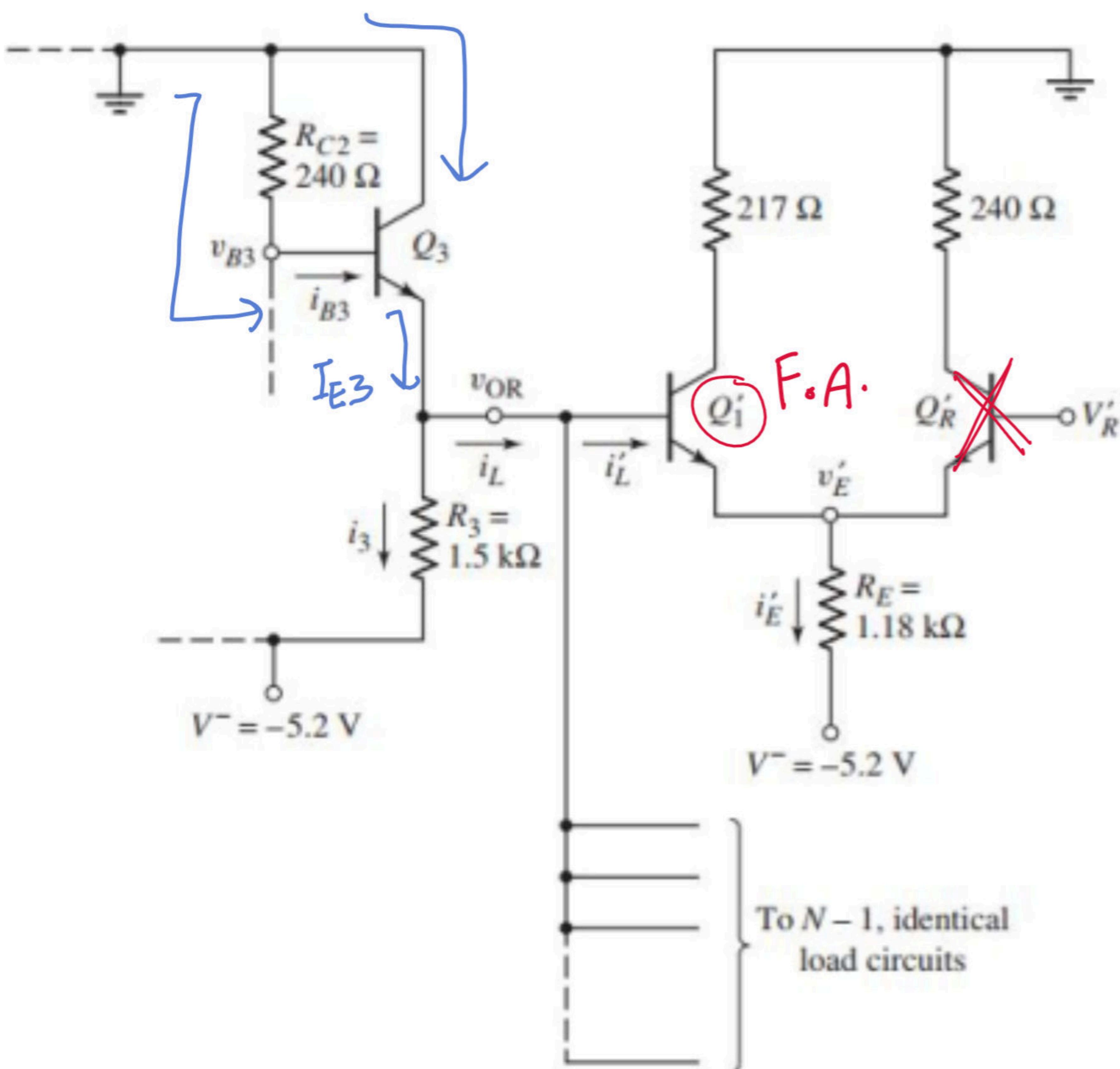
$$v_R = V_{BS} - 0.7$$

Q_5 Always in F.A. mode

Case 2: Both V_x, V_y Low:



ECL: Fanout Calculation



$$V'_E = V_{OR} - 0.7$$

$$I'_L = \frac{I'_E}{\beta + 1}$$

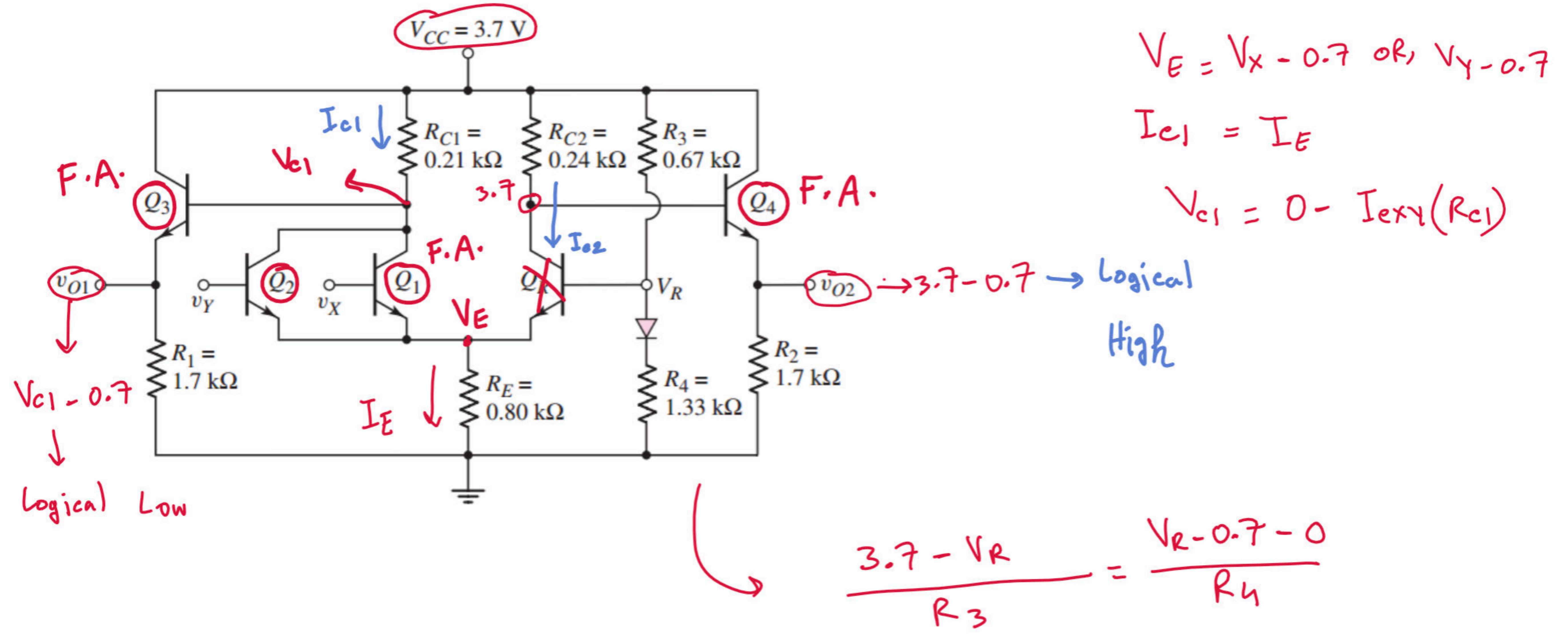
$$I_{E3} = I_{B3} (\beta + 1)$$

$$I_L = I_{E3} - I_3$$

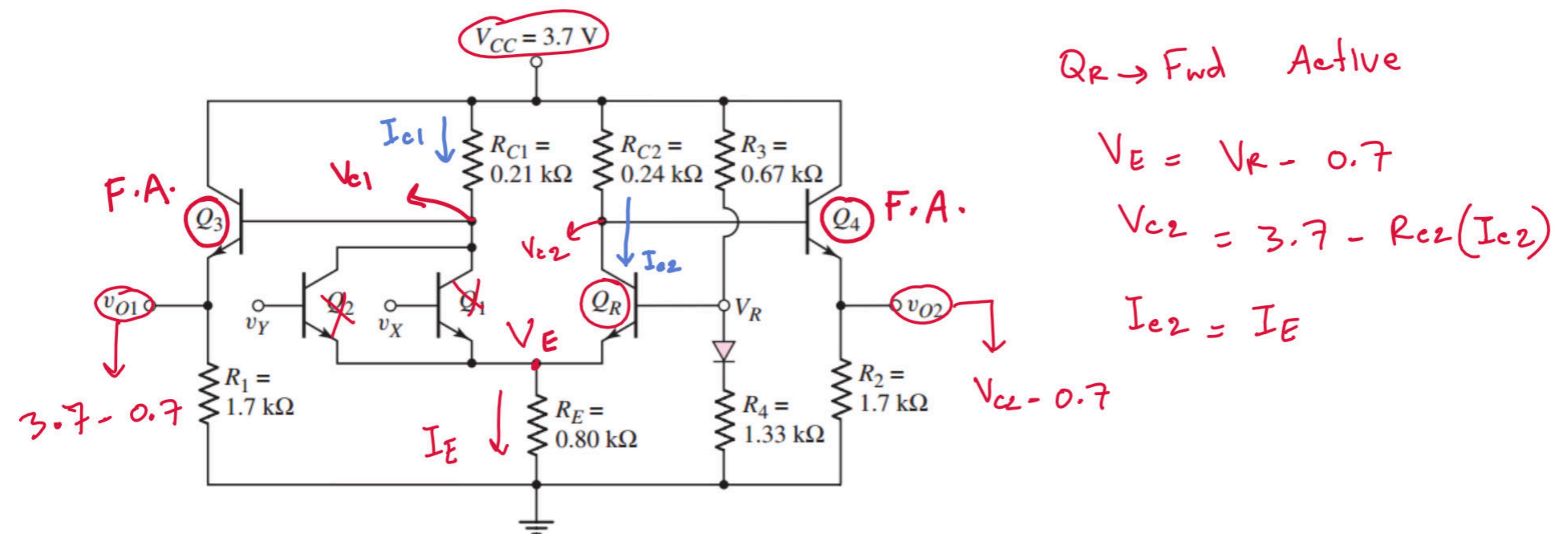
Fanout, $N \rightarrow$ Supply = Demand
 $\hookrightarrow I_L = N I'_L$

HW 5.5.1

Case 1: at least one of V_x , V_y is High



Case 2: Both V_x , V_y Low:

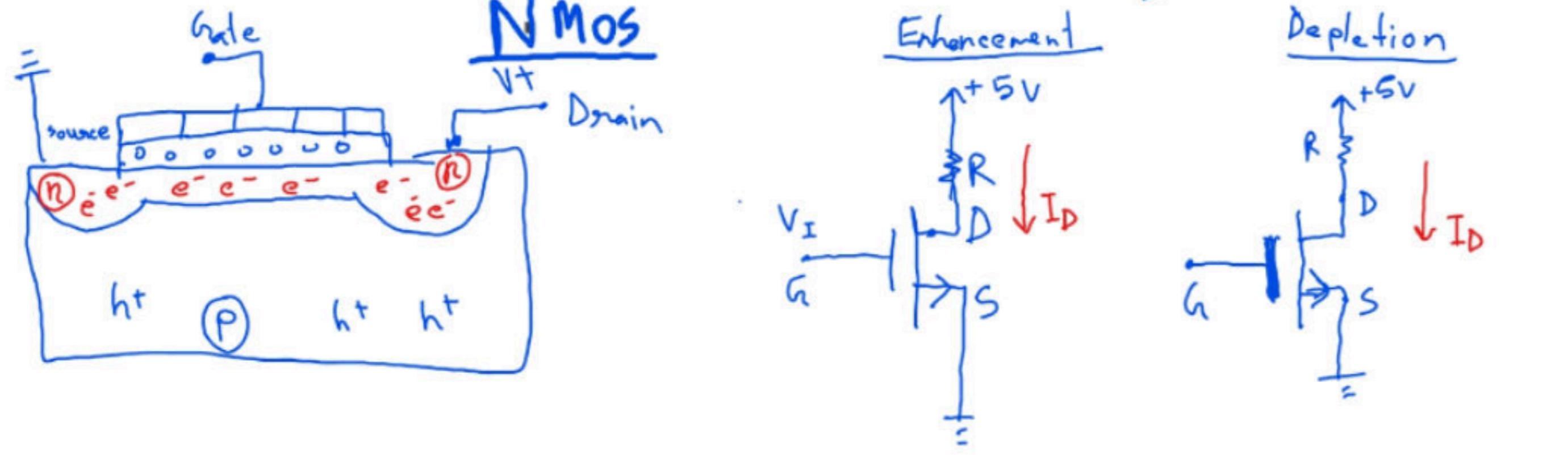


Week-6

Mosfet Logic

Mosfet-1

Basic Operation

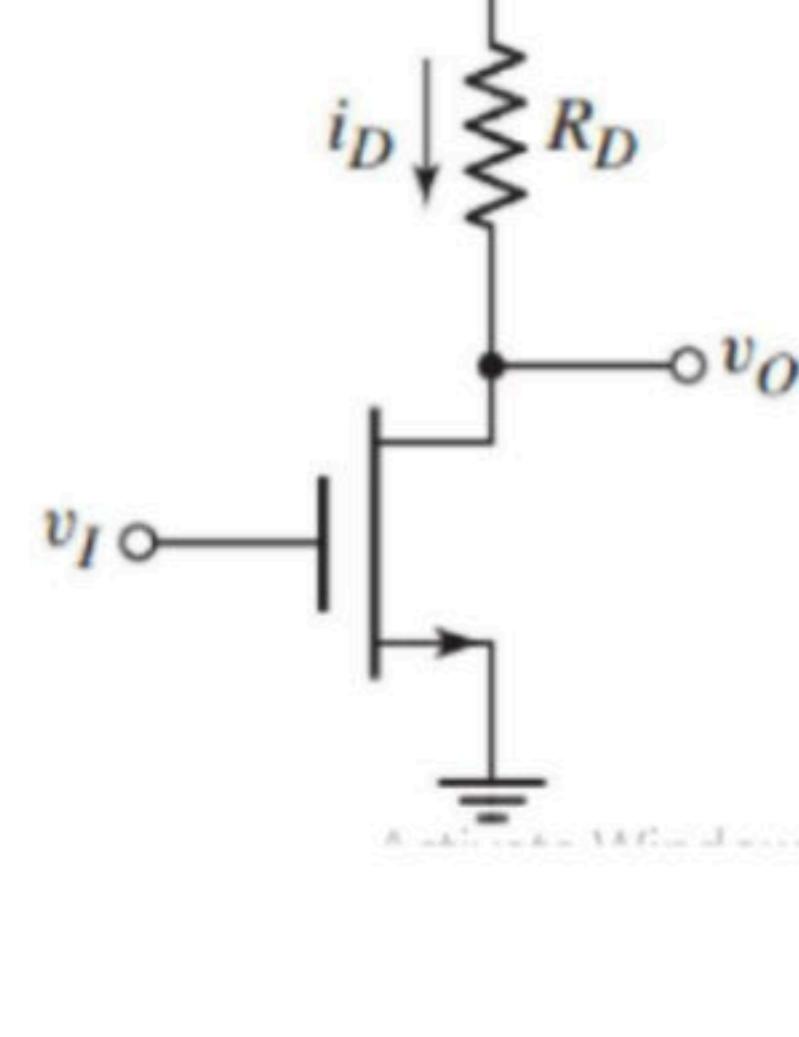


Mode	Formula	Verify/condition
OFF	$I_D = 0$	$V_{GS} < V_{TN}$
ON	$I_D = k_n [2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2]$	$ON \rightarrow V_{GS} \geq V_{TN}$
	$I_D = 0$ (always)	$Triode \rightarrow V_{GD} \geq V_{TN}$ $\therefore V_{DS} \leq V_{GS} - V_{TN}$
Saturation	$I_D = k_n [(V_{GS} - V_{TN})^2]$	$ON \rightarrow V_{GS} \geq V_{TN}$ $Sat \rightarrow V_{GD} < V_{TN}$ $V_{DS} > V_{GS} - V_{TN}$

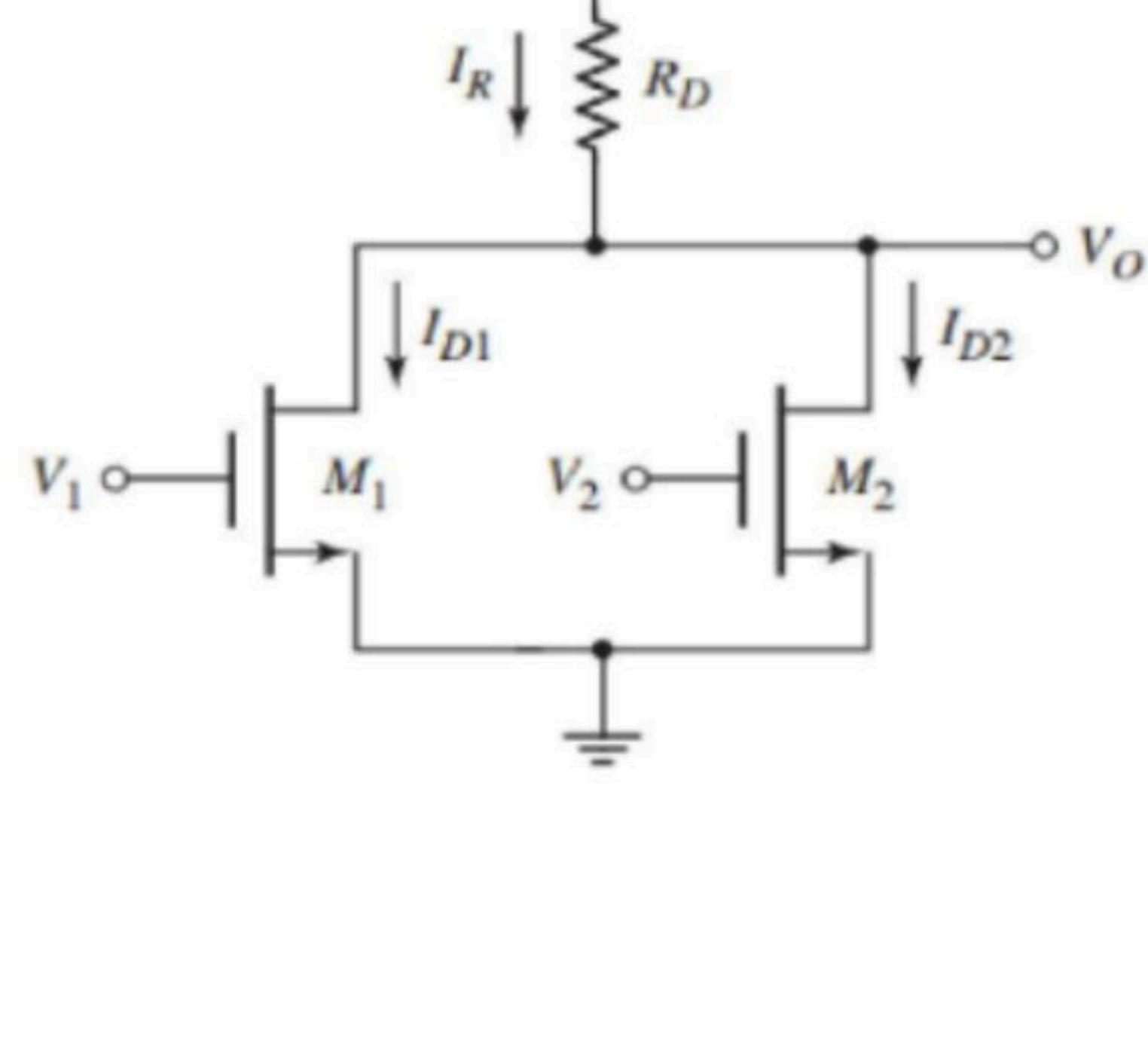
Transition point:
 $V_{DS(Sat)} = V_{GS} - V_{TN}$

NMOS Inverter Example

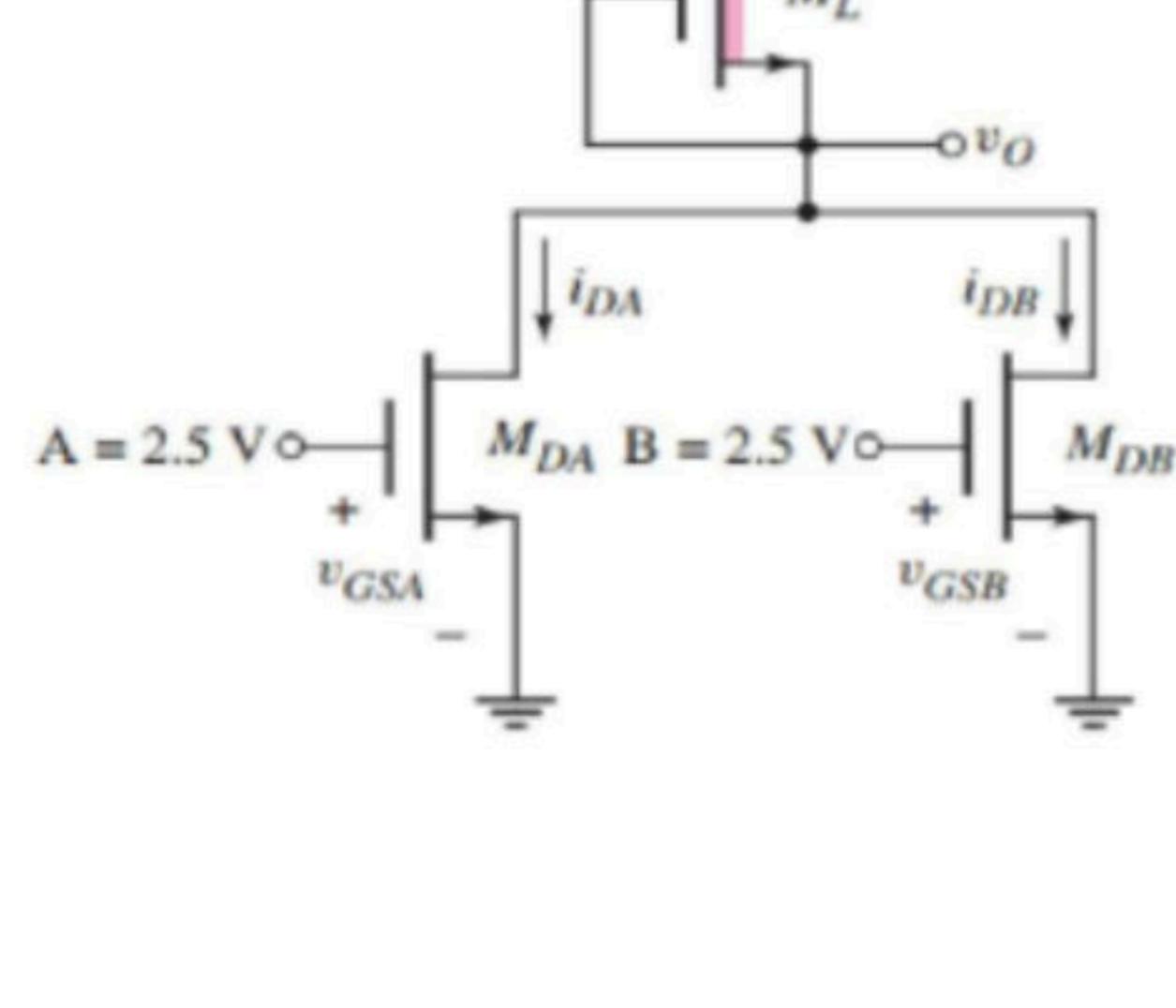
Determine V_0 for $V_I = 5V$ and $V_I = 1.5V$.



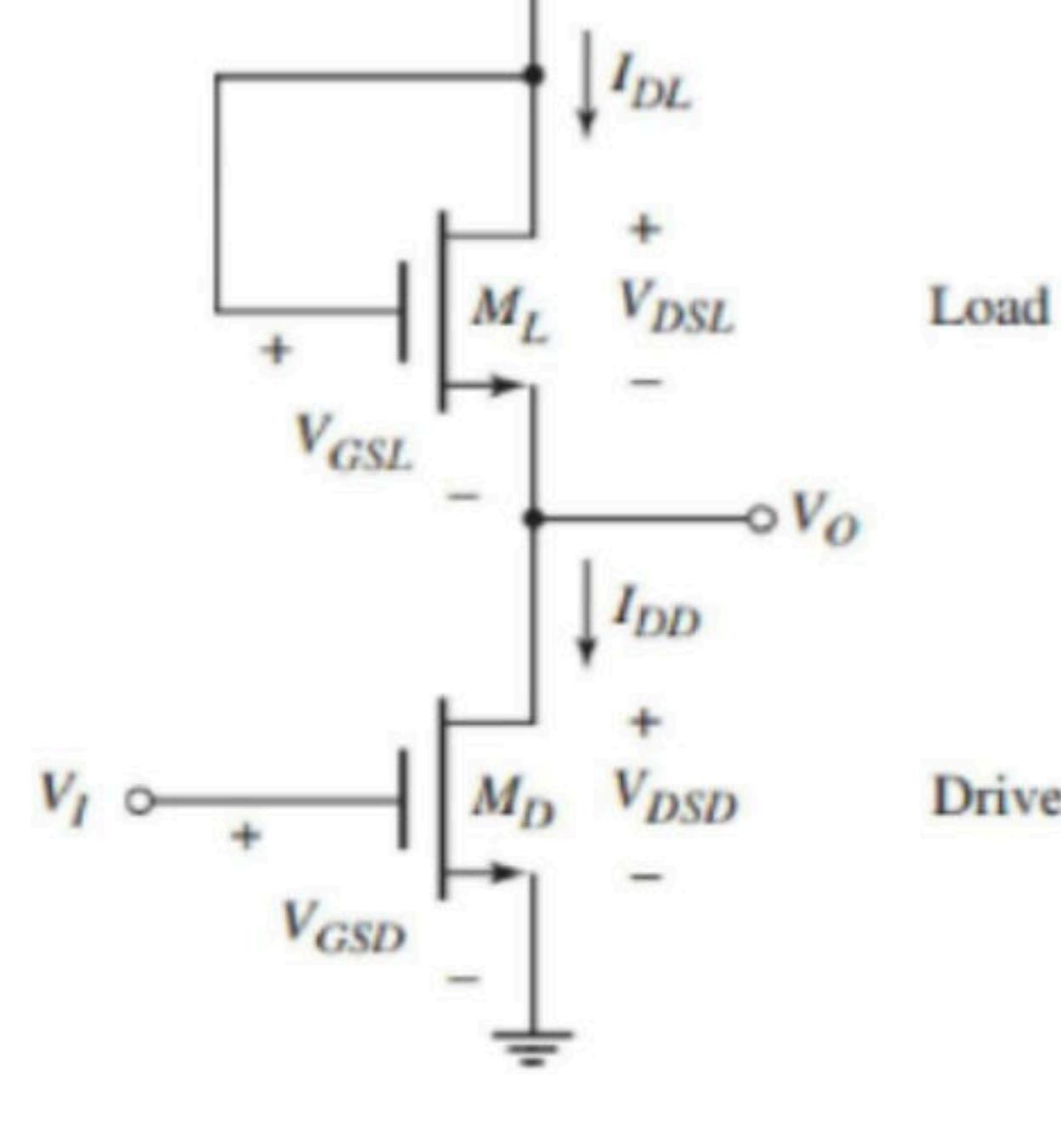
NMOS NOR GATE



NMOS NOR Gate with Depletion Load

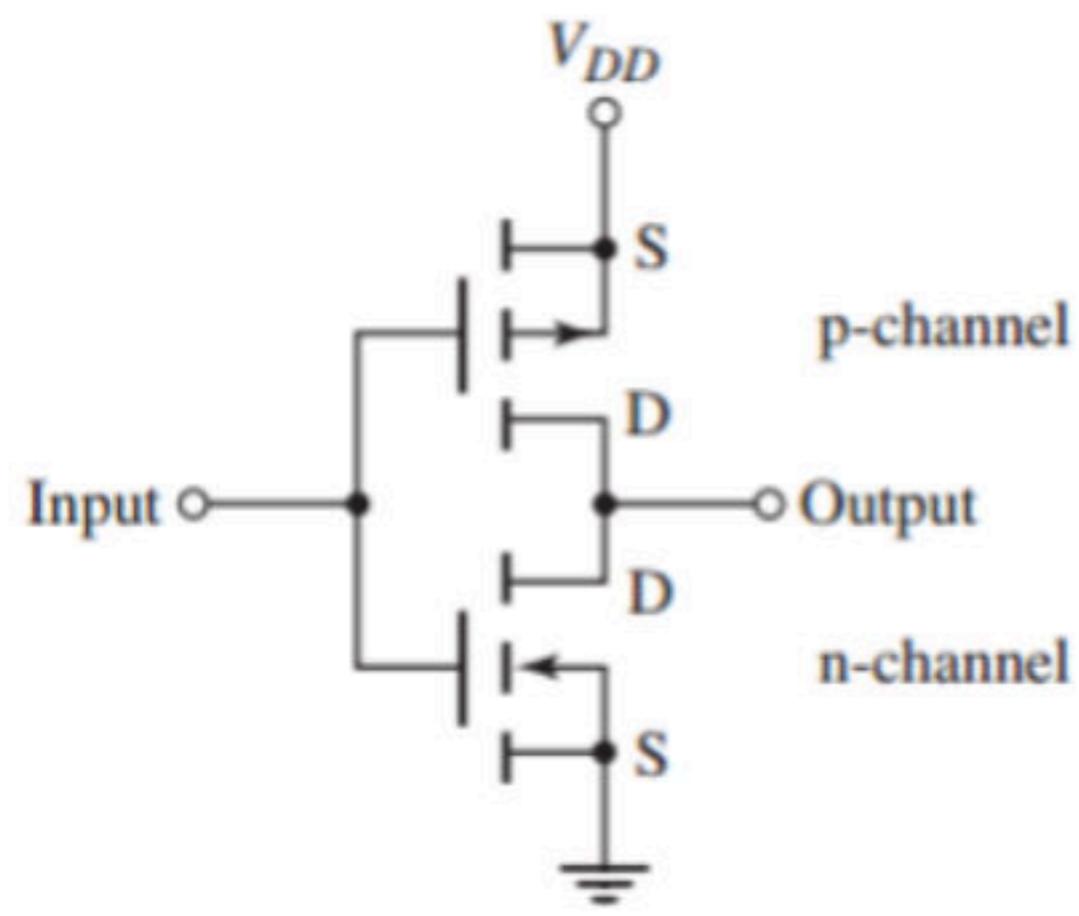


NMOS Inverter with Enhancement Load



Mosfet -2 (CMOS)

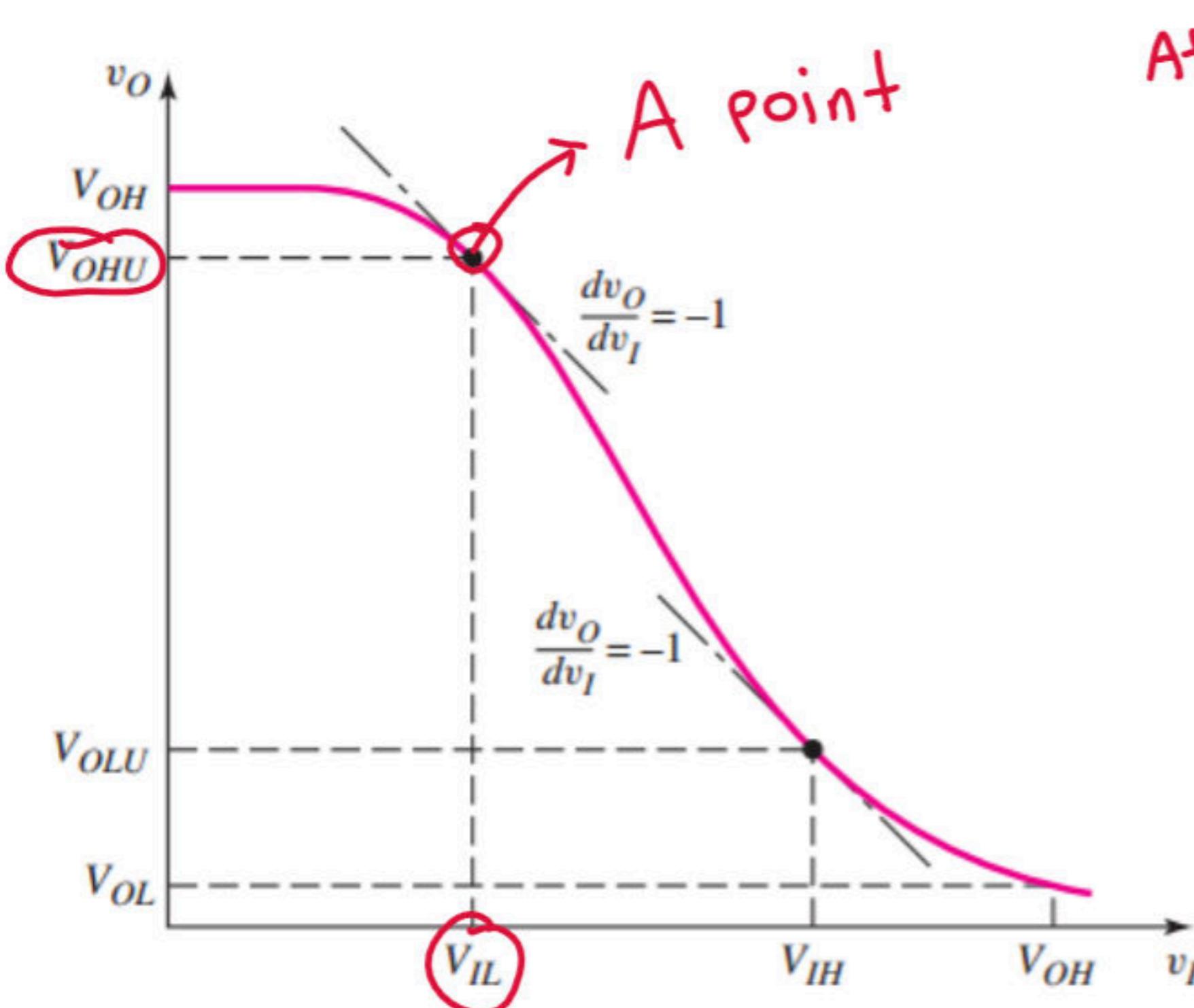
CMOS Inverter Noise Margin Calculation



EXAMPLE 16.9

Objective: Determine the noise margins of a CMOS inverter.

Consider a CMOS inverter biased at $V_{DD} = 3.3$ V. Assume the transistors are matched with $K_n = K_p$ and $V_{TN} = -V_{TP} = 0.4$ V.



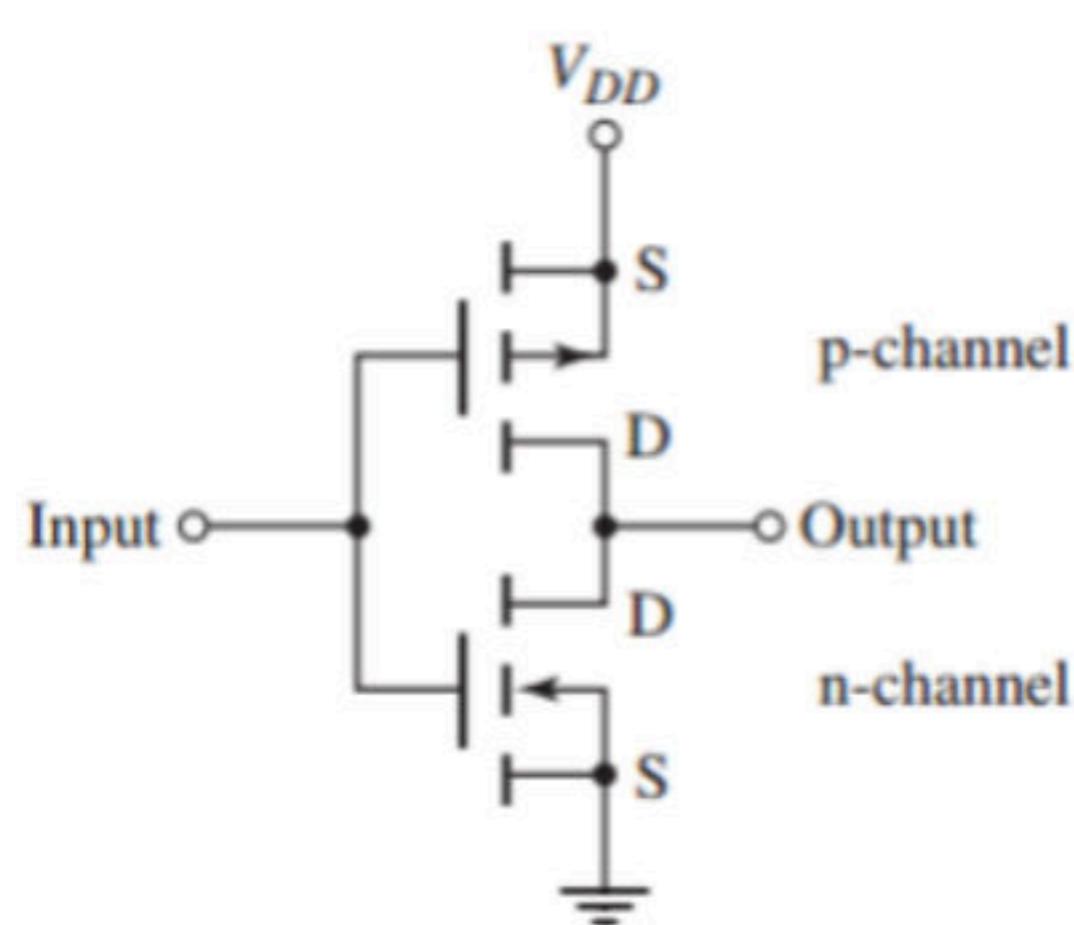
At point A, NMOS in Saturation
PMOS in Triode

Case 1:
 $v_{OHU}, v_{IL} \rightarrow$

$$I_{DP} = I_{DN}$$

$$\rightarrow k_p [2(V_{SDP} - |V_{TP}|) V_{SDP} - V_{SDP}^2] = k_n [V_{DSN} - V_{TN}]^2$$

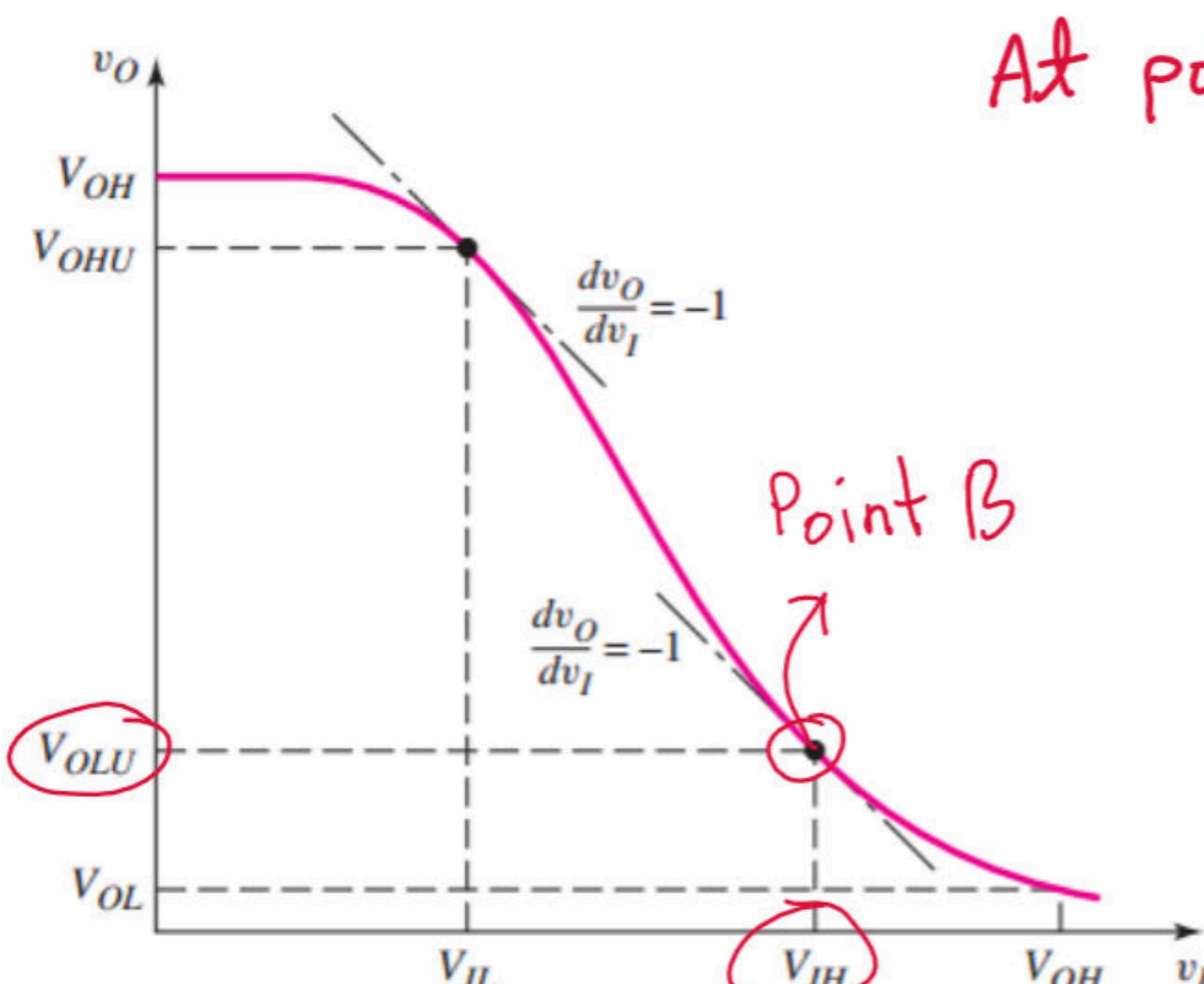
$$\rightarrow 2(3.3 - 0.4)(3.3 - V_o) - (3.3 - V_o)^2 = [V_I - 0.4]^2$$



EXAMPLE 16.9

Objective: Determine the noise margins of a CMOS inverter.

Consider a CMOS inverter biased at $V_{DD} = 3.3$ V. Assume the transistors are matched with $K_n = K_p$ and $V_{TN} = -V_{TP} = 0.4$ V.



At point B, NMOS in Triode
PMOS in Saturation

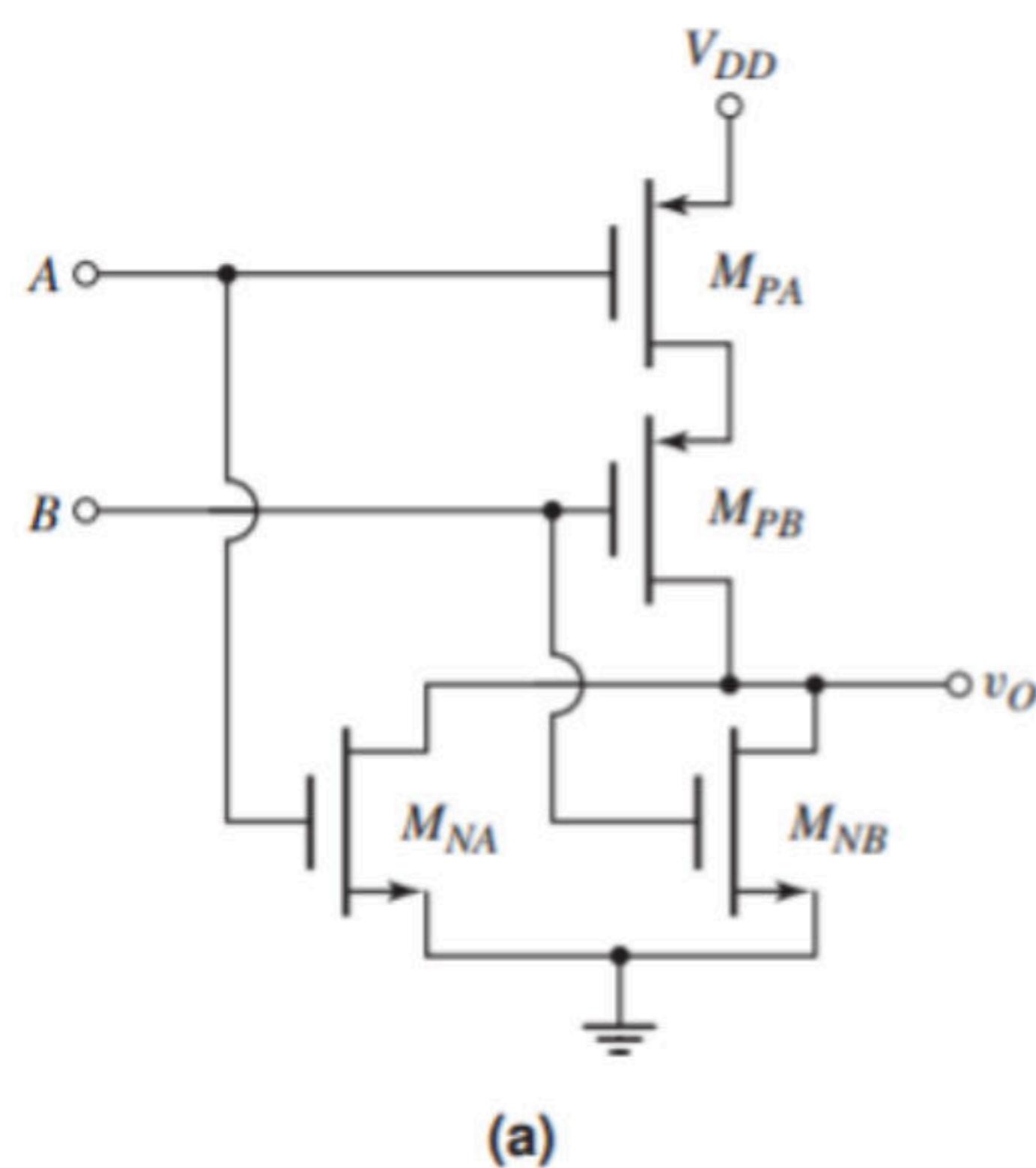
case 2: $v_{OLU}, v_{IH} \rightarrow$

$$I_{DN} = I_{DP}$$

$$\rightarrow k_n [2(V_{DSN} - V_{TN}) V_{DSN} - V_{DSN}^2] = k_p [V_{SDP} - |V_{TP}|]^2$$

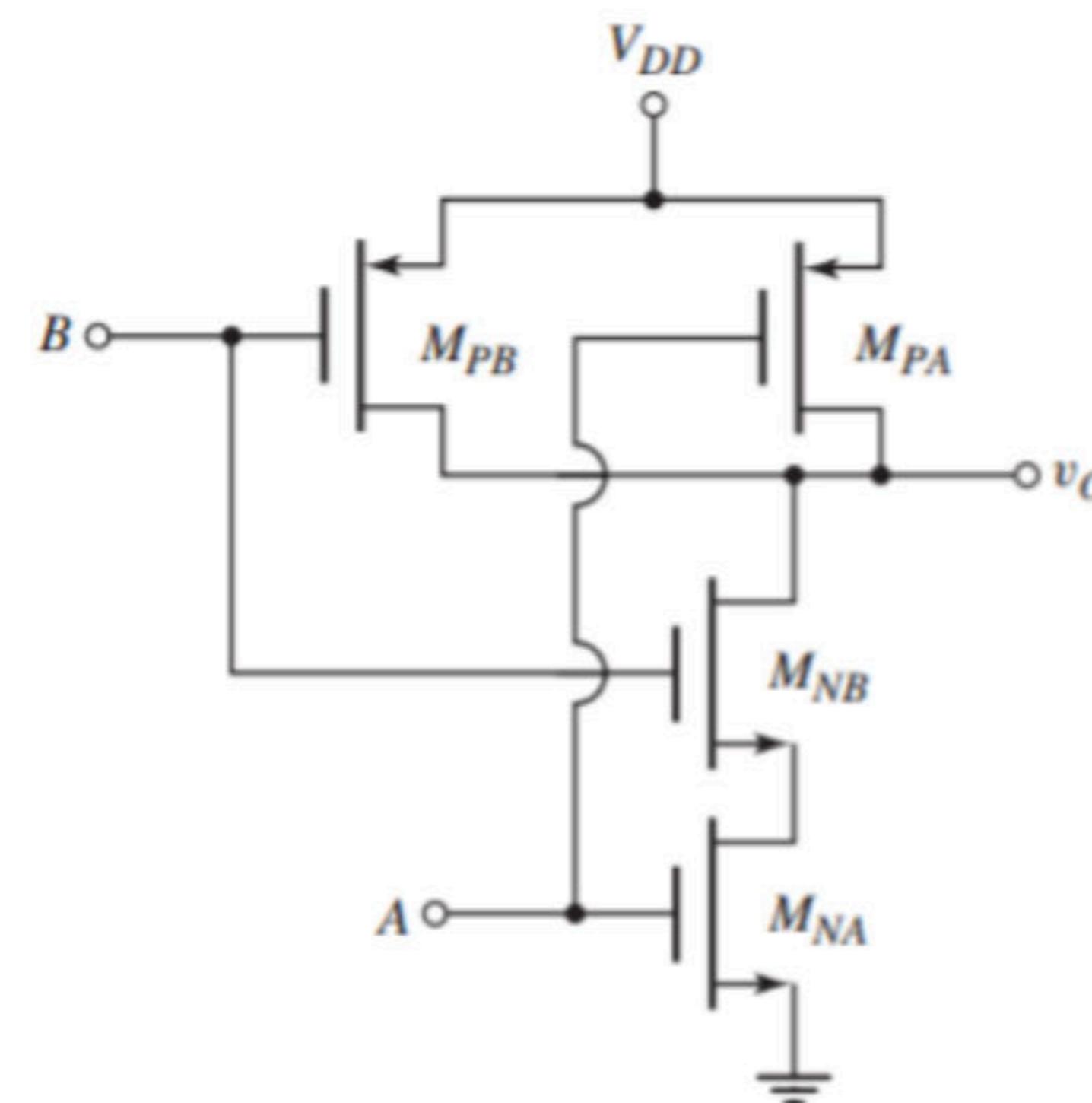
$$\rightarrow 2(V_I - 0.4)V_o - V_o^2 = (3.3 - V_I - 0.4)^2$$

CMOS NAND & NOR GATE



A	B	v_O
0	0	V_{DD}
V_{DD}	0	0
0	V_{DD}	0
V_{DD}	V_{DD}	0

(b)



Complex Logic Functions Using CMOS

DESIGN EXAMPLE 16.11

Objective: Design a CMOS logic circuit to implement a particular logic function.

Implement the logic function $Y = AB + C(D + E)$ in a CMOS design. The signals A, B, C, D , and E are available.

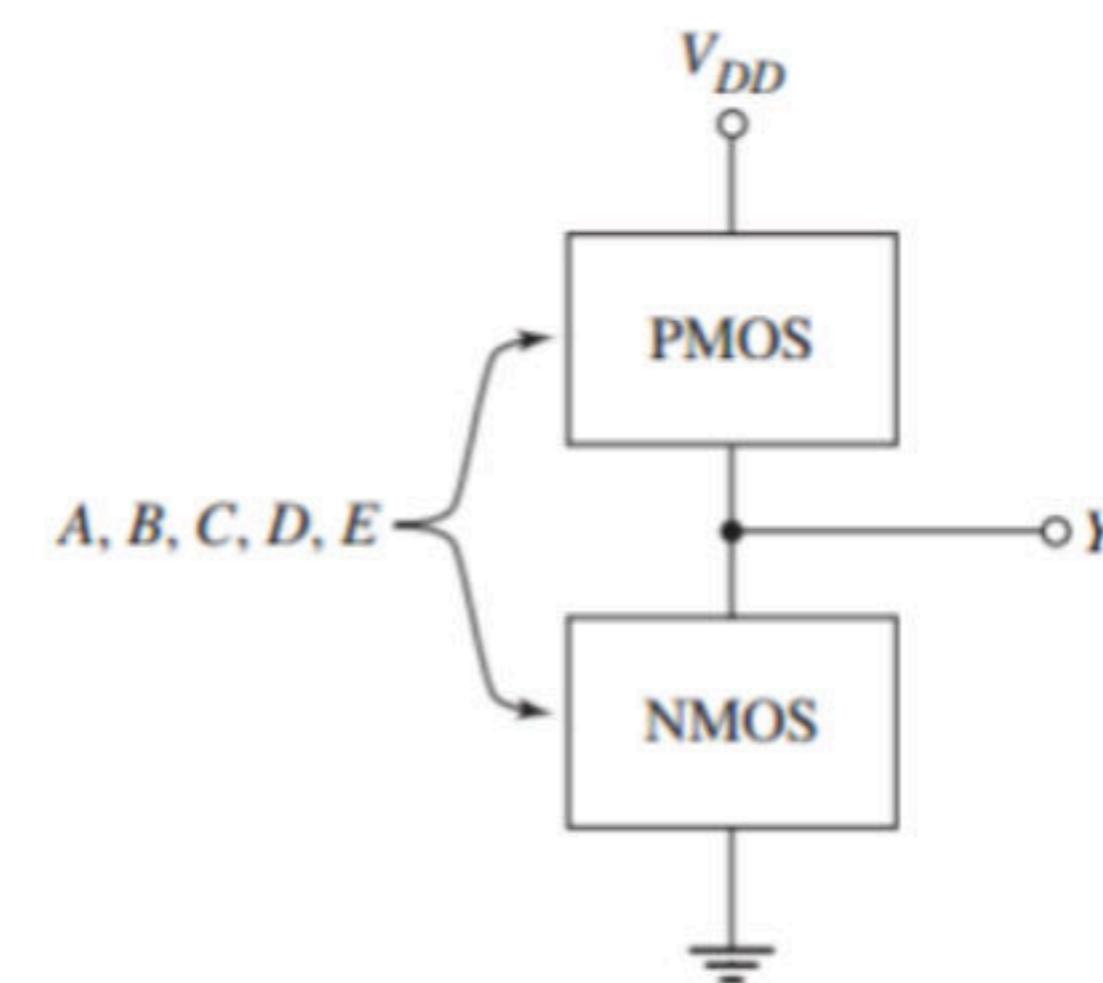
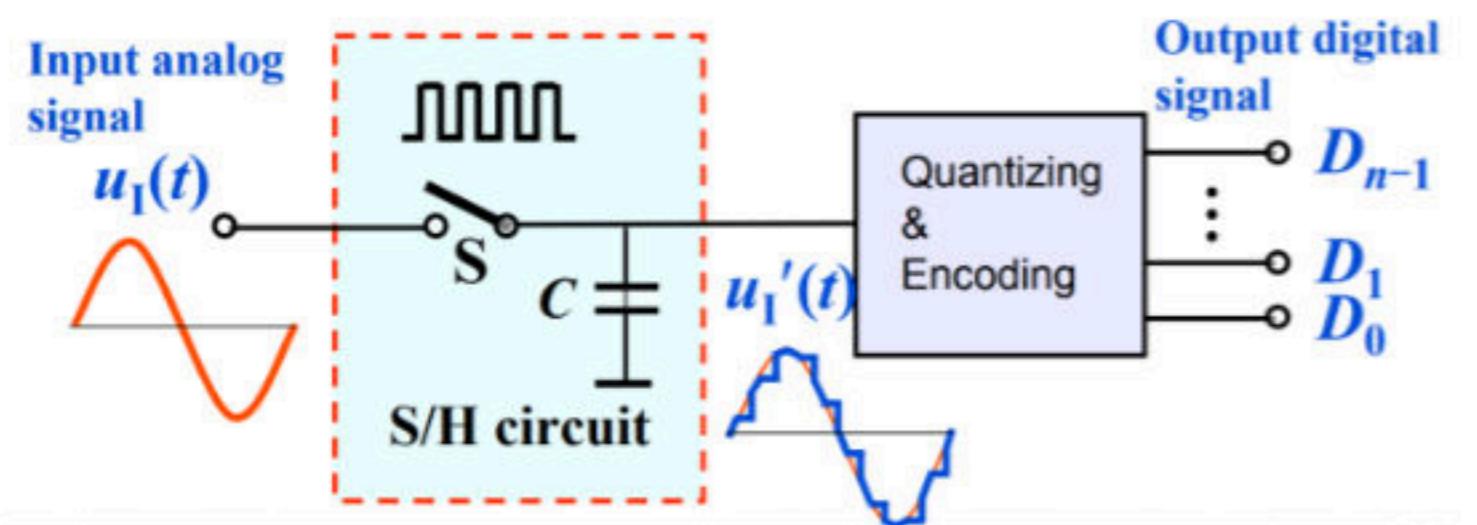


Figure 16.38 General CMOS design

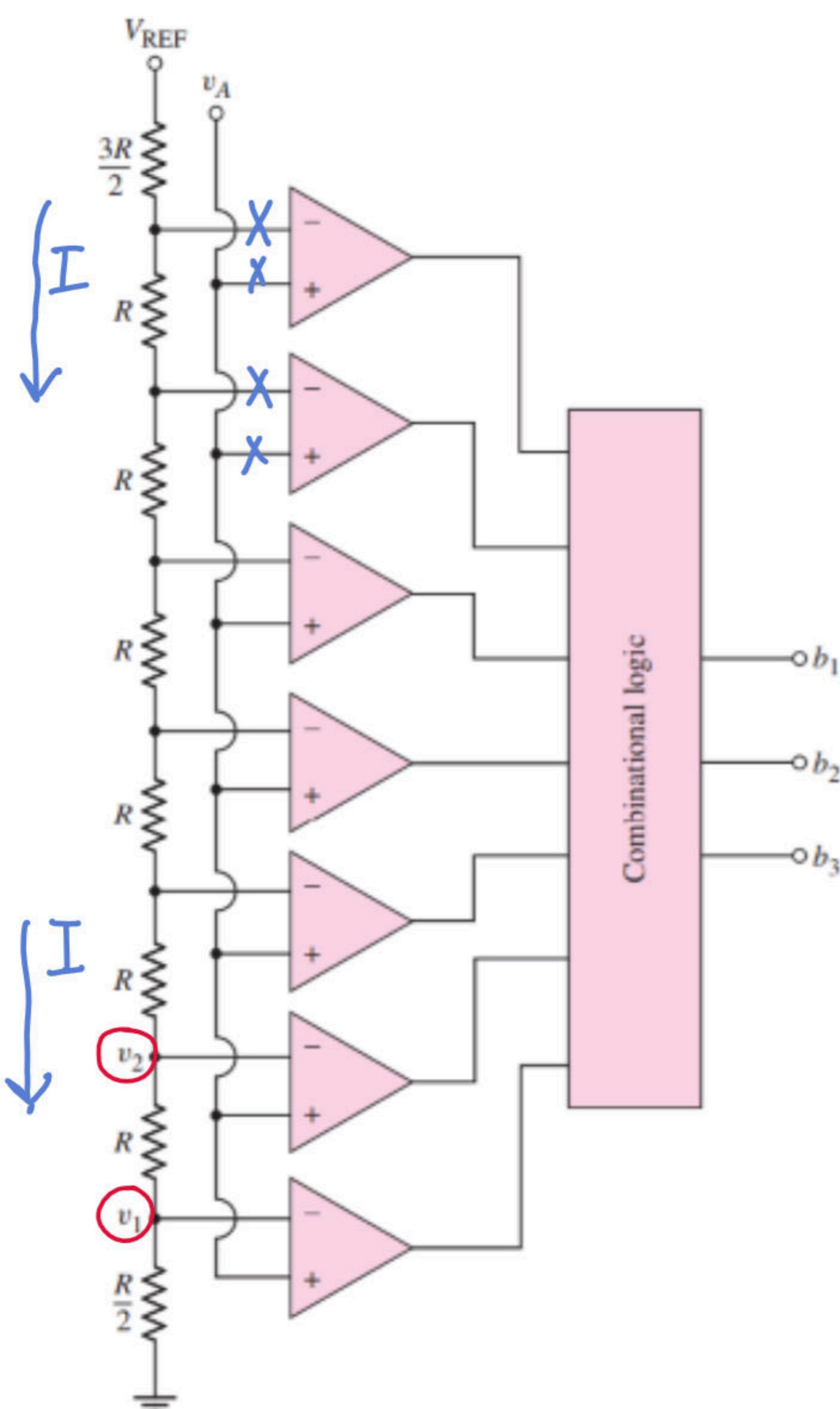
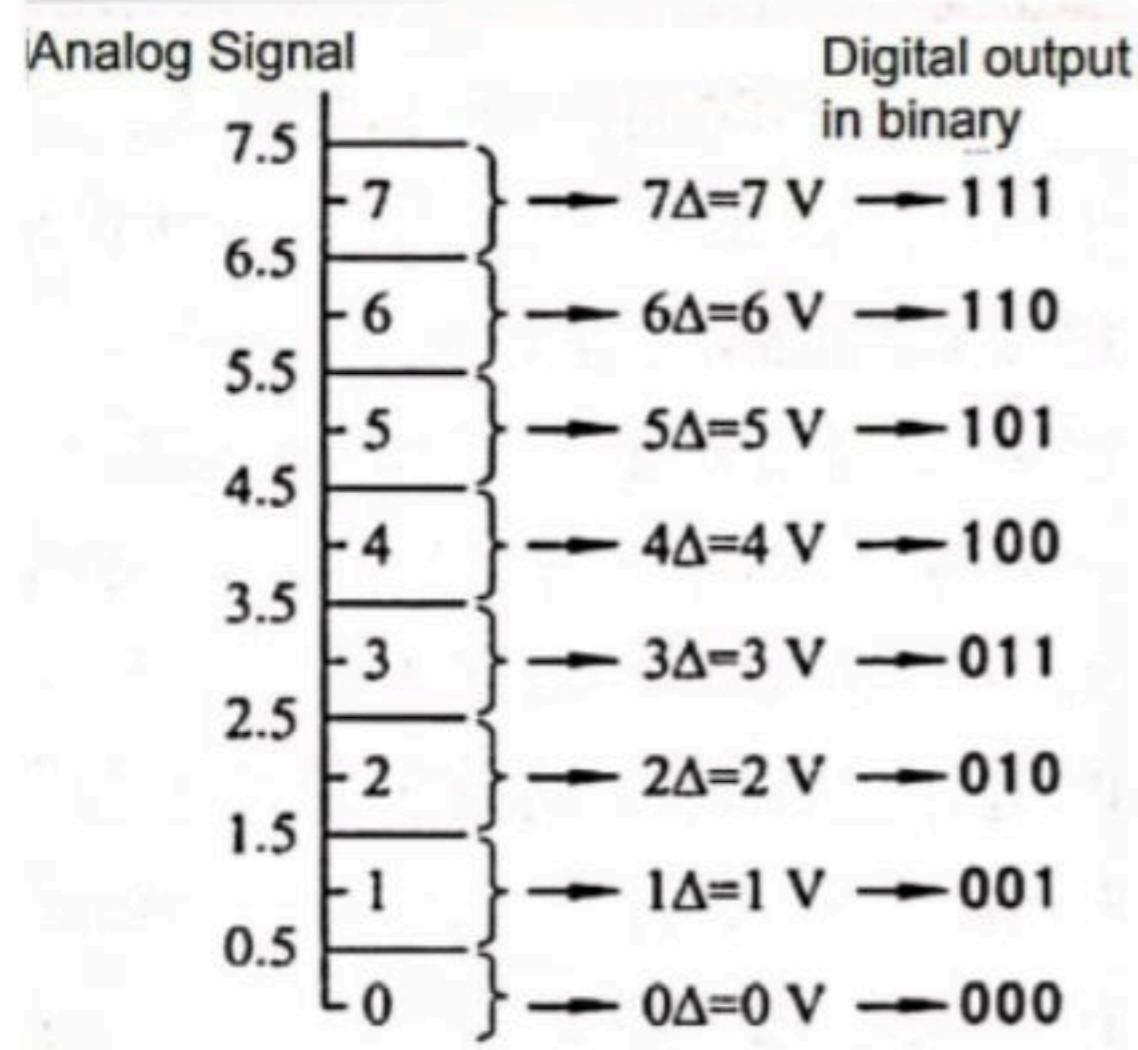
Week-7

ADC and DAC Converters

A/D Conversion Process



Quantizing and Encoding



$$I = \frac{V_{REF} - 0}{R_{\text{Total}}} = \frac{V_{ref}}{\frac{3R}{2} + 6R + \frac{R}{2}}$$

$$I = \frac{V_{REF}}{8R}$$

$$\star v_1 = I(4) = \frac{V_{ref}}{8R}(4) = \frac{V_{ref}}{16}$$

$$\star v_2 = I\left(\frac{3R}{2}\right) = \frac{V_{ref}}{8R}\left(\frac{3R}{2}\right) = \frac{V_{ref}}{16} \cdot \star 3$$

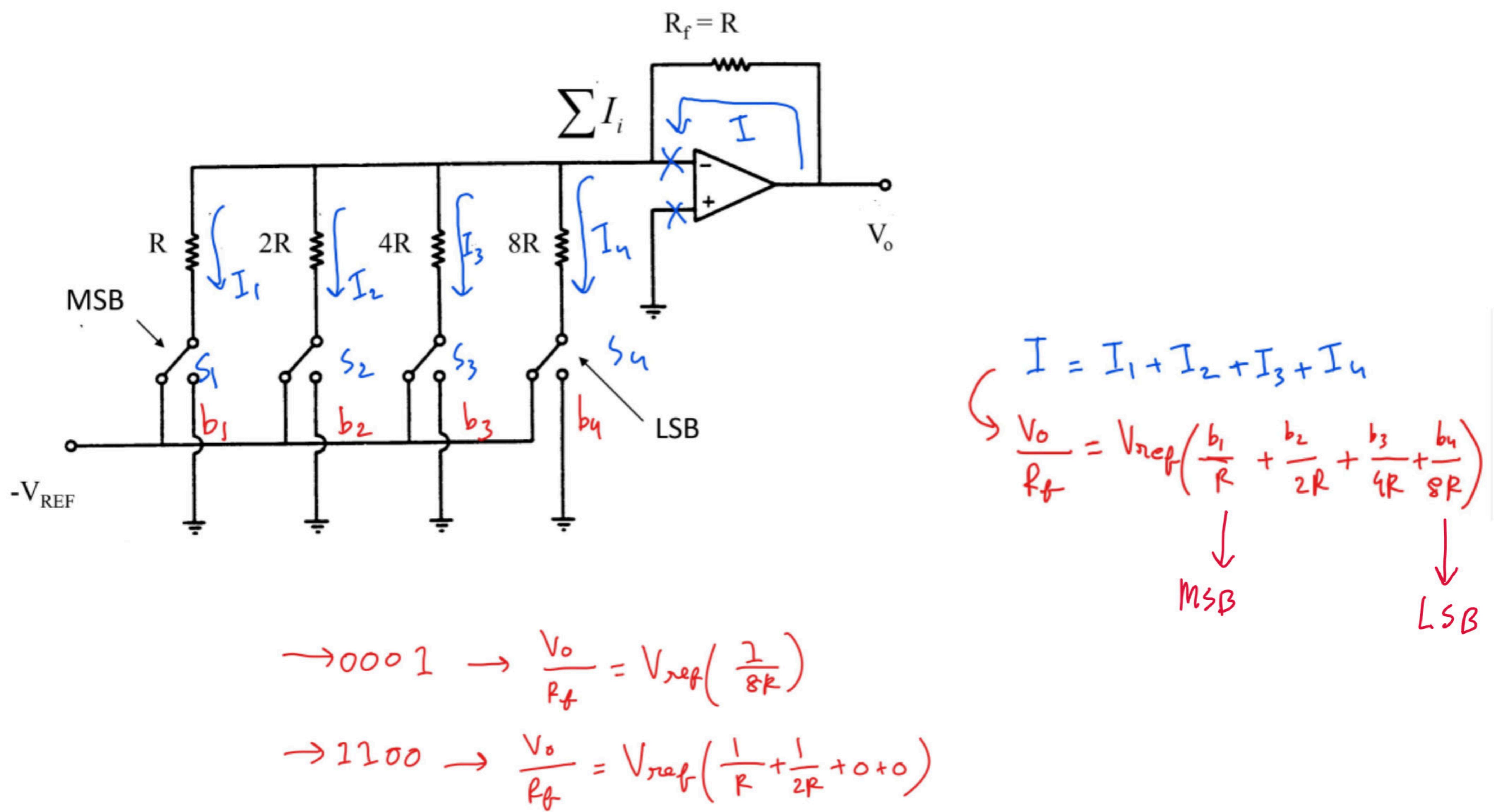
$$\text{Resolution} = v_2 - v_1 = v_3 - v_2 = v_4 - v_3$$

$$\therefore \Delta = 2 * \frac{V_{ref}}{16}$$

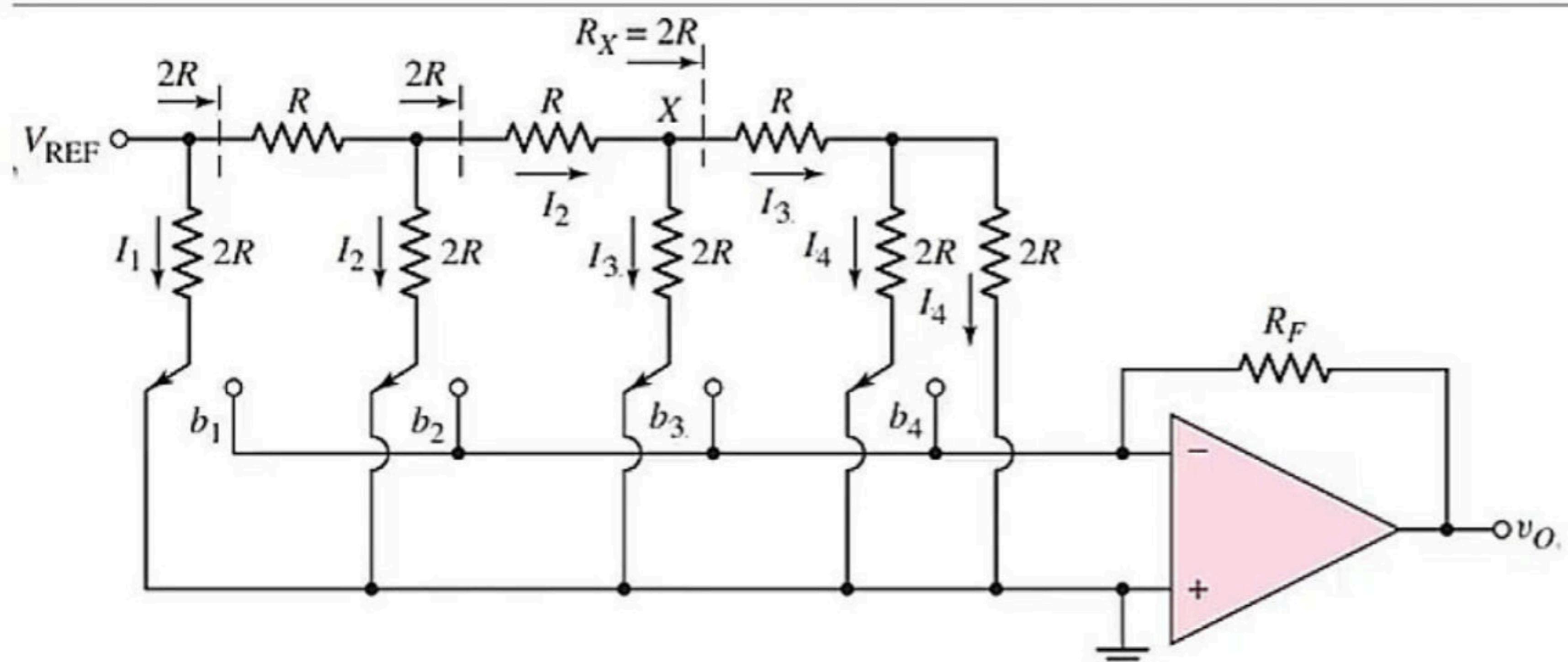
Resistor = 8 pieces = 2^N

Computation = 7 pieces = $2^N - 1$

Binary Weighted Resistor



R-2R Ladder



$$\frac{-v_o}{R_f} = \frac{V_{ref}}{2R} \left(b_1 + \frac{b_2}{2} + \frac{b_3}{4} + \frac{b_4}{8} \right)$$

Handwritten notes indicate the mapping of bits to switches:

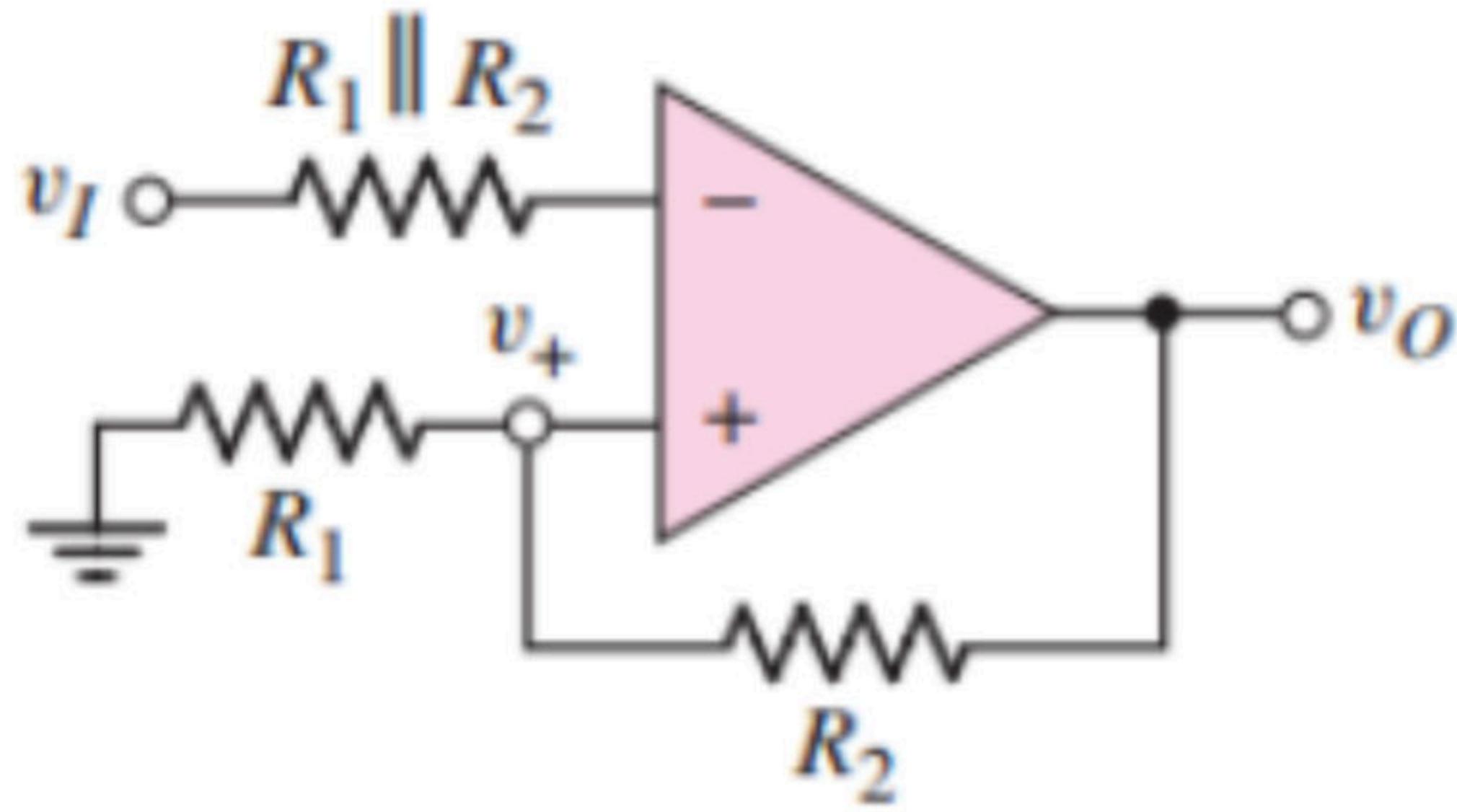
- $MSB \rightarrow b_1$
- $LSB \rightarrow b_4$

Week-8-1

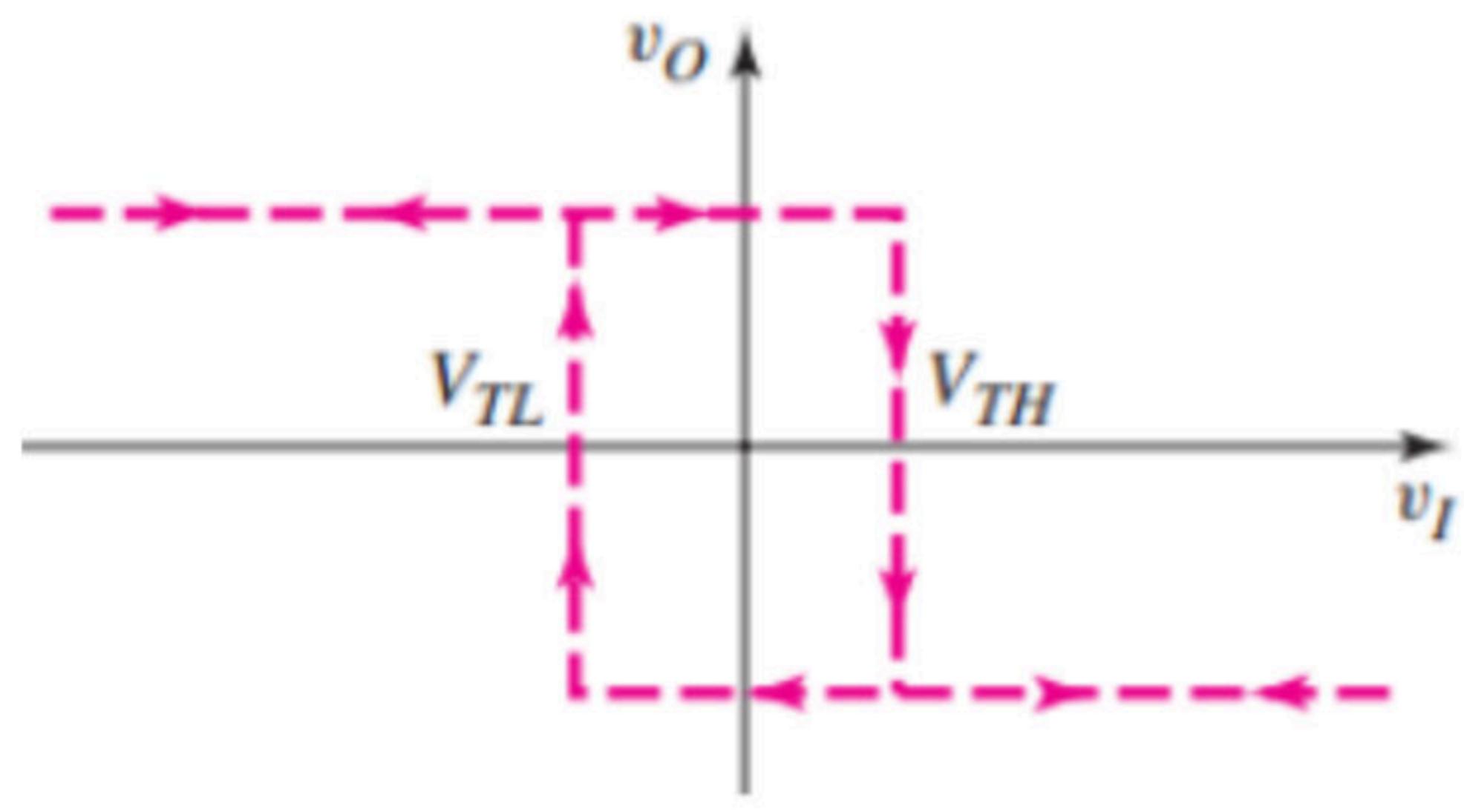
Schmitt Trigger

Schmitt Trigger

Basic Inverting Schmitt



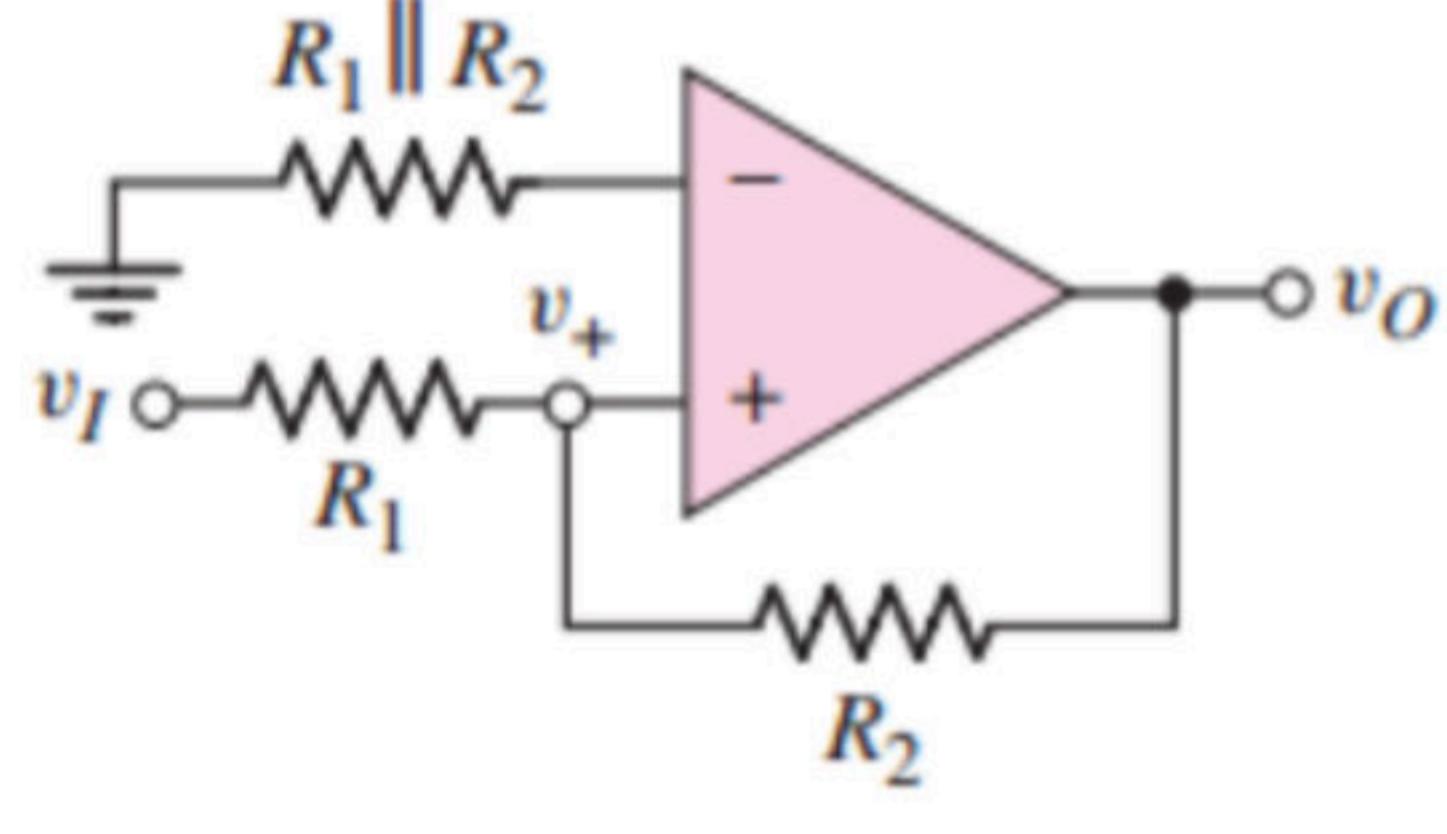
$$V_{TH} = V_H \frac{R_1}{R_1 + R_2}$$



$$V_{TL} = V_L \frac{R_1}{R_1 + R_2}$$

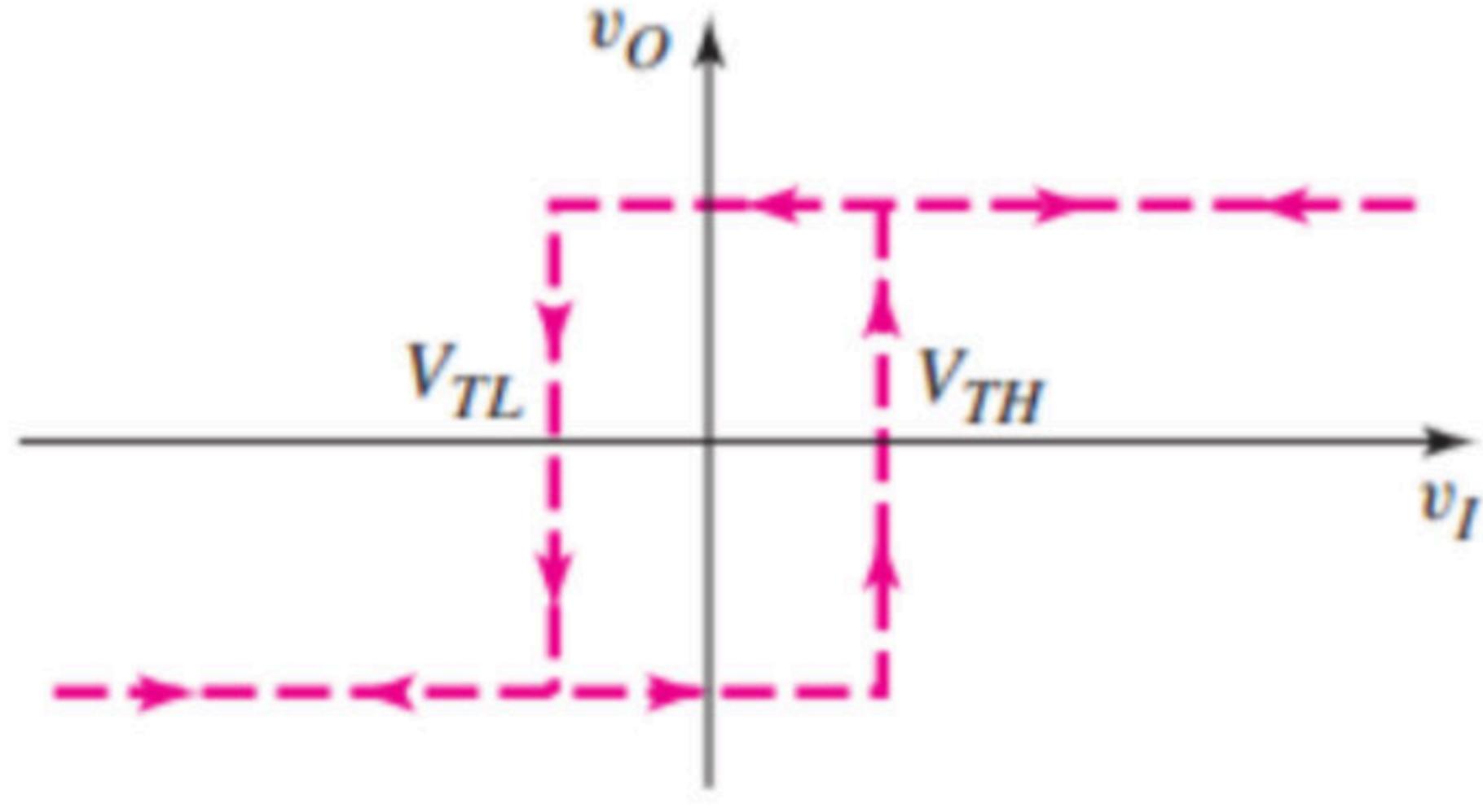
④ Hysteresis Width
 $= V_{TH} - V_{TL}$

Basic Non-Inverting Schmitt



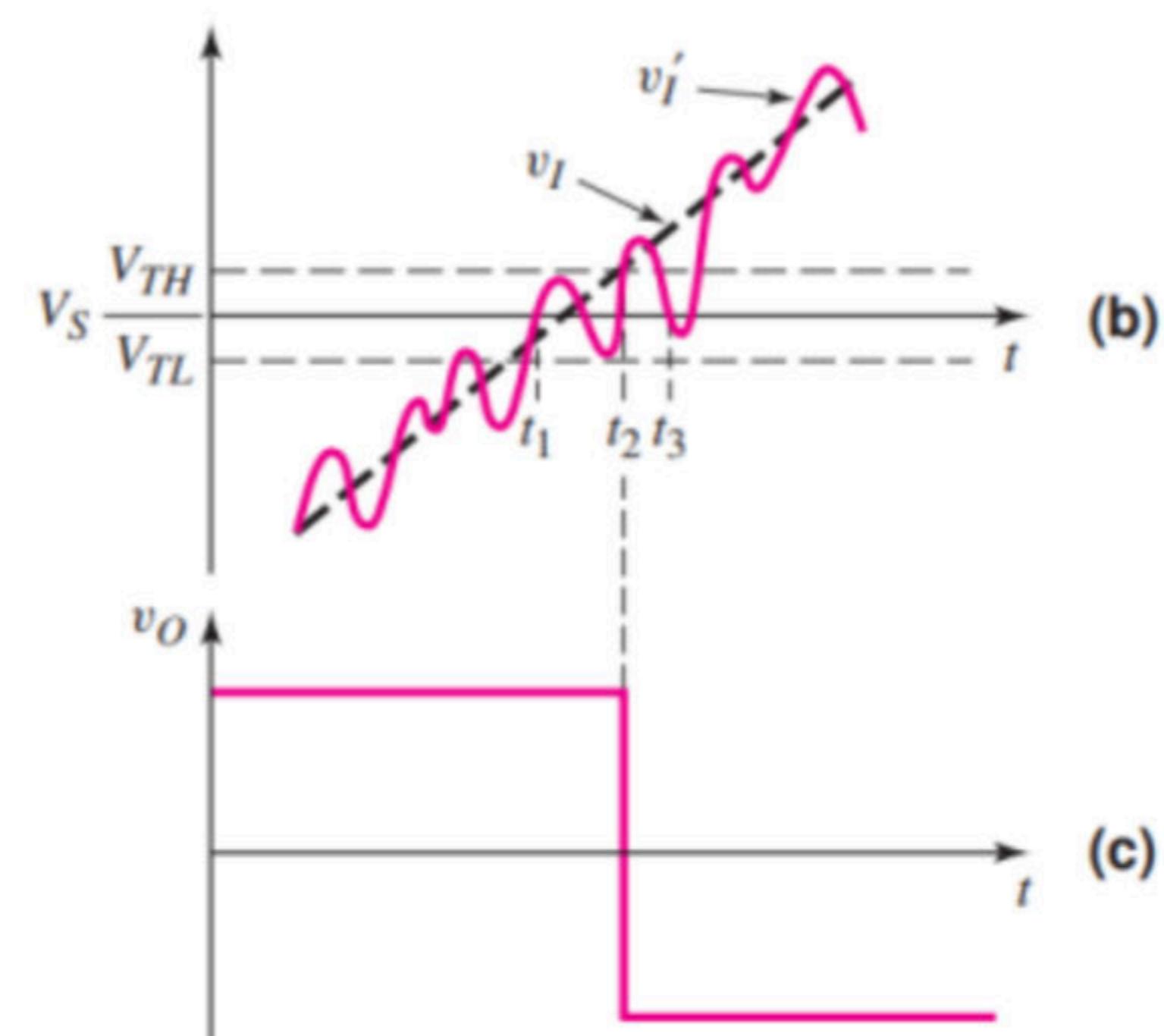
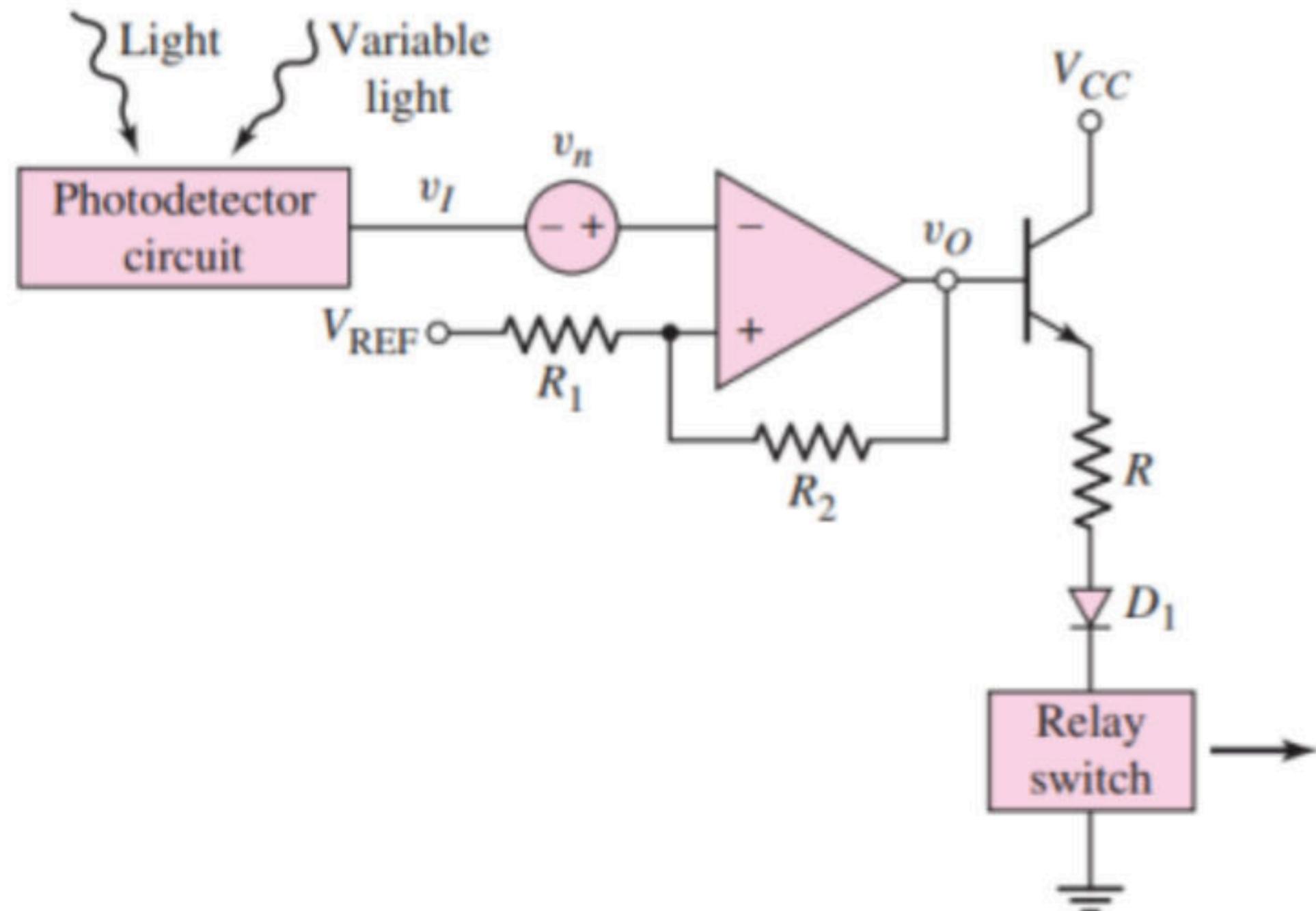
$$V_{TH} = V_L \left(\frac{-R_1}{R_2} \right)$$

$$V_{TL} = V_H \left(\frac{-R_1}{R_2} \right)$$



④ Hysteresis Width
 $= V_{TH} - V_{TL}$

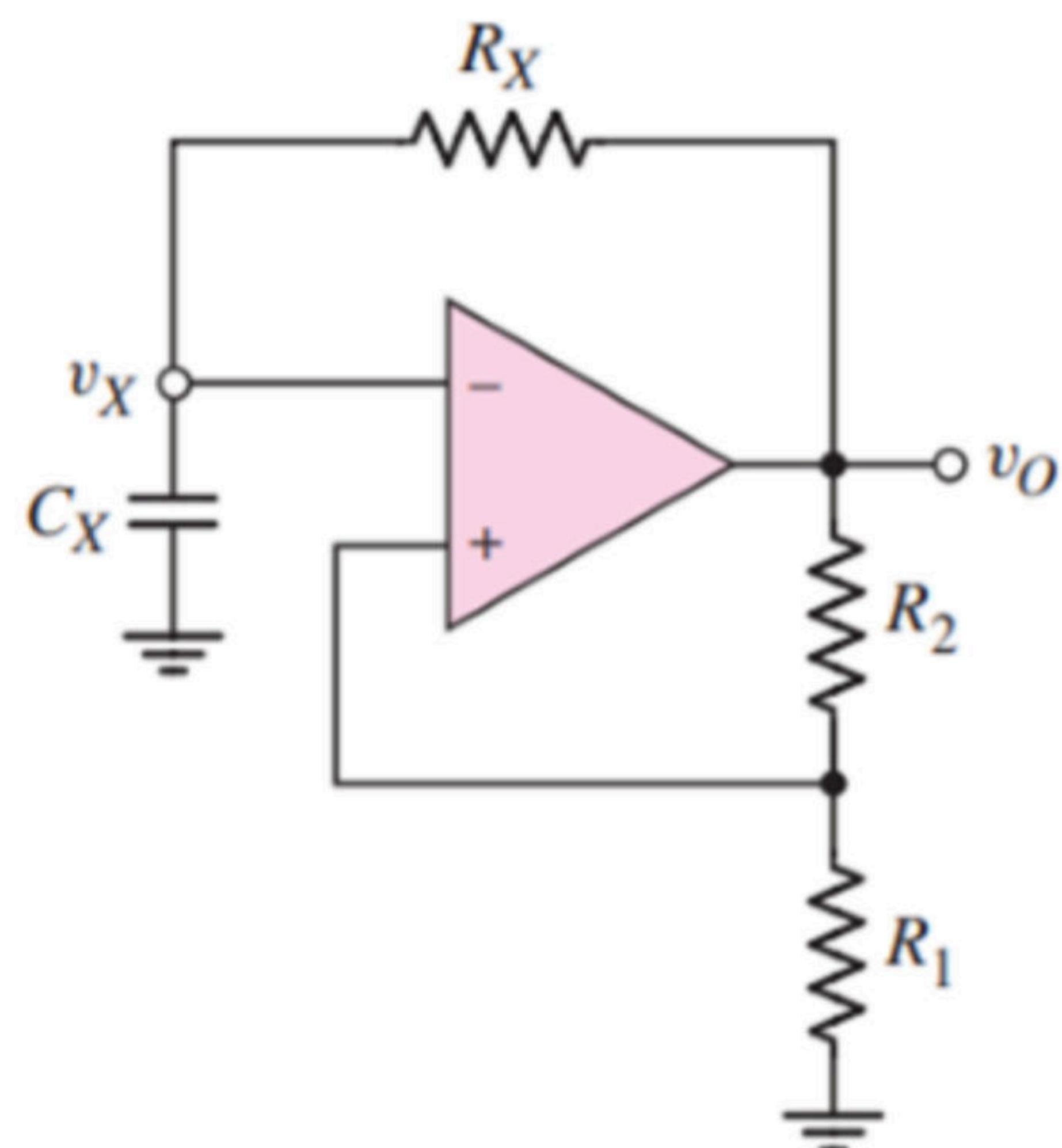
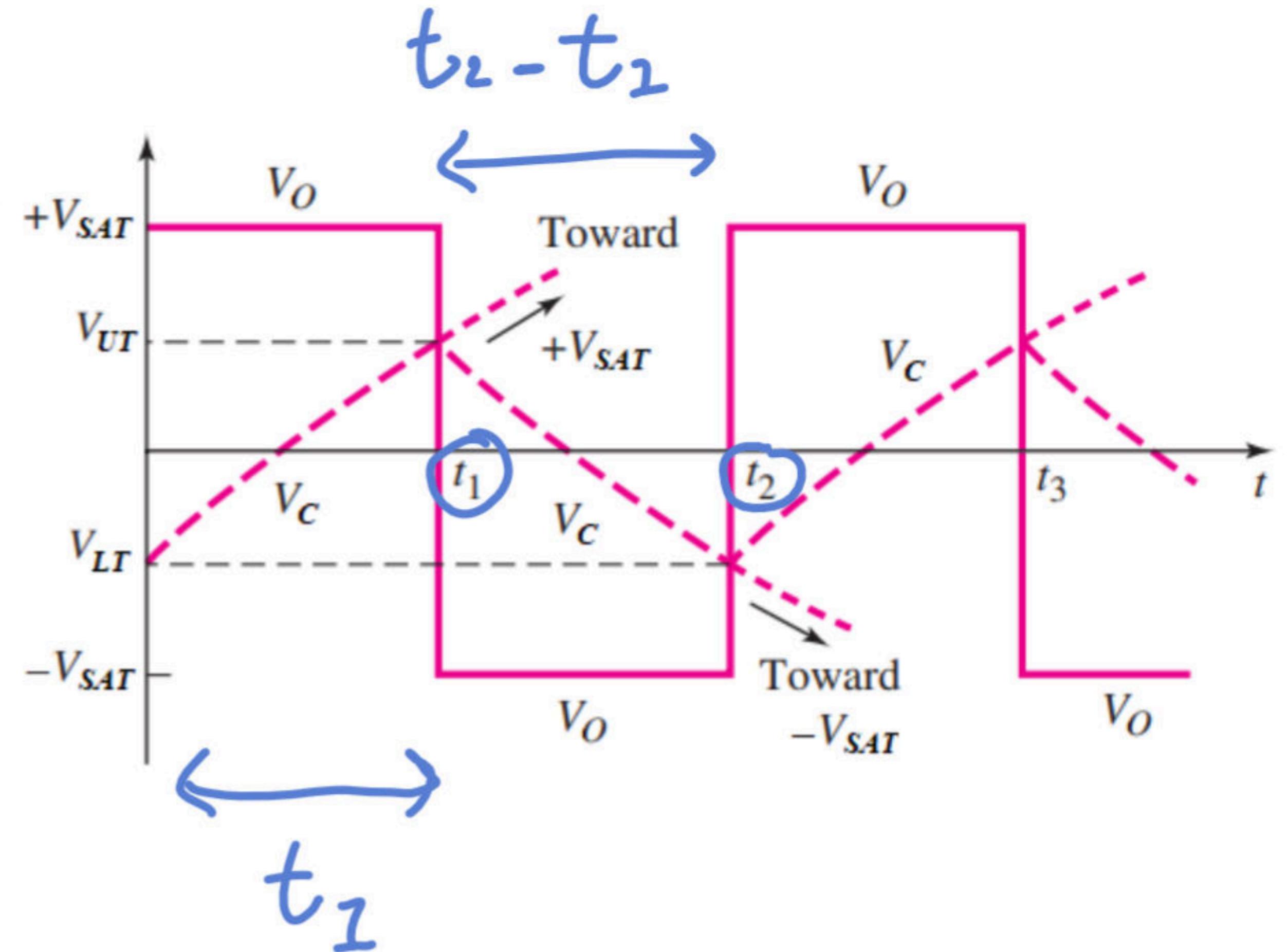
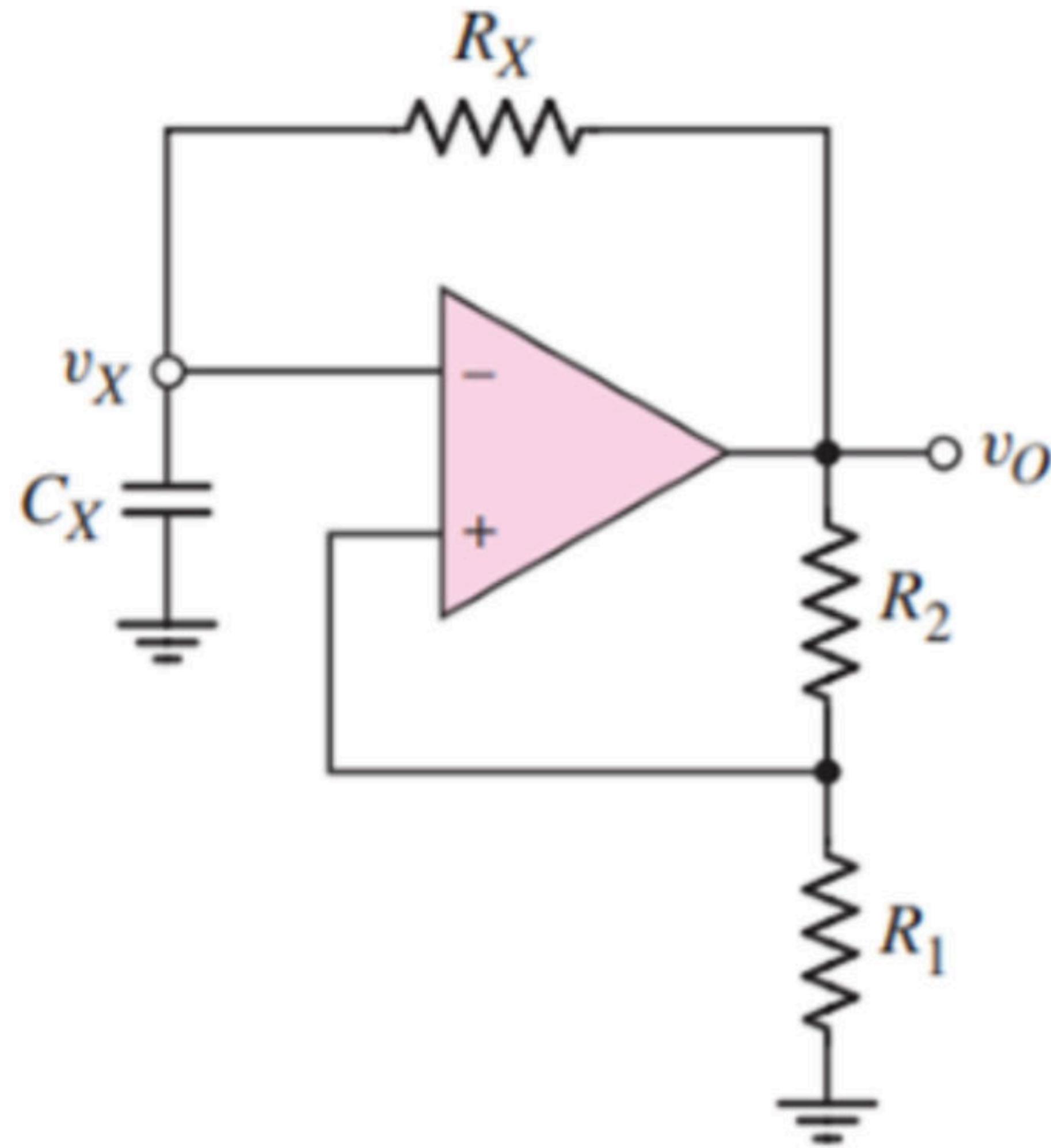
Application of Schmitt Trigger



Week-8-2

Wave Generator

Square Wave Generator or, Astable Multivibrator

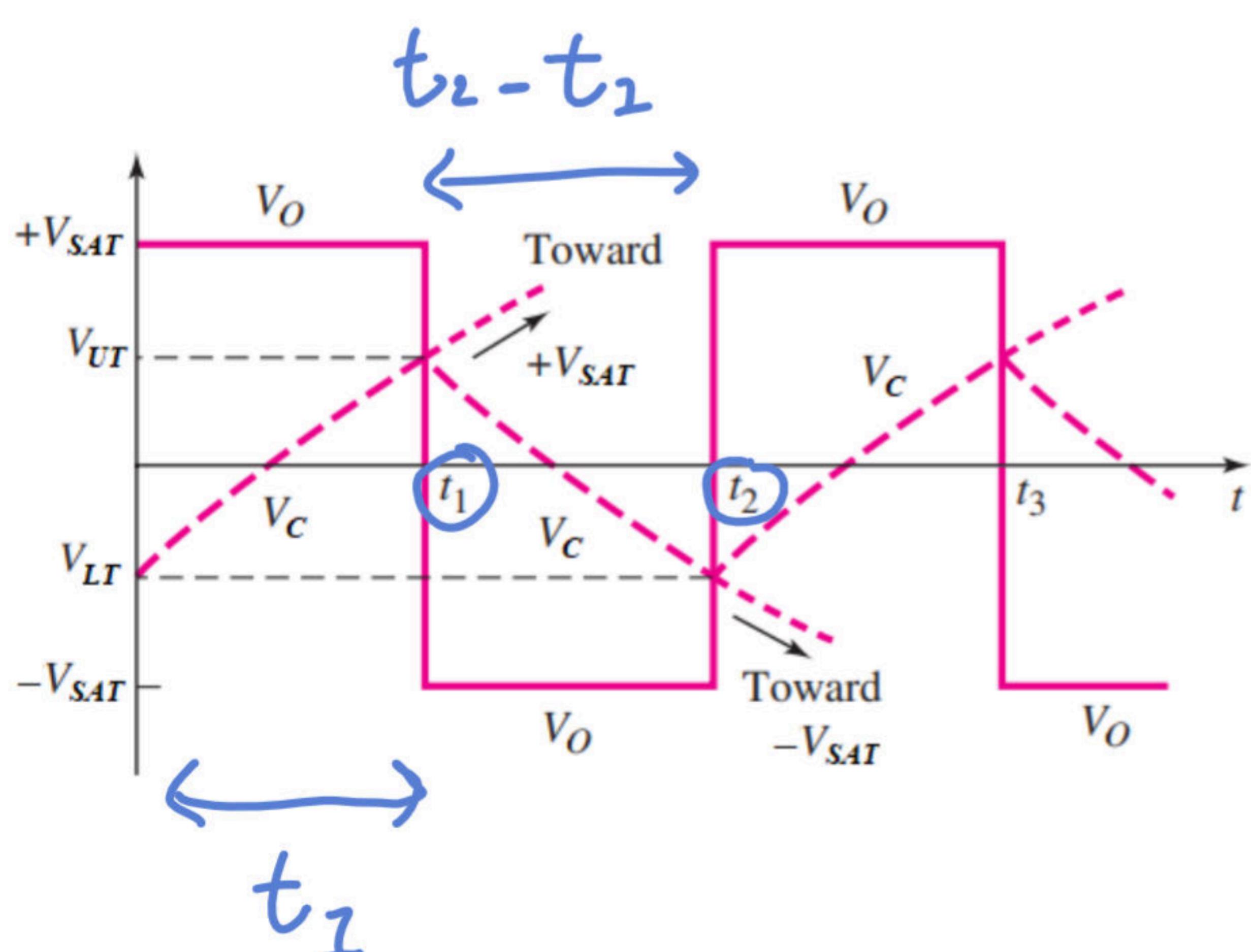
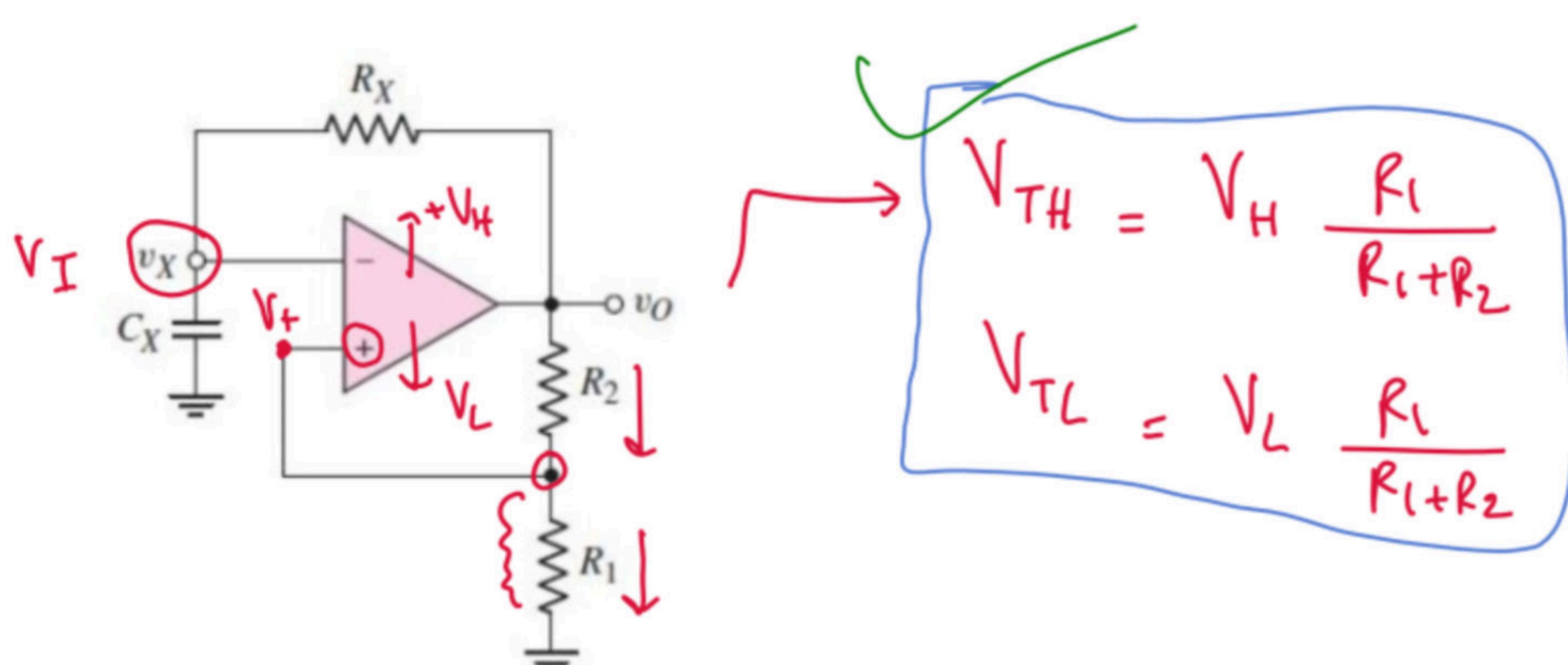


How long v_o is Low

$$t_2 - t_1 = R_X C_X \ln \left[\frac{-V_{SAT} + V_{TH}}{-V_{SAT} - V_{TL}} \right]$$

How long v_o is Hi

$$t_1 = R_X C_X \ln \left[\frac{+V_{SAT} - V_{TL}}{+V_{SAT} - V_{TH}} \right]$$



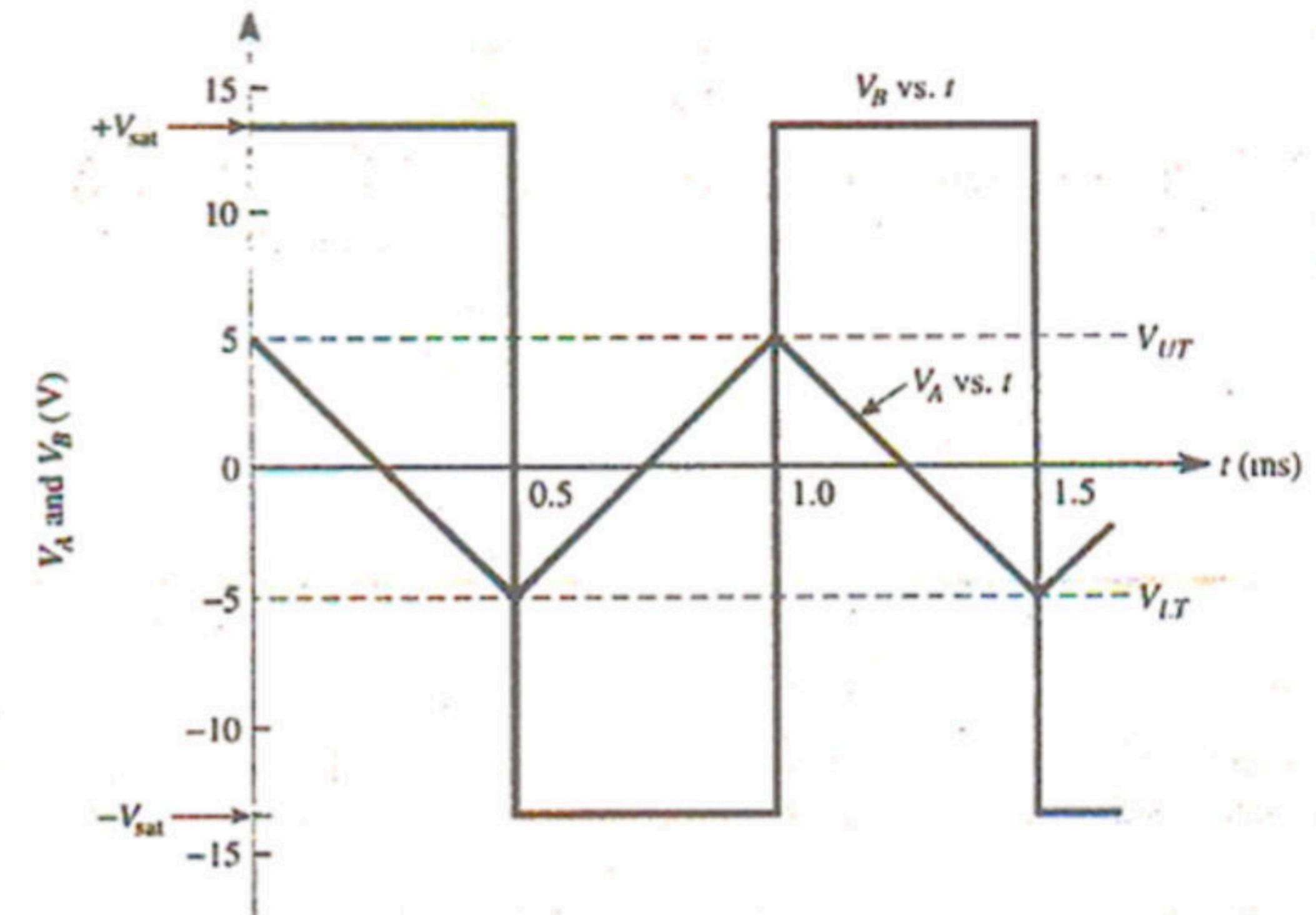
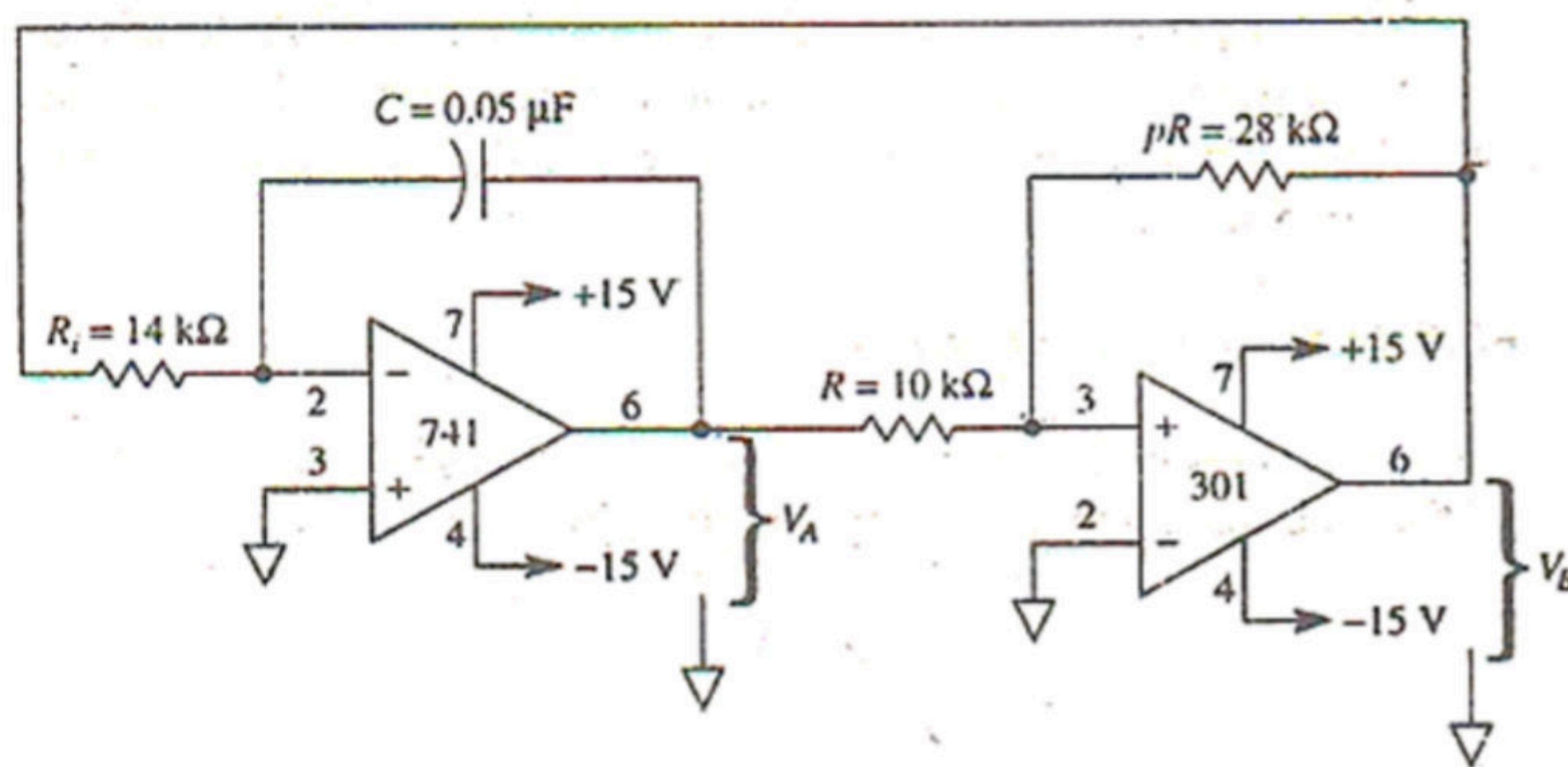
Period = $T = T_1 + T_2$

Freq = $\frac{1}{T}$

Duty cycle \rightarrow How long my output is High in one period.

Duty cycle $\rightarrow \frac{T_1}{T} \times 100\%$.

Triangular Wave Generator



$$\therefore \Delta T_2 = t_2 - t_1 = (R_{ic}) \frac{V_{LT} - V_{uT}}{V_L} \rightarrow \text{when } V_A \text{ is rising}$$

$$\Delta T_1 = t_2 = (R_{ic}) \frac{V_{uT} - V_{LT}}{V_H} \rightarrow V_B = V_H \text{ when } V_A \text{ is falling}$$

$$V_{uT} = V_L \left(\frac{-R}{pR} \right)$$

$$V_{LT} = V_H \left(\frac{-P}{pR} \right)$$

