CSE460: VLSI Design (Summer 2022)- Midterm

Practice problems for exams

[At the end of each lecture there is a "Reading" section in buX. After watching the lectures and reading the corresponding texts, try to solve the following problems. The final questions in the exam will be conceptual & analytical (theoretical and problem solving).]

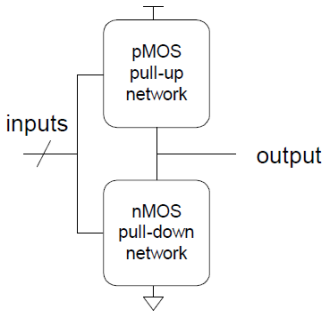
More problems will be added in this doc as we progress through the semester.

Week 1: Introduction to VLSI Design, History and Timeline

1. Comparison between FET and other types of transistors.
2. How do MOSFETs allow us high levels of integration in IC design?
3. What is Moore's law? Briefly explain using appropriate diagrams.
4. Describe different levels of design abstraction.
5. Suppose, you are building a digital system that has 4 inputs (x1, x2, x3, x4) and you want to produce the output 1 only if the combination of the inputs are 0, 1, 0, 1, respectively. Design a circuit that implements the system using logic gates.
6. Design the simplest circuit that has three inputs, x1, x2, and x3, which produces an output value of 1 whenever two or more of the input variables have the value 1; otherwise, the output has to be 0. (Using karnaugh maps)
7. Design a circuit with output f and inputs x1, x0, y1, and y0. Let X = x1x0 and Y = y1y0 represent two 2-digit binary numbers. The output f should be 1 if the numbers represented by X and Y are equal. Otherwise, f should be 0.
8. Practice designing different logic circuits using logic gates for arbitrary logic functions.

Week 2: Introduction to CMOS technology and CMOS circuits

1. Why do we use impure (doped) silicon as our substrate for building MOS transistors?
2. What is the conduction complement rule?
3. Explain the following general structure of a CMOS logic gate, mentioning the different behaviours for different combinations of the networks:



4. Design CMOS compound gates that implements the following functions:
    a. Y = (A.B+C.D).E
    b. Y = (A+B).(C+D)
    c. Y = (A.B.C) + D
    d. Y = $\overline{A.(B+C).D}$
5. What is signal strength? Explain the behavior of MOS transistors as pass transistors while mentioning which transistors produce which type of strong and weak signals.
6. Explain restoring and non-restoring properties of a device with the help of different kinds of CMOS tristate devices.
7. Explain how the complexity, cost and area requirement for a 2:1 MUX can be reduced by orders of magnitude by going from gate-level implementation to CMOS transmission gate/CMOS tristate inverter implementation.
8. Design a 2:1 MUX using CMOS tristate inverters and explain its working principle.
9. Design a positive level triggered D latch and explain its working principle.
10. Design a positive edge triggered D flip flop and explain its working principle using a suitable timing diagram.
11. Practice designing CMOS logic gates for arbitrary logic functions.

Week 3: Introduction to FSMs

1. What is a sequential circuit? Give a few practical examples of finite state machines.
2. Using a block diagram, explain the working mechanism of a general sequential circuit.
3. What is the difference between a Moore type FSM and a Mealy type FSM?

Week 4: Finite State Machines

1. Derive the Moore type state diagram, state table, state assigned table and the final circuit for the following systems:
    a. A modulo-6 up counter (i.e. a counter that counts 0,1,2,3,4,5,0,1,2,...).
        i. It should have a 1-bit input w, a clock signal and a multi-bit output z.
        ii. The machine should increase its count whenever w = 1, and hold its previous count otherwise.
        iii. At each counting step the machine should output the value of the count in binary.

b. A machine that detects the following pattern in its input (w) : 1, 0, 1.
    i. Repeating and overlapping sequences should be detected.
    ii. The machine should generate the output z = 1 if in the past 3 clock cycles 101 pattern was detected, and z = 0 otherwise.
c. A machine that has the following state table:

Present state	Next state		Output
	$w = 0$	$w = 1$	z
A	A	B	0
B	A	C	0
C	A	D	0
D	A	D	1

a. An FSM that has an input w and an output z. The machine has to generate z = 1 when the previous four values of w were 1001 or 1111; otherwise, z = 0. Overlapping input patterns are allowed. An example of the desired behavior is:

$$w : 0101111001100111111$$
$$z : \ 0000001001000100 11$$

2. Explain different types of encoding schemes for FSMs mentioning their advantages and disadvantages.
3. Practice designing Moore type state diagrams for different scenarios.
4. How one-hot encoded sequential circuits can be faster than moore/mealy type sequential circuits?

Week 5: Fabrication; Layout and Stick Diagram

1. Draw the typical cross-section of an nMOS/pMOS transistor carefully denoting each terminal and their constituent materials.
2. Draw the cross-section of a CMOS inverter in an n-well process (carefully denote each terminal and their constituent materials).
3. Draw the cross-section of a CMOS inverter in a p-well process (carefully denote each terminal and their constituent materials).
4. What are well and substrate taps and why are they necessary?
5. Describe the fabrication process steps briefly.
6. What is the photolithography process?
7. Why do we need contacts?
8. Explain briefly: CVD process, Diffusion process, Ion Implantation process.
9. Discuss some of the basic simplified rules for layout design and using the rules, derive the dimensions of an unit transistor (in terms of λ).
10. In 6 separate figures, draw the set of 6 layout layer masks (n-well, polysilicon, n+ diffusion, p+ diffusion, contact, metal) for the following CMOS inverter layout:(Fig1)
11. Briefly discuss the properties of a standard cell layout.
12. Draw the layout of an isolated nMOS/pMOS transistor.

13. Design the layout of a NAND3/NOR3 gate and determine the area.
14. Explain the "Well-spacing" rule for Lambda based design approach.
15. Define "Wiring Tracks" and derive its dimensions.
16. Explain how one can estimate the area of a layout by counting the vertical and horizontal wiring tracks from its corresponding stick diagram.
17. Practice drawing stick diagrams and estimating the area of different CMOS inverting logic functions/gates.

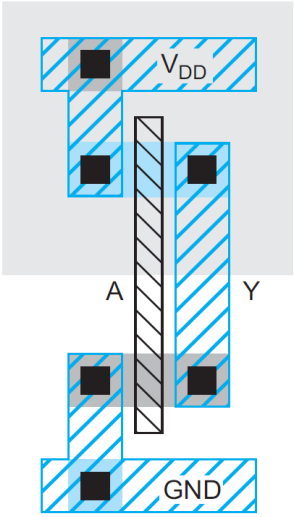


Fig. 1; Draw set of 6 layout masks