Andrew's Tasks:

- Custom7Seg.VHDL and testing code
    - Wrote the code for component holding the letter and symbol assignments in regards to specific inputs and the test code to be run on the FPGA board
- IO_Controller.VHDL
    - Wrote the code for the IO_Controller component
- PCE.VHDL and testbench (is actually PEC (program execution counter) ~ but I read the pdf as PCE)
    - Wrote code for the PEC (program execution counter) and the testbench to ensure that the PEC works as intended
- Scheduler.VHDL and testbench
    - Wrote, debugged (multiple times, probably 100+ times) the scheduler component and ensured that all functionalities of the scheduler were met.
- SMDB.VHDL
    - Instantiated components and wrote the backbone code for the SMDB
- SMDB top level design diagram and Datapaths design diagram
    - Used SmartDraw to create diagrams
    - I'm very sorry for your eyes, it was just not meant to be. (first time visio user)
- Crying and sobbing in pain
    - Shared equally between myself and Shakeeb Zacky

- All of the work done towards this project was shared equally (including the pain and sadness)