Digital Logic Design Laboratory

Digital Clock with Exclusion of 44 in Display

Project Report

GROUP MEMBERS:

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OBJECTIVES:

1. The primary objective of this project was to design and implement a digital clock using flip flops and logic gates.
2. The clock actually operates on a unique timekeeping mechanism where 1 minute is equivalent to 59 seconds, and 1 hour is equivalent to 59 minutes
3. Additionally, the clock was designed to exclude the number '44' from both the minute's and second's display.

COMPONENTS USED:

1. D -flipflop
2. T- flipflop
3. IC-7432
4. IC-7408
5. IC-7404
6. 7 segment display
7. Logisim software

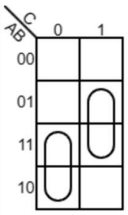
TRUTHTABLES & KMAPS:

1. Truthtable for Mod-6 counter:

	Current States			**Next States**			**Flipflop**		
	QA	QB	QC	QA+	QB+	QC+	D_{QA}	D_{QB}	D_{QC}
0	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	0	0	1	0
2	0	1	0	0	1	1	0	1	1
3	0	1	1	1	0	0	1	0	0
4	1	0	0	1	0	1	1	0	1
5	1	0	1	0	0	0	0	0	0

KMap for D_{QA} :

KMap

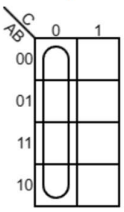


Boolean Algebra

$A\overline{C}+BC$

KMap for D_{QC} :

KMap

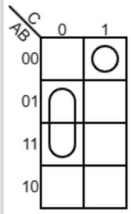


Boolean Algebra

$\overline{C}$

KMap for D_{QB} :

KMap



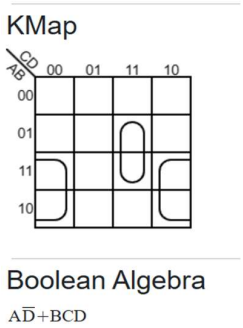
Boolean Algebra

$B\overline{C}+\overline{A}\overline{B}C$

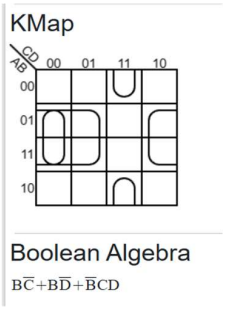
2. Truthtable for Mod-10 counter:

	Current States				Next States				Flipflop			
	QA	QB	QC	QD	QA+	QB+	QC+	QD+	D_{QA}	D_{QB}	D_{QC}	D_{QD}
0	0	0	0	0	0	0	0	1	0	0	0	1
1	0	0	0	1	0	0	1	0	0	0	1	0
2	0	0	1	0	0	0	1	1	0	0	1	1
3	0	0	1	1	0	1	0	0	0	1	0	0
4	0	1	0	0	0	1	0	1	0	1	0	1
5	0	1	0	1	0	1	1	0	0	1	1	0
6	0	1	1	0	0	1	1	1	0	1	1	1
7	0	1	1	1	1	0	0	0	1	0	0	0
8	1	0	0	0	1	0	0	1	1	0	0	1
9	1	0	0	1	0	0	0	0	0	0	0	0

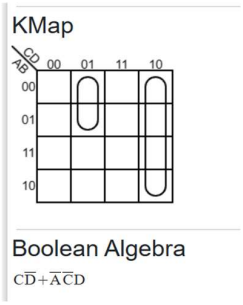
KMap for D_{QA} :



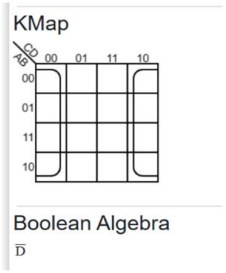
KMap for D_{QC} :



KMap for D_{QB} :



KMap for D_{QD} :

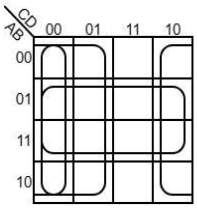


3. Truthtable for Mod-10(4 skip) counter:

	Current States				Next States				Flipflop			
	QA	QB	QC	QD	QA+	QB+	QC+	QD+	T_{QA}	T_{QB}	T_{QC}	T_{QD}
0	0	0	0	0	0	0	0	1	0	0	0	1
1	0	0	0	1	0	0	1	0	0	0	1	1
2	0	0	1	0	0	0	1	1	0	0	0	1
3	0	0	1	1	0	1	0	0	0	1	1	0
4	0	1	0	1	0	1	1	0	0	0	1	1
5	0	1	1	0	0	1	1	1	0	0	0	1
6	0	1	1	1	1	0	0	0	1	1	1	1
7	1	0	0	0	1	0	0	1	0	0	0	1
8	1	0	0	1	0	0	0	0	1	0	0	1

KMap for T_{QA} :

KMap

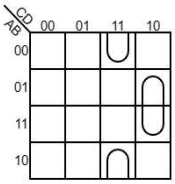


Boolean Algebra

$\overline{D}+B+\overline{C}$

KMap for T_{QB} :

KMap

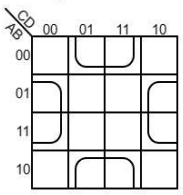


Boolean Algebra

$BC\overline{D}+\overline{B}CD$

KMap for T_{QC} :

KMap

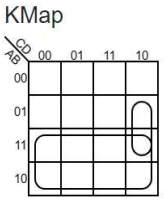


Boolean Algebra

$B\overline{D}+\overline{B}D$

KMap for T_{QD} :

KMap

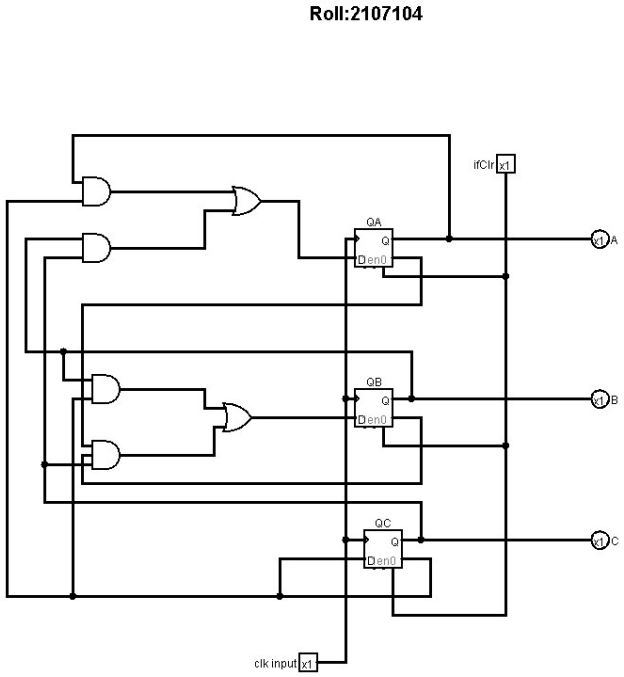


Boolean Algebra

$A+BC\overline{D}$

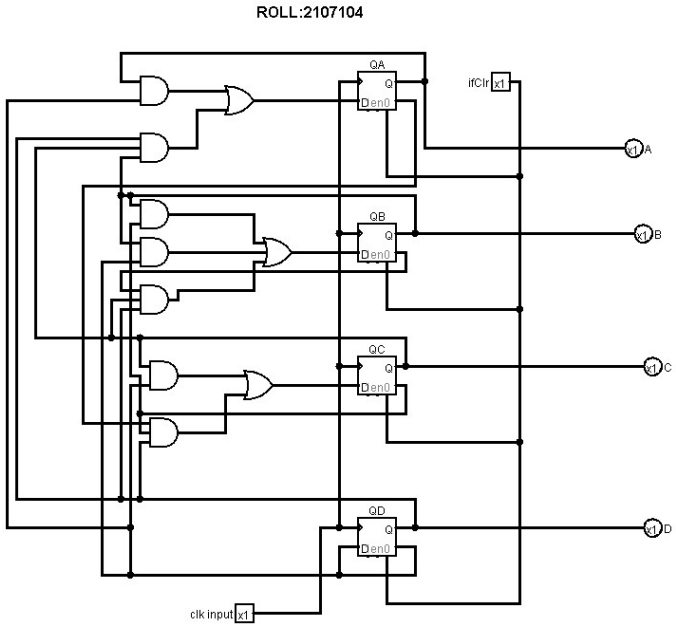
Circuit Diagrams:

1.Mod-6 Counter:



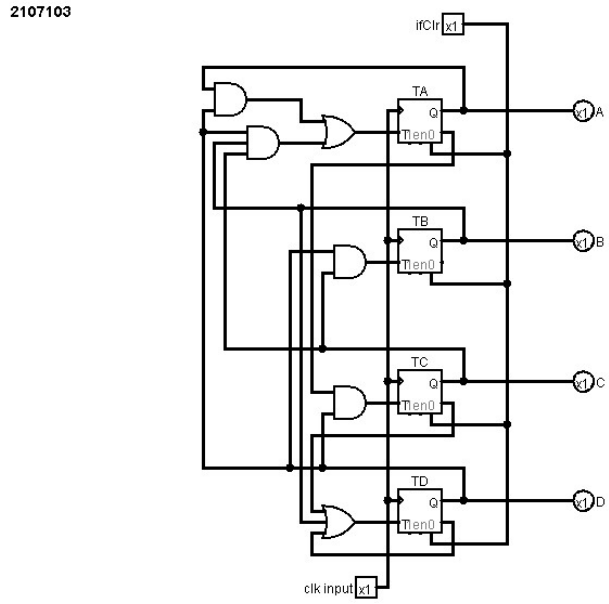
Here we used 3 D-flipflops and 2 inputs. Clock input used for getting synchronous pulse and ifclr used for getting the reset state.

2.Mod-10 Counter:



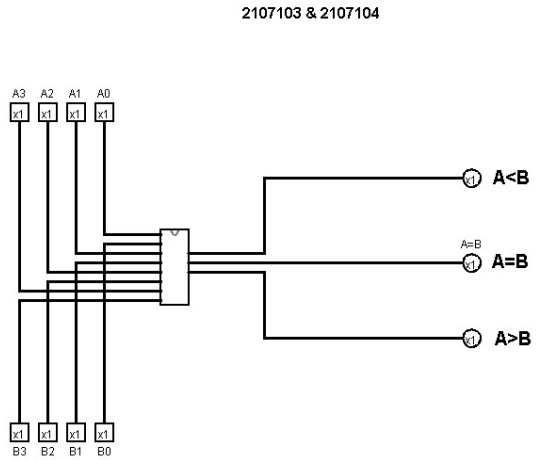
Here we used 4 D-flipflops and 2 inputs. Clock input used for getting synchronous pulse and ifclr used for getting the reset state.

3. Mod-10 Counter(skips 4):

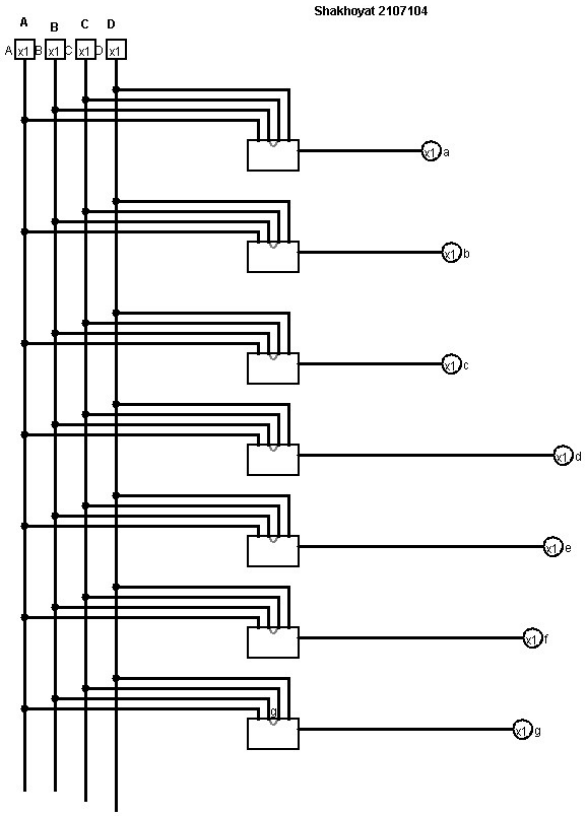


Here we used 4 D-flipflops and 2 inputs. Clock input used for getting synchronous pulse and ifclr used for getting the reset state. The basic difference is its skipping the digit 4.

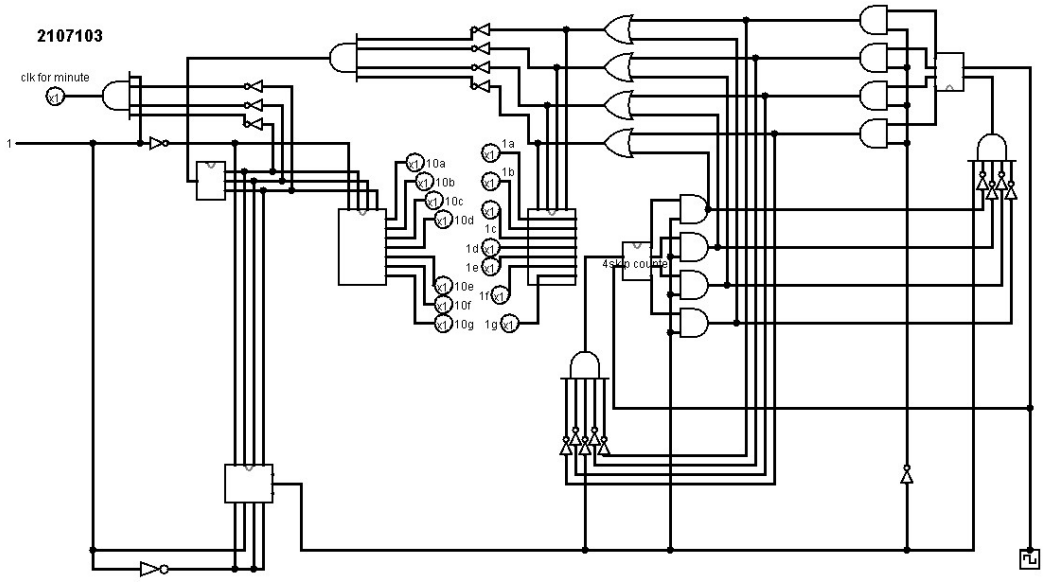
4. 4 Bit Comparator:



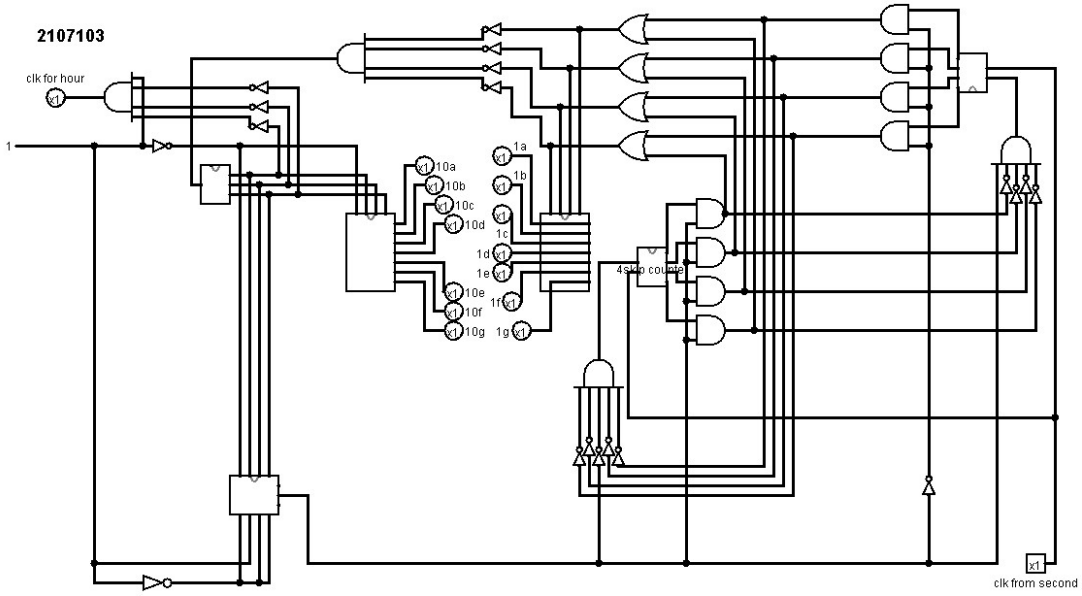
5. 4 Bit to 7 segment Decoder:



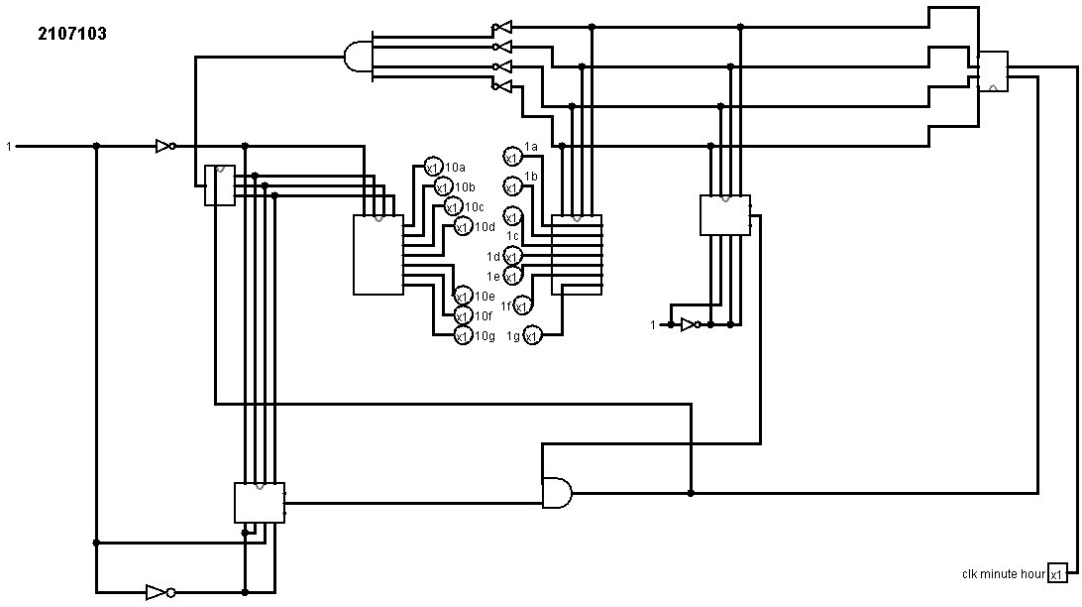
6. Second Circuit:



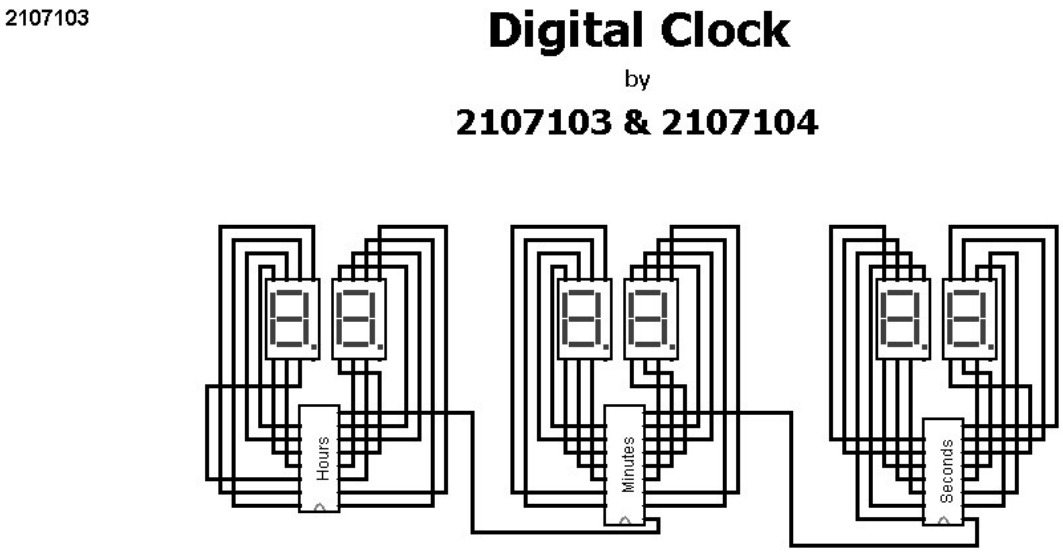
7. Minute Circuit:



8. Hour Circuit:



9. Clock Final:



WORK FLOW:

1. Second Circuit: At the beginning, the clock pulse goes to the Mod-10 counter, whenever the mod 10 counter hits 0 it passes a pulse to Mod-6 counter. When the Mod-6 counter hits 4, the output of Mod-10 counter is ignored and the output of Mod-10(4 skip) counter is used. And when both the counters hits 0, one pulse goes to minute circuit.

2. Minute Circuit: At the beginning, the pulse from the second circuit goes to the Mod-10 counter, whenever the Mod-10 counter hits 0 it passes a pulse to Mod-6 counter. When the Mod-6 counter hits 4, the output of Mod-10 counter is ignored and the output of Mod-10(4 skip) counter is used. And when both the counter hits 0, one pulse goes to hour circuit.

3. Hour Circuit: At the beginning, the pulse from the minute circuit goes to the Mod-10 counter, whenever the Mod-10 counter hits zero it passes a pulse to

Mod-6 counter. And when the Mod-6 counter hits 2 and Mod-10 counter hits 4 a pulse goes to the ifClr input of the counters which sets the both counters to reset states.

DISCUSSION & CONCLUSION:

Through the project, we learned how we can design and implement a critical circuits by ourselves. As the circuits are quite complex, there are too many logic gates used. Which may occur some unexpected time delay in the output. If implementation on the circuit level could be more optimized then it could be far better minimizing the time delay. So we could have been more cautious while implementing and choosing the circuits we chose for the project to avoid this unexpected time delay that we are having.