CBCS SCHEME

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21CS33

Third Semester B.E./B.Tech. Degree Examination, Dec.2024/Jan.2025
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note : *Answer any FIVE full questions, choosing ONE full question from each module.*

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. With a neat diagram and mathematical analysis explain fixed bias circuit. **(06 Marks)**
b. With hysteresis characteristics explain the working of Inverting Schmitt trigger. **(06 Marks)**
c. Explain current to voltage and voltage to current convertor. **(08 Marks)**

OR

2 a. Discuss Regulated power supply parameters. **(06 Marks)**
b. Explain the working of R-2R ladder D to A convertor. **(06 Marks)**
c. Explain successive approximation A to D convertor. **(08 Marks)**

Module-2

3 a. Find all the prime implicates of the function
$f(a,b,c,d) = \Pi(0,2,3,4,5,12,13) + \Pi d(8,10)$
using the Quine-McCluskey method. **(10 Marks)**
b. Plot the Karnaugh maps and find all the minimal sums and minimal products of the following Boolean functions.
i) $f(a,b,c) = \sum(2,4,5,6,7)$ ii) $f(a,b,c) = \Pi(1,4,5,6)$. **(10 Marks)**

OR

4 a. With an example, explain Petrik's method. **(06 Marks)**
b. For the given Boolean function, determine a minimal sum and a minimal product using MEV techniques using a, b and c as the map variables.
$f = \sum(3,4,5,7,8,11,12,13,15)$. **(08 Marks)**
c. Explain entered variable map method. **(06 Marks)**

Module-3

5 a. Implement the following function using 8 : 1 multiplexer,
$F(a,b,c,d) = \sum m(0, 1, 5, 6, 8, 10, 12, 15)$. **(07 Marks)**
b. Implement 7-segment decoder using PLA. **(08 Marks)**
c. Discuss Four kinds of three state buffers. **(05 Marks)**

OR

6 a. Implement Full Adder using 3 : 8 Decoder. **(07 Marks)**
b. Design Hexadecimal to ASCII code converter using suitable ROM. Give the connection diagram of ROM. **(08 Marks)**
c. Explain static 1 Hazard with its recover method. **(05 Marks)**

Module-4

7 a. Explain structure of VHDL program. Write VHDL code for 4 bit parallel adder using full adder as component. **(08 Marks)**

b. Explain the working of SR latch using NOR gates. **(06 Marks)**

c. Explain edge triggered D flip flop. **(06 Marks)**

OR

8 a. Explain J-K Master slave flip flop with suitable timing diagram. **(10 Marks)**

b. Derive the characteristics equations for D, T, SR and JK flip flops. **(10 Marks)**

Module-5

9 a. With a neat diagram, explain 4-bit parallel adder with accumulator. **(10 Marks)**

b. Define counter. Design mod-5 counter using J-K flip flop. **(10 Marks)**

OR

10 a. With neat diagram, explain 4 bit SISO register. **(08 Marks)**

b. Mention the application of shift registers. **(05 Marks)**

c. Explain the working of a 3 bit shift register. **(07 Marks)**

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