DATA SHEET

FocalTech

FT5536G

True Multi-Touch
Capacitive Touch Panel Controller

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INTRODUCTION

The FT5536G is a single-chip capacitive touch panel controller with built-in enhanced Micro-controller unit (MCU) with 54KB PRAM, 18KB DRAM and 128KB Flash. It provides the benefits of full screen common mode scan technology, fast response time and high level of accuracy. It can drive capacitive type touch panel with up to 22 driving (TX) and 28 sensing lines (RX).

FEATURES

- Mutual Capacitive Sensing Techniques
- Full Screen Common Mode Scan Techniques
- True Multi-touch up to 10 Points of absolute X and Y Coordinates
- High immunity to RF and power Interferences
- Supports up to 22TX + 28RX
- Supports up to 10 fingers
- High immunity to inductive power noise
- Automatic mode switching (Active, Monitor, Sleep)
- Supports>120Hz sampling rate
- Auto-calibration
- Support IIC (up to 400Kbps) interface
- Power
  - 2.7 to 3.6V Operating Voltage
  - IOVCC supports 1.7V~3.6V
- Built-in 128KB Flash
- Features “short I/O” testing for sense pins
- 3 Operating Modes
  - Active
  - Monitor
  - Sleep
- Operating Temperature Range: -40°C to +85°C
- Package:
  - QFN60L 6x6x0.6mm, 0.35mm/pitch

1. OVERVIEW

1.1. Typical Applications

FT5536G accommodates a wide range of applications with a set of buttons up to a 2D touch sensing device; It's powerful design for below applications.

- Tablets
- E-book
- Navigation systems, GPS
- Game consoles
- POS (Point of Sales) devices
- Portable MP3 and MP4 media players
- Digital cameras

FT5536G support Touch Panel, the spec is listed in the following table,

Part Number	Package	TX	RX	Total Channels	Recommended for Smart Phone TP Size
FT5536G	QFNL 6x6x0.6mm Pitch =0.35mm	22	28	50	□8”

2. FUNCTIONAL BLOCK DESCRIPTION

2.1. Architecture Overview

Figure2-1 shows the overall architecture for the FT5536G.

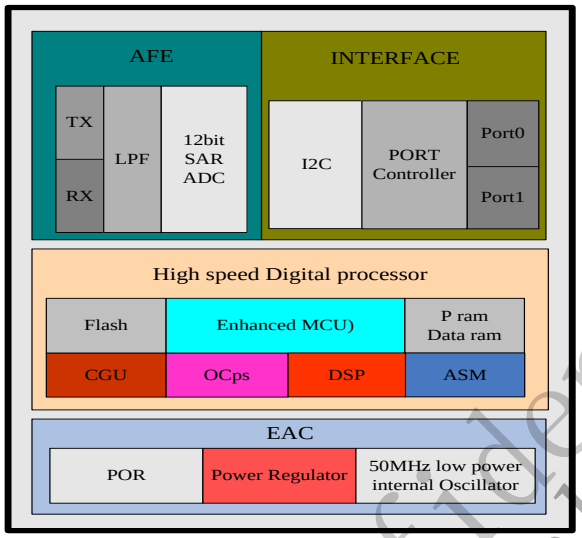


Figure 2-1 System Architecture Diagram

The FT5536G is comprised of five main functional parts listed below,

- **Touch Panel Interface Circuits**

The main function for the AFE and AFE controller is to interface with the touch panel. It scans the panel by sending AC signals to the panel and processes the received signals from the panel. It includes both Transmit (TX) and Receive (RX) functions. Key parameters to configure this circuit can be sent via serial interfaces.

- **Enhanced MCU with DSP accelerator**

For the Enhanced MCU, larger program and data memories are supported. Furthermore, a Flash memory is implemented to store programs and some key parameters.

Complex signal processing algorithms are implemented by MCU and DSP accelerator to detect the touches reliably and efficiently. Communication protocol software is also implemented in this MCU to exchange data and control information with the host processor.

- **External Interface**
  - I2C: an interface for data exchange with host
  - INT: an interrupt signal to inform the host processor that touch data is ready for read
  - RSTN: an external low signal reset the chip. The port is also use to wake up the FT5536G from the Sleep mode.
- **A watch dog timer is implemented to ensure the robustness of the chip.**
- **A voltage regulator to generate 1.8V for digital circuits from the input VDD3 supply**
- **Power On Reset (POR) is active until VDDD is higher than some level and hold decades of μs.**

2.2. MCU

This section describes some critical features and operations supported by the enhanced MCU.

Figure 2-2 shows the overall structure of the MCU block. In addition to the enhanced MCU core, we have added the following circuits,

- A DSP accelerator cooperates with MCU to process the complex algorithms
- Timer: A number of timers are available to generate different clocks
- Clock Manager: To control various clocks under different operation conditions of the system

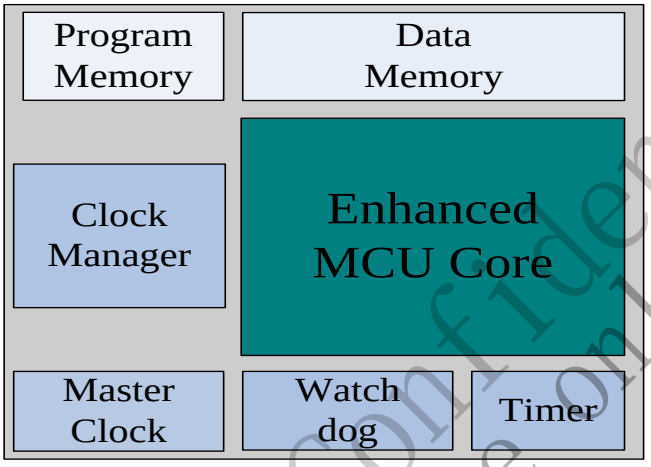


Figure 2-2 MCU Block Diagram

2.3. Operation Modes

FT5536G offers following three modes:

- **Active Mode**

When in this mode, FT5536G actively scans the panel. The default scan rate is 100 frames per second. The host processor can configure it to speed up or to slow down.

- **Monitor Mode**

In this mode, FT5536G scans the panel at a reduced speed. The default scan rate is 25 frames per second and the host processor can increase or decrease this rate. In this mode, most algorithms are stopped. A simpler algorithm is being executed to determine if there is a touch or not. When a touch is detected, FT5536G shall enter the Active mode immediately to acquire the touch information quickly. During this mode, the serial port is closed and no data shall be transferred with the host processor.

- **Sleep Mode**

In this mode, the chip is set in a power down mode. It shall only respond to the “RESET” signal from the host processor. The chip therefore consumes very little current, which help prolong the standby time for the portable devices.

2.4. Interface

Figure 2-3 shows the interface between a host processor and FT5536G. This interface consists of the following three sets of signals:

- Serial Interface
- Interrupt from FT5536G to the Host
- Reset Signal from the Host to FT5536G

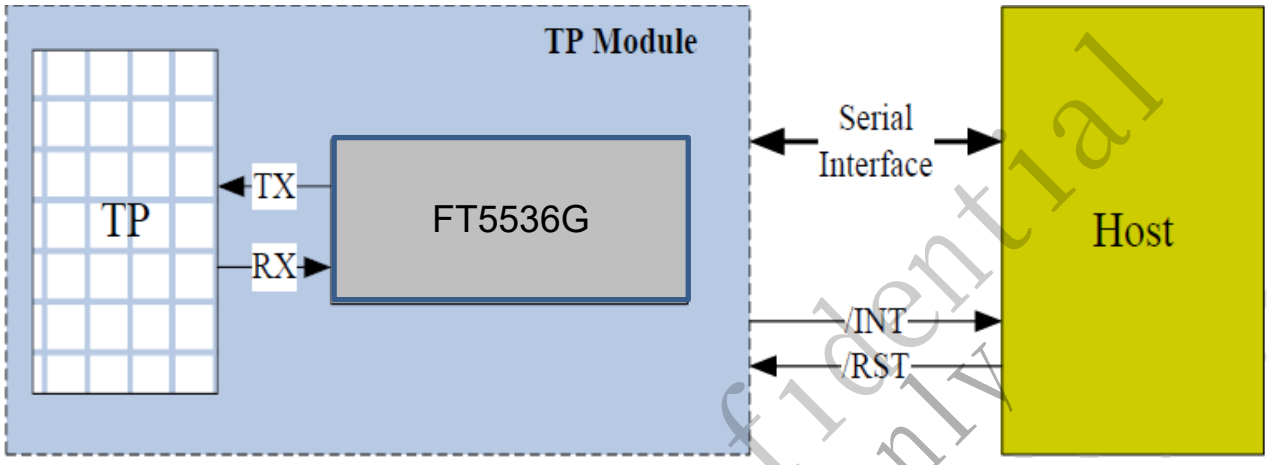


Figure 2-3 Host Interface Diagram

The serial interface of FT5536G is I2C. The detail of the interface is described in detail in Section 2.5. The interrupt signal (/INT) is used for FT5536G to inform the host that data are ready for the host to receive. The /RST signal is used for the host to wake up FT5536G from the Sleep mode. After resetting, FT5536G shall enter the Active mode.

2.5. Serial Interface

- **I2C Interface**

FT5536G supports the I2C interfaces, which can be used by a host processor or other devices.
The default I2C address is 0x70 and can be changed to the other assigned address by setting.
The I2C is always configured in the Slave mode. The data transfer format is shown in **Figure 2-4**.

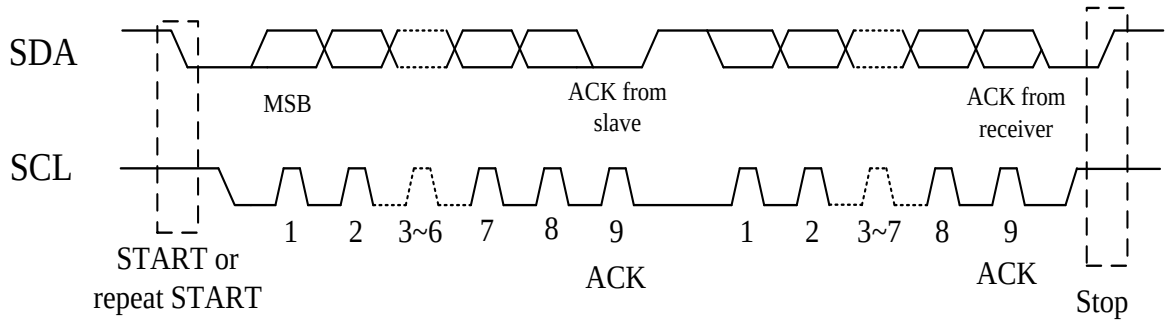


Figure 2-4 I2C Serial Data Transfer Format

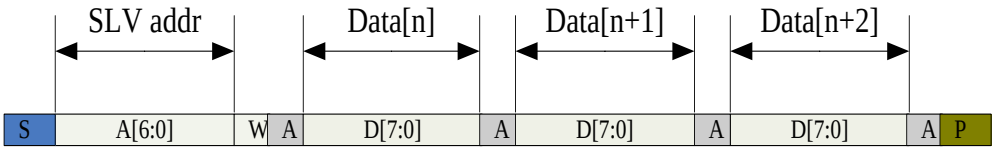


Figure 2-5 I2C master write, slave read

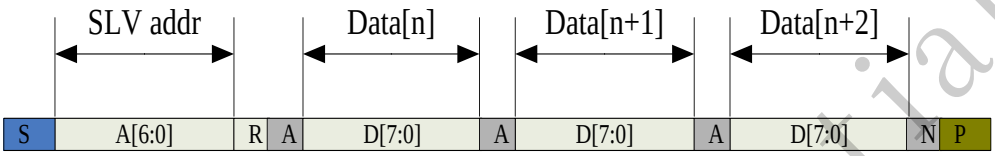


Figure 2-6 I2C master read, slave write

Table 2-1 lists the meanings of the mnemonics used in the above figures.

Table 2-1 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/ W	READ/WRITE bit, '1' for read, '0'for write
A(N)	ACK(NACK) bit
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table 2-2.

Table 2-2 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	0	400	KHz
Bus free time between a STOP and START condition	1.3		us
Hold time (repeated) START condition	0.6		us
Data setup time	100		ns
Setup time for a repeated START condition	0.6		us
Setup Time for STOP condition	0.6		us

3. ELECTRICAL SPECIFICATIONS

3.1. Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Power Supply Voltage	VDD3 – VSS	2.7 ~ +3.6	V	1, 2
I/O Digital Voltage	IOVCC	1.7~ +3.6	V	1
Operating Temperature	Topr	-40 ~ +85	□	1
Storage Temperature	Tstg	-55 ~ +150	□	1
ESD “Human Body Mode”	HBM	8000	V	3
ESD “Charged Device Mode”	CDM	≧1000	V	4
Latch up	I latch-up	+/-200@1.5Vmax	mA	5

Notes

1. If used beyond the absolute maximum ratings, FT5536G may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.
2. Make sure VDD (high) ≥VSS (low)
3. ESD HBM refers to ANSI/ESDA/JEDEC JS-001-2014.
4. ESD CDM is based on JESD22-C101-E.
5. Latch up refers to JESD78

3.2. DC Characteristics

Table 3-2 DC Characteristics

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high-level voltage	VIH	V		0.7 x IOVCC	--	IOVCC+0.3	
Input low -level voltage	VIL	V		-0.3	--	0.3 x IOVCC	
Output high -level voltage	VOH	V		0.7 x IOVCC	--	--	
Output low -level voltage	VOL	V		--	--	0.3 x IOVCC	
I/O leakage current	ILI	uA		-1	--	1	
Current consumption (Normal operation mode)	Iopr	mA	Report Rate 100Hz, 1 Fingers	12	12.24	-	VDD3=2.8V
Current consumption (Monitor mode)	Imon	mA	Report Rate 30Hz	0.5	0.54	-	VDD3=2.8V
Current consumption (Sleep mode)	Islp	uA		10	42	-	VDD3=2.8V
Step-up output voltage	VDD5	V	VDD3=2.8V	-	5V	-	-
Power Supply voltage	VDD3	V		2.7	--	3.6	-

Notes:

This sample data is intended for design guidance only. Values shown are typical for a 22Tx × 28Rx sensor configured at 100 Hz report rate. Actual current will depend on the particular sensor design and firmware options. The DC characteristics are tested under the temperature 25℃.

3.3. AC Characteristics

AC Characteristics of Oscillators

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
OSC clock 1	fosc1	MHz	VDD3=2.8V; Ta=25℃	49	50	51	

Table 3-3 AC Characteristics of TX

Item	Symbol	Test Condition	Min	Typ	Max	Unit	Note
TX acceptable clock	ftx		50	150	400	KHz	

3.4. I/O Ports Circuits

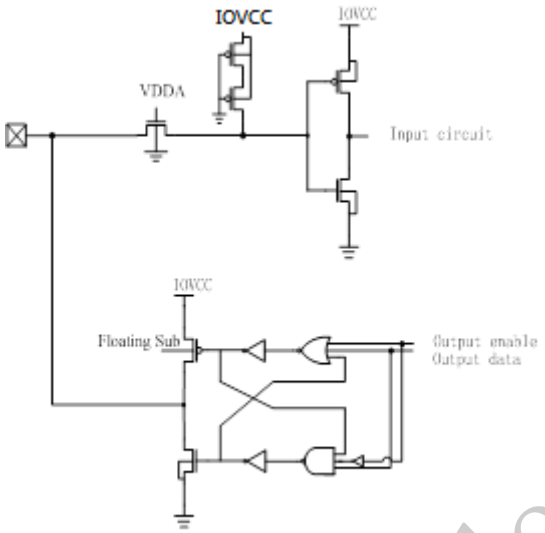


Figure 3-1 General Purpose *In/Out Port Circuit.*

The input/output property can be configured via firmware setting. The firmware can also control its output behavior as push-pull or as open-drain that SDA of I2C interface is required.

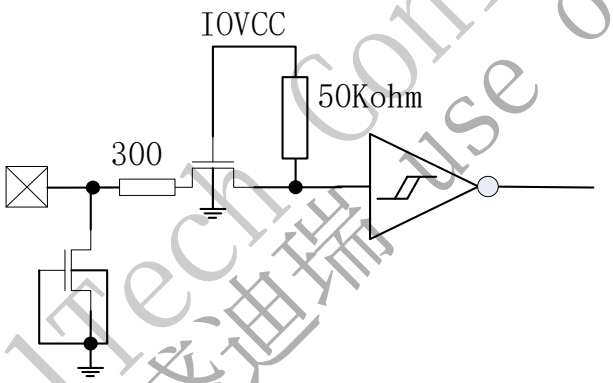


Figure 3-2 Reset Input Port Circuits

3.5. Power ON/ Reset Sequence

Reset should be pulled down to be low before powering on and powering down. I2C shouldn't be used by other devices during Reset time after VDD powering on (Trtp). INT signal will be sent to the host after initializing all parameters and then start to report points to the host.

If Power is down, the voltage of supply must be below 0.3V and Tpdt is more than 1ms.

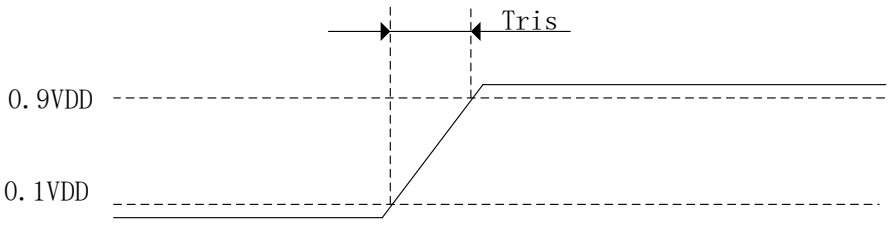


Figure 3-3 Power on time

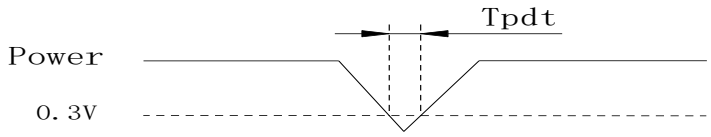


Figure 3-4 Power Cycle requirement

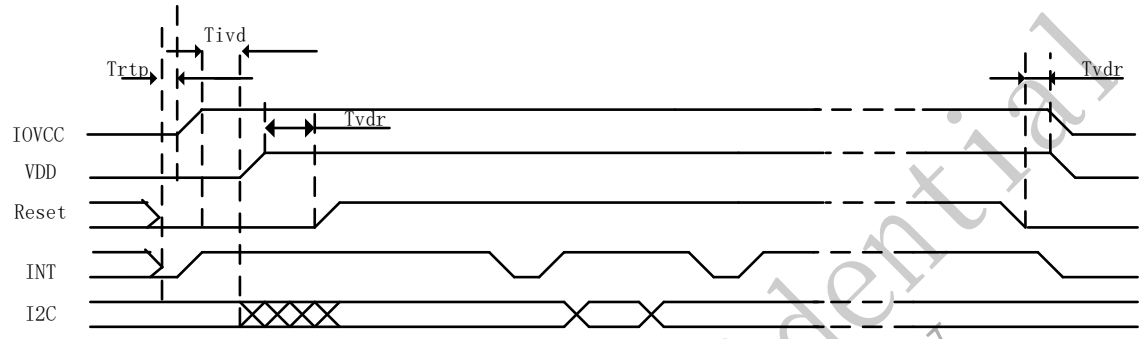


Figure 3-5 Power on Sequence

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on.

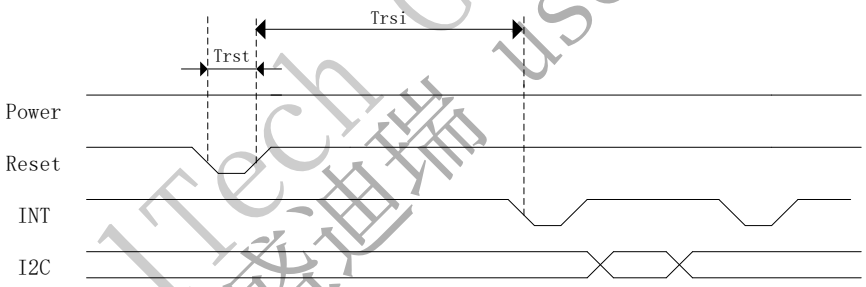


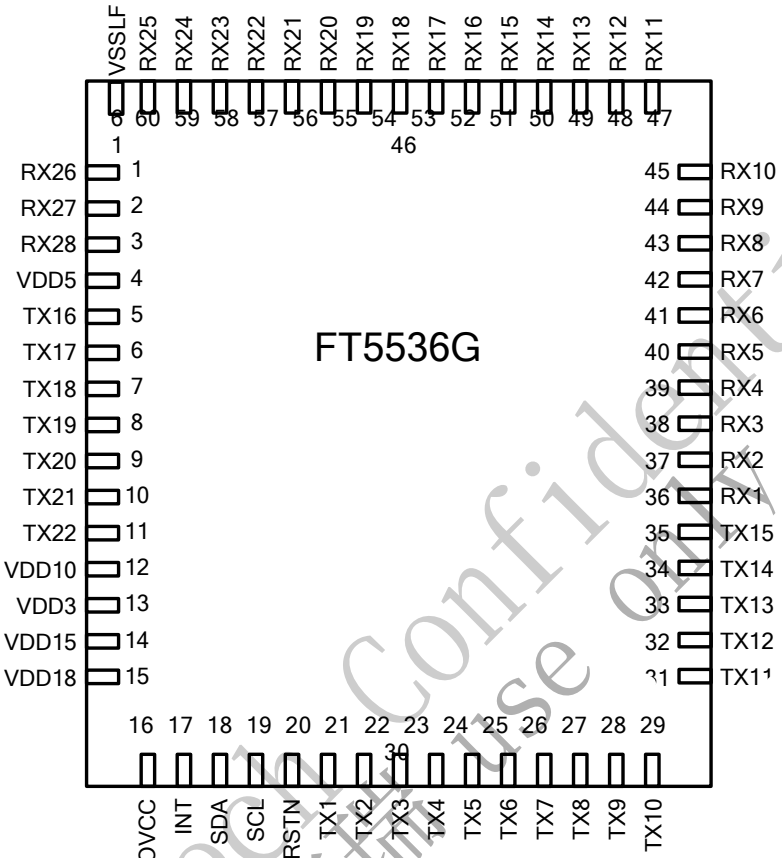
Figure 3-6 Reset Sequence

Table 3-5 Power on/Reset Sequence Parameters

Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	--	5	ms
Tpdt	Time of the voltage of supply being below 0.3V	5	--	ms
Trtp	Time of resetting to be low before powering on	100	--	μs
Tivd	Delay time of VDD powering on after IOVCC	10		μs
Tvdr	Reset time after VDD powering on	1	--	ms
Trsi	Time of starting to report point after resetting	--	200	ms
Trst	Reset time	1	--	ms

4. PIN CONFIGURATIONS

Pin List of FT5536G



FT5536G Package Diagram

Table 4-1 Pin Definition

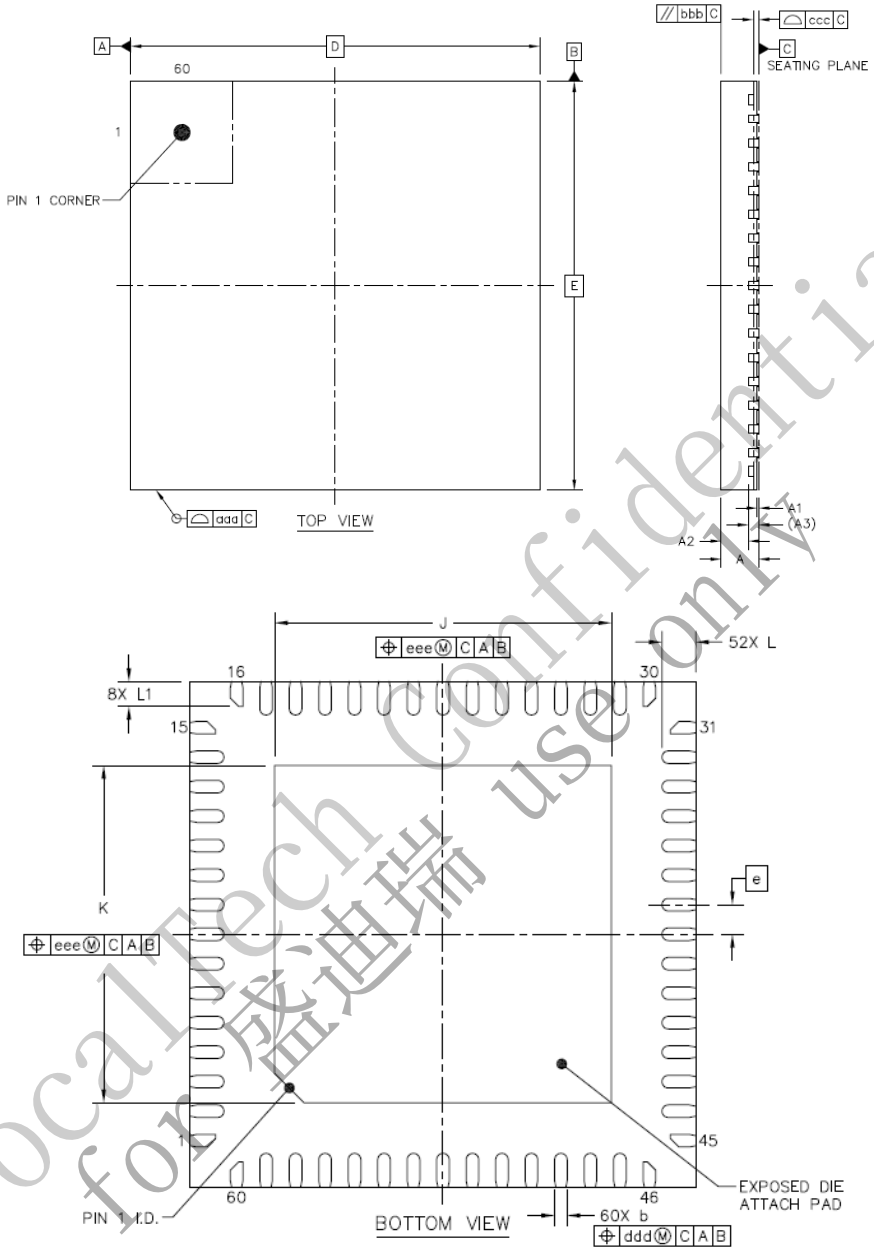
Table 4-1 Pin Definition

Name	Pin No.	Type	Description
	FT5536G		
RX28	3	I	Receiver input pins
RX27	2	I	Receiver input pins
RX26	1	I	Receiver input pins
RX25	60	I	Receiver input pins
RX24	59	I	Receiver input pins
RX23	58	I	Receiver input pins
RX22	57	I	Receiver input pins
RX21	56	I	Receiver input pins
RX20	55	I	Receiver input pins
RX19	54	I	Receiver input pins
RX18	53	I	Receiver input pins
RX17	52	I	Receiver input pins
RX16	51	I	Receiver input pins
RX15	50	I	Receiver input pins
RX14	49	I	Receiver input pins
RX13	48	I	Receiver input pins
RX12	47	I	Receiver input pins
RX11	46	I	Receiver input pins
RX10	45	I	Receiver input pins
RX09	44	I	Receiver input pins
RX08	43	I	Receiver input pins
RX07	42	I	Receiver input pins
RX06	41	I	Receiver input pins
RX05	40	I	Receiver input pins
RX04	39	I	Receiver input pins
RX03	38	I	Receiver input pins
RX02	37	I	Receiver input pins
RX01	36	I	Receiver input pins
TX15	35	O	Transmit output pin
TX14	34	O	Transmit output pin
TX13	33	O	Transmit output pin
TX12	32	O	Transmit output pin
TX11	31	O	Transmit output pin
TX10	30	O	Transmit output pin
TX09	29	O	Transmit output pin
TX08	28	O	Transmit output pin
TX07	27	O	Transmit output pin
TX06	26	O	Transmit output pin
TX05	25	O	Transmit output pin

Name	Pin No. FT5536G	Type	Description
TX04	24	O	Transmit output pin
TX03	23	O	Transmit output pin
TX02	22	O	Transmit output pin
TX01	21	O	Transmit output pin
VDD5	4	PWR	Internal generated 5V power supply, A 1μF ceramic capacitor to ground is required.
TX16	5	O	Transmit output pin
TX17	6	O	Transmit output pin
TX18	7	O	Transmit output pin
TX19	8	O	Transmit output pin
TX20	9	O	Transmit output pin
TX21	10	O	Transmit output pin
TX22	11	O	Transmit output pin
VDD10	12	PWR	Digital power supply, A 1μF ceramic capacitor to ground is required.
VDD3	13	PWR	Digital power supply, A 1μF ceramic capacitor to ground is required.
VDD15	14	PWR	Digital power supply, A 1μF ceramic capacitor to ground is required.
VDD18	15	PWR	Digital power supply, A 1μF ceramic capacitor to ground is required.
IOVCC	16	PWR	I/O power supply
INT	17	I/O	Interrupt request to the host, or Wakeup request from the host.
SDA	18	I/O	I2C data input and output
SCL	19	I/O	I2C clock input
RSTN	20	I	External Reset, Low is active
VSSLF	61	PWR	Analog ground

5. PACKAGE INFORMATION

5.1. Package Information of QFN-6x6-60L Package



Item		Symbol	Millimeter		
			Min	Type	Max
Total Thickness		A	0.5	0.55	0.6
Stand Off		A1	0	0.035	0.05
Mold Thickness		A2	----	0.4	----
L/F Thickness		A3	0.152 REF		
Lead Width		b	0.13	0.18	0.23
		b1	0.07	0.12	0.17
Body Size	X	D	6 BSC		
	Y	E	6 BSC		
Lead Pitch		e	0.35 BSC		
EP Size	X	J	3.9	4	4.1
	Y	K	3.9	4	4.1
Lead Length		L	0.35	0.4	0.45
		R	1.45	1.55	1.65
Package Edge Tolerance		aaa	0.1		
Mold Flatness		bbb	0.1		
Co Planarity		ccc	0.08		
Lead Offset		ddd	0.1		
Exposed Pad Offset		eee	0.1		

5.2. Order Information

Package Type	QFN
	60Pin(6 * 6)
	60Pin(0.6– P0.35)

Product Name	Package Type	# TX Pins	# RX Pins
FT5536G	QFN-60L	22	28

6. DISCLAIMER

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7. REVISION HISTORY

Date	Revision #	Description	Page	Auditor
Nov. 19, 2020	1.0	Original.	All	RD