[1] **Instruction:** addi sp, sp, -96

Opcode: 0010011 (7 bits)
Immediate: -96 (12 bits)
Source Register : sp (x2, 5 bits)(00010)
Destination Register: sp (x2, 5 bits)(00010)
Function :000 (3 bits)

[2] **Instruction:** sd s3, 56(sp)

Opcode: 0100011 (7 bits)
Immediate: 56 (12 bits)
Source Register: s3 (x2, 5 bits)(00010)
Base Register: sp (x2, 5 bits)(00010)
Function : 011 (3 bits)

[3] **Instruction:** mv s1, a1

Opcode: 0010011 (7 bits)
Immediate: 0 (12 bits)
Source Register: a1 (x11, 5 bits)(01011)
Destination Register: s1 (x9, 5 bits)(01001)
Function : 000 (3 bits)

[4] **Instruction:** sd ra, 88(sp)

Opcode: 0100011 (7 bits)
Immediate: 88 (12 bits)
Source Register: ra(x1, 5 bits)(00001)
Base Register: sp (x2, 5 bits)(00010)
Function : 011 (3 bits)

[5] **Instruction:** mv s4, a0

Opcode: 0010011 (7 bits)
Immediate: 0 (12 bits)
Source Register: a0 (x10, 5 bits)(01010)
Destination Register: s4(x20, 5 bits)(10100)
Function : 000 (3 bits)

[6] **Instruction:** jal ra, 14304<enormlz>

Opcode: 1101111 (7 bits)
Immediate: 14304(20 bits)
Destination Register: ra (x1, 5 bits)(00001)

[7] **Instruction:** addi s3, s3, -1

Opcode: 0010011 (7 bits)
Immediate: -1 (12 bits)
Source Register: s3 (x19, 5 bits)(10011)
Destination Register: s3(x19, 5 bits)(10011)
Function :000 (3 bits)

[8] **Instruction:** li a2, 0

Opcode: 0010011 (7 bits)
Immediate: 0 (12 bits)

Destination Register: a2(x12, 5 bits)(01100)

Function :000 (3 bits)

[9] **Instruction:** jal ra, 13d30<eshupl>

Opcode: 1101111 (7 bits)

Immediate: 13d30(20 bits)

Destination Register: ra (x1, 5 bits)(00001)

[10]**Instruction:** ld s0, 80(sp)

Opcode: 0000011 (7 bits)

Immediate: 80 (12 bits)

Source Register: sp(x2, 5 bits)(00010)

Destination Register: s0(x8, 5 bits)(01000)

Function :011 (3 bits)

[11]**Instruction:** li a4, 0

Opcode: 0010011 (7 bits)

Immediate: 0 (12 bits)

Destination Register: a4(x14, 5 bits)(01110)

Function :000 (3 bits)

[12]**Instruction:** bltu a3, a2, 14984<eiremain+0xe4>

Opcode: 1100011 (7 bits)

Immediate: 14984(12 bits)

Source Register: a2 (x12, 5 bits)(01100)

Destination Register: a3(x13, 5 bits)(101101)

Function :100 (3 bits)

[13]**Instruction:** lhu a2,-2(a5)

Opcode: 0000011 (7 bits)

Immediate: -2 (12 bits)

Source Register: a5(x15, 5 bits)(10011)

Destination Register: a2(x12, 5 bits)(10011)

Function :000 (3 bits)

[14]**Instruction:** bne s0, s3, 1492c<eiremain+0x8c>

Opcode: 1100011 (7 bits)

Immediate: 1492c (12 bits)

Source Register: s3(x19, 5 bits)(10011)

Destination Register: s0(x8, 5 bits)(01000)

Function :100 (3 bits)

[15]**Instruction:** ld ra, 88(sp)

Opcode: 0000011 (7 bits)

Immediate: 88(12 bits)

Source Register: sp(x2, 5 bits)(00010)

Destination Register: ra(x1, 5 bits)(00001)

Function :011 (3 bits)