Low Latency Radix-2^2 N-Point SDF Pipelined FFT VLSI Architectures for LTE-MIMO Applications

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Abstract. In this paper, a high throughput low latency Radix-22 N-Point (N = 128, 256, 512, 1024, 2048) single path delay feedback (SDF) pipelined-streaming input variable length fast Fourier transform (FFT) architectures has been proposed for Long Term Evolution (LTE) Multiple-Input-Multiple-Output (MIMO) applications. The proposed FFT architecture has been implemented by using Xilinx Artix-7 FPGA to analyze the performance metrics. The proposed FFT architectures have been designed and implemented to deliver throughput of 550 Mega-Samples-Per-Second (MSPS) at a sampling rate of 550 MHz clock frequency. Even though the proposed FFT architecture consumes additional Block-RAMs (BRAM) and quite an amount of Xilinx-Xtreme DSP/ DSP48 resources, the Power Delay Product (PDP) of the proposed FFT is excellent compared to the existing FFT architectures. The proposed pipelined FFT 2048-point architectures exhibits very less latency (11.382 µs at 550 MHz) as compared to the latency of existing system (56.88 µs at 200 MHz). Furthermore, the proposed FFT also shows an improvement of 2.75 times clock frequency and an improvement of 79.98% in latency. The proposed FFT architecture outperforms well in terms of high throughput, low latency and better Power Delay Product with extra hardware as trade-off.

Keywords: Pipeline, Throughput, Power Delay Product, Single Path Delay Feedback, VLSI Architecture.

1 Introduction

Fast Fourier Transformation (FFT)/Inverse Fast Fourier Transformation (IFFT) are the best frequency transformation techniques in wireless digital communication system. Further, Orthogonal Frequency Division Multiplexing (OFDM) System is one of the best digital communication mechanisms in which FFT/IFFT techniques are used to perform frequency transformation techniques [16]. FFT is used for converting the time domain signals into frequency domain

signals and IFFT is used for converting the frequency domain signals into time domain signals. In Single path delay feedback FFT (SDF-FFT) structure, high speed or high throughput operation can be achieved due to parallel structures which provides higher throughput but consumes more hardware resources [25].

Many different types of FFT architectures have been proposed in the literature, processing a different number of samples per iteration. For many high-speed applications, it is useful to process one or a few samples per iteration in a streaming manner. Suitable architectures for this are often referred to as pipeline FFT architectures [1]. As the name suggests, they consist of a pipeline of butterfly (BF) stages that consume either one (single stream [2]) or several (parallel stream [3]) samples per clock cycle. In this paper, single-stream pipeline FFT implementation is considered. However, many of the presented techniques are possible to utilize when mapping parallel stream FFT architectures to FPGAs.

A number of different single-stream FFT architectures have been proposed [1], [2], [4]–[10]. Most of these architectures are either variants of the single-path delay feedback (SDF) architecture [1], [2] or single-path delay commutator architecture [6] or in some cases combination [8], [9].The earlier attempts at optimizing the FPGA implementations of FFT cores are, however, mainly concentrated at the algorithmic and/or architectural level, or onthe mapping between algorithm and architecture. However, as is evident from this paper, significant improvements can be obtained when mapping a given FFT architecture, utilizing the architectural features of the FPGA. Hence, it is not only the FFT architecture that affects the results but also the mapping to the hardware.

Fixed length FFT processors are proposed by Derafshi et al. in [11], specific FFT size and specific standard was discussed by K. George et al. in [12] and a lower power FFT was focused by Y.-T.Lin et al. in [13]. FFT processor presented by B.Wang et al. in [14] focuses on higher speed and supports only 64-point FFT computation. D.Revanna [15] presented the design and implementation of scalable FFT processor for wire-less applications with the clock frequency as 200 MHz and the maximum throughput as 200 Mega-Samples-Per-Second (MSPS). K. Vijayakanthan et al. [16] presented the pipelined FFT for low power OFDM application. High-speed pipelined SDF-FFT processor using Vedic-multiplier was discussed in [17]. A low power pipelined Radix-2 mixed SDC-SDF FFT architecture was presented in [18].

Efficient FPGA mapping techniques of pipeline SDF-FFT cores to minimize the resource utilization was proposed in [19].A pipeline digit-slicing multiplier-less Radix-22 SDF-FFT structure was presented in [20]. A new low-power butterfly unit for single-path delay feedback FFT architectures was discussed in [21].Optimized implementations of two different pipeline FFT processors were presented in [22] and an efficient MIMO-OFDM Radix-2 single-path delay

feedback FFT Implementation on FPGA was presented in [23], [24]. A new FFT architecture for 4 × 4 MIMO-OFDMA systems with variablesymbol lengths was proposed in [25]. This algorithm has the computational complexity of radix-4 FFT algorithm, but retains the simplicity and regularity of radix-2 FFT algorithm. The main advantage of this radix-22 algorithm is that the number of non-trivial multiplications is reduced. The rest of the paper is organized as: Section 2 describes the proposed FFT architecture whereas the simulation results and analysis are discussed in Section 3. Finally, Section 4 concludes the paper.

2 Proposed FFT Architecture

In the Radix -2 SDF architecture for 2k point FFT in each stage, the required N/2 butterfly operations are time multiplexed onto one butterfly operator. Delay buffers are used to support the time-multiplexing. The inter-stage multipliers are used to multiply stage outputs by twiddle factor WNkn. The radix-2 SDF architecture required log2N-1 inter-stage complex multipliers, 2 log2N complex adders, and N-1 delay buffers. This Radix-22pipelined streaming input based variable length SDF-FFT has been implemented in Xilinx Artix-7 FPGA. The proposed FFT has been designed and implemented to deliver high throughput for the LTE-MIMO Applications. The proposed variable length FFT architecture support all word length supported by the LTE Standard. The word lengths supported by the proposed FFT is 128, 256, 512, 1024 and 2048. The proposed FFT provides a maximum throughput of 550 MSPS at the Maximum Clock frequency of 550 MHz which is 2.75 times faster than the existing [15] variable length FFT architecture. The FFT architecture [15] delivers a maximum throughput of 200 MSPS at the maximum clock rate of 200 MHz. The Radix-4 butterfly structure has been shown in Fig. 1. The generic SDF-FFT architecture has been shown in Fig. 2. The proposed Pipelined SDF-FFT architecture has been depicted in Fig.3. The sample input and output waveform of the FFT has been shown in Fig. 4.

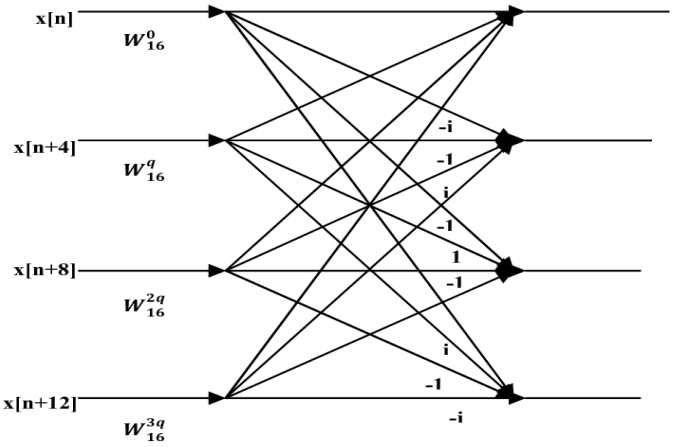

Fig. 1. Radix-4 butterfly

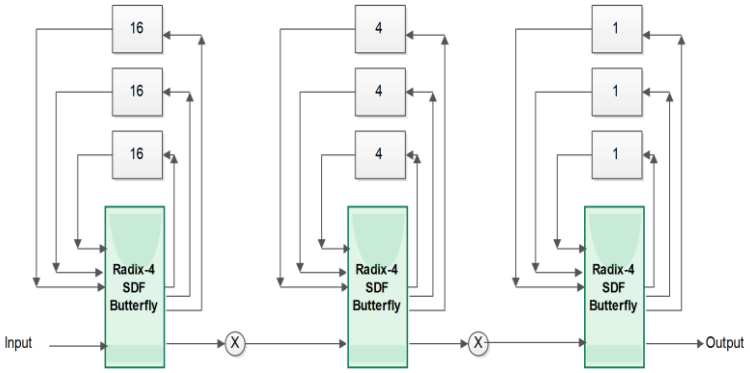

Fig. 2. Single-path Delay Feedback FFT Architecture

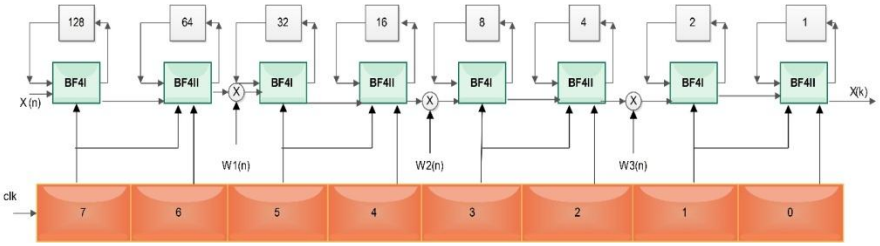

Fig. 3. Proposed Radix-2^2 Pipelined SDF-FFT

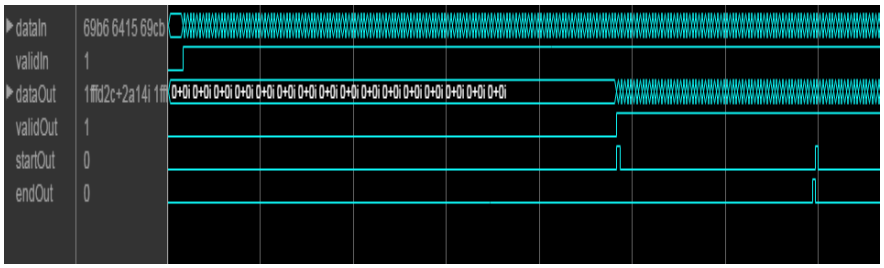

Fig. 4. Proposed Radix-2^2 Pipelined SDF-FFT

The hardware resources of Xilinx Artix-7 FPGA such as Block RAMs (BRAM), Multipliers, Adders, Xilinx Xtreme DSP Blocks and CLBs were used to implement the propose Radix-4 SDF-FFT with high throughput. The higher throughput has been achieved by utilizing pipelined architecture by sacrificing additional hardware blocks as trade-off in the proposed FFT whereas the Power Delay Product (PDP) of the proposed FFT is excellent while compared to the existing FFT Architecture [15]. Hence the proposed FFT architecture has to be preferred for low power and high throughput FFT such as in MIMO-OFDM Receivers for LTE applications.

3 Simulation Results and Discussions

The proposed FFT architecture has been implemented in Xilinx Artix-7 FPGA and supports the word length of 128, 256, 512, 1024 and 2048 bits. The simulation parameters were listed out in Table 1.

Table 1. Simulation Parameters

Items	Description
Radix	2^2
Type	Pipelined Streaming Input
Word Length - LTE	128, 256, 512, 1024, 2048
Clock Frequency (MHz)	550
Throughput (MSPS)	550
Input Size	16
Output Size	16
Xilinx FPGA	Artix-7
DSP Slice	Xilinx Xtreme DSP
Multipliers	4
Optimization	High Throughput
Application	LTE-MIMO

The comparative analysis of the performance metrics of the proposed FFT with the existing FFT architectures were listed out in Table 2. From the comparative analysis it is evident the proposed FFT outperforms well in terms of minimum latency of 3.933 µs and high throughput of 550 MSPS compared to the other FFT architectures. The computation time of the existing FFT [15] for FFT length of 2048 is 56.88 µs and the maximum throughput is 200 MSPS at the maximum clock frequency of 200 MHz. The performance metrics of the other FFT architecture in the literature were also listed out. The maximum throughput and minimum computation time are achieved at the cost of additional hardware resources as a trade-off.

Table 2. Comparison of FFT Computation Time with Existing FFT Processors

Technique	**Latency (µs)**						**Frequency (MHz)**	**Scalable Architecture**
	64	**128**	**256**	**512**	**1024**	**2048**		
[11]	-	-	-	-	26	-	100	No
[12]	-	40.34	47.30	52.30	61.14	-	470	Yes
[13]	-				-	57	17.86	Yes
[14]	2.1	-	-	-	-	-	31.69	No
[15]	1.27	2.6	5.53	11.98	26.11	56.88	200	Yes
[18]	12.84	-	-	-	-	-	43.181	No
[19]	-	-	-	-	3.58	-	294	No
[22]	0.27	-	1.08	-	4.35	-	236.7	No
[23]	1.13	2.28	4.70	10.45	23.31	-	55.66	No
Proposed	-	0.698	1.222	2.266	3.933	11.382	550	Yes

Table 3. Performance Metrics of FFT Length = 128

Technique	No of Xtreme DSP Slices	No of Clock Cycles	Frequency (MHz)	Computation (µs)	Total Power (mW)	Power Delay Product (PDP)	Throughput (MSPS)
[15]	4	520	200	2.6	407.83	1060.35	200
Proposed Pipelined-Streaming	9	349	550	0.698	389.12	271.60	550

Table 4. Performance Metrics of FFT Length = 256

Technique	No of Xtreme DSP Slices	No of Clock Cycles	Frequency (MHz)	Computation (µs)	Total Power (mW)	Power Delay Product (PDP)	Throughput (MSPS)
[15]	-	1106	200	5.53	434.20	2401.12	200
Proposed Pipelined-Streaming	9	611	550	1.222	404.35	494.11	550

Table 5. Performance Metrics of FFT Length = 512

Technique	No of Xtreme DSP Slices	No of Clock Cycles	Frequency (MHz)	Computation (µs)	Total Power (mW)	Power Delay Product (PDP)	Throughput (MSPS)
[15]	-	2396	200	5.1	428.57	2185.70	200
Proposed Pipelined-Streaming	9	1133	550	2.266	622.09	1409.65	550

Table 6. Performance Metrics of FFT Length = 1024

Technique	No of Xtreme DSP Slices	No of Clock Cycles	Frequency (MHz)	Computation (µs)	Total Power (mW)	Power Delay Product (PDP)	Throughput (MSPS)
[15]	-	5222	200	26.11	432.01	11279.78	200
[19]	16	1054	294	4.58	-	-	294
[22]	16	1042	235.6	4.35	-	-	235.6
Proposed Pipelined-Streaming	16	2163	550	3.933	1105.95	4349.701	550

The performance metrics the proposed FFT with the word length as 128 has been depicted in Table 3. The throughput of the proposed 128-point FFT architecture is 550 MSPS at the clock frequency of 550 MHz and the FFT computation time is

0.698 µs whereas the computation time of the existing FFT [15] is 2.6 µs. The total power consumption of the proposed FFT is 389.12 mW whereas it is 407.83mW for the existing FFT. Similarly, the performance metrics the proposed FFT with the word length as 256 has been depicted in Table 4. The throughput of the proposed 256-point FFT architecture is 550 MSPS at the clock frequency of 550 MHz and the FFT computation time is 1.222 µs whereas the computation time of the existing FFT [15] is 5.53 µs. The total power consumption of the proposed FFT is 404.35mW whereas it is 434.20mW for the existing FFT.

The performance metrics the proposed FFT with the word length as 512 has been depicted in Table 5. The throughput of the proposed 512-point FFT architecture is 550 MSPS at the clock frequency of 550 MHz and the FFT computation time is 2.266 µs whereas the computation time of the existing FFT [15] is 5.1 µs. The total power consumption of the proposed FFT is 622.09mW whereas it is 428.57mW for the existing FFT. Similarly, the performance metrics the proposed FFT with the word length as 1024 has been depicted in Table 6. The throughput of the proposed 1024-point FFT architecture is 550 MSPS at the clock frequency of 550 MHz and the FFT computation time is 3.933 µs whereas the computation time of the existing FFT [15] is 26.11 µs. The total power consumption of the proposed FFT is 1105.95mW whereas it is 432.01mW for the existing FFT.The performance metrics the proposed FFT with the word length as 2048 has been depicted in Table 7. The throughput of the proposed 2048-point FFT architecture is 550 MSPS at the clock frequency of 550 MHz and the FFT computation time is 211.382 µs whereas the computation time of the existing FFT [15] is 56.88 µs. The total power consumption of the proposed FFT is 1658.82mW whereas it is 434.44mW for the existing FFT. Whereas the FFT for MIMO application exhibits a very low throughput of 24 MSPS at the clock frequency of 24 MHz.

Table 7. Performance Metrics of FFT Length = 2048

Technique	No of Xtreme DSP Slices	No of Clock Cycles	Frequency (MHz)	Computation (µs)	Total Power (mW)	Power Delay Product (PDP)	Throughput (MSPS)
[15] Single	-	11376	200	56.88	434.44	24710.95	200
[25] MIMO	192	-	24	-	-	-	24
Proposed Pipelined-Streaming	24	6260	550	11.382	1658.82	18880.69	550

Table 8. FFT Length vs Number of Clock Cycles

FFT Length	Number of Clock Cycles		
	Existing [15]	Proposed FFT	Improvement (%)
128	520	349	32.88
256	1106	611	44.75
512	2396	1133	52.71
1024	5222	2163	58.57
2048	11376	6260	44.97

The impact of FFT length on the number of clock cycles to complete the FFT operation has been tabulated in Table 8. Different FFT lengths and the corresponding number of clock cycles for the existing FFT [15] and the proposed FFT architecturesare exhibited. As the FFT length increases, the number of clock cycles to complete the FFT operation also increases. The percentage of improvement for the number of clock cycles for different FFT length are listed out.

The impact of FFT length on the FFT computation time to complete the FFT operation has been tabulated in Table 9. Different FFT lengths and the corresponding FFT computation timefor the existing FFT [15] and the proposed FFT architectures are exhibited. As the FFT length increases, FFT computation timeto complete the FFT operation also increases. The percentage of improvement for the FFT computation timefor different FFT length are listed out.

Table 9. FFT Length vs FFT Computation Time (µs)

FFT Length	**FFT Computation Time (µs)**		
	Existing [15]	**Proposed FFT**	**Improvement (%)**
128	2.6	0.698	73.15
256	5.53	1.222	77.90
512	11.98	2.266	81.08
1024	26.11	3.933	84.93
2048	56.88	11.382	79.98

Table 10. Comparative Analysis of Power Delay Product (PDP)

FFT Length	Power Delay Product		
	Existing [15]	Proposed FFT	Improvement (%)
128	1060.35	271.60	74.38
256	2401.12	494.11	79.42
512	2185.70	1409.65	35.50
1024	11279.78	4349.701	61.43
2048	24710.95	18880.69	23.59

The impact of FFT length on the Power Delay Product of the FFT operation has been tabulated in Table 10. Different FFT lengths and the corresponding Power Delay Product for the existing FFT [15] and the proposed FFT architectures are exhibited. As the FFT length increases, Power Delay Product to complete the FFT operation also increases. The percentages of improvement of Power Delay Product of for different FFT length are listed out.

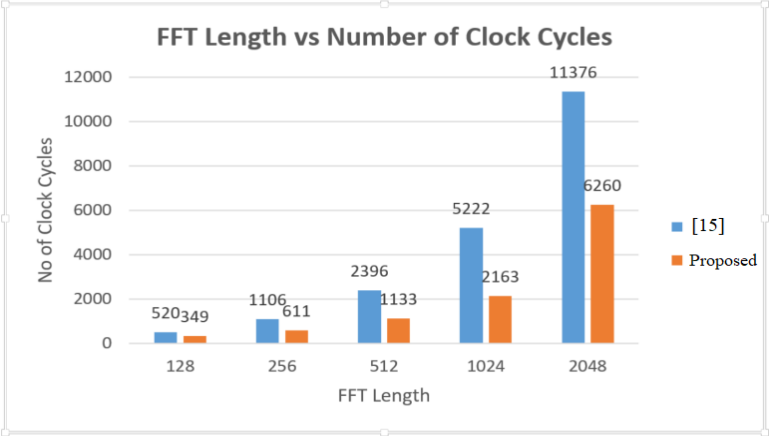

Fig. 5. Impact of FFT Length on the Number of Clock Cycles

The impact of FFT length on the number of clock cycles to complete the FFT operation has been shown in Fig. 5. Different FFT lengths and the corresponding number of clock cycles for the existing FFT [15] and the proposed FFT architectures are exhibited. As the FFT length increases, the number of clock cycles to complete the FFT operation also increases. The impact of FFT length on the FFT computation time to complete the FFT operation has been depicted in Fig. 6. Different FFT lengths and the corresponding FFT computation time for the existing FFT [15] and the proposed FFT architectures are exhibited. As the FFT length increases, FFT computation time to complete the FFT operation also increases.

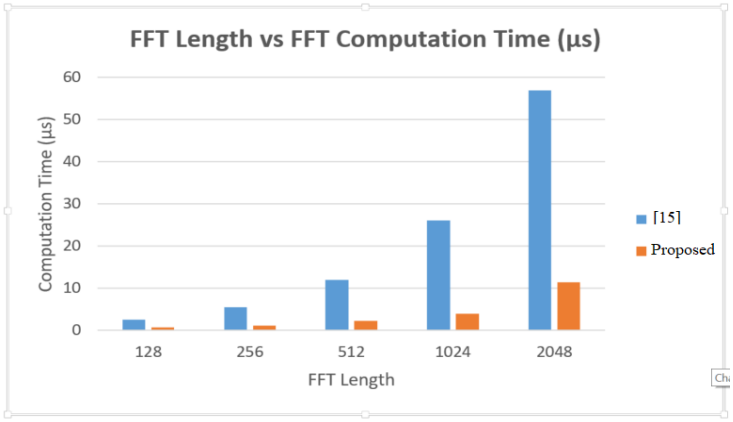

Fig. 6. Impact of FFT Length on the FFT Computation Time

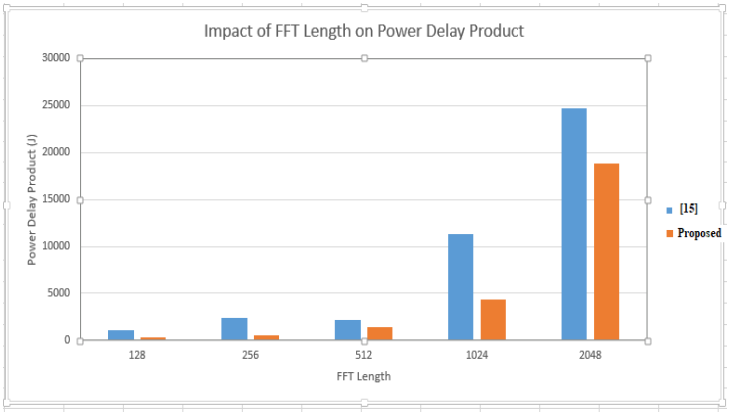

Fig. 7. Impact of FFT Length on the Power Delay Product (PDP)

The impact of FFT length on the Power Delay Product of the FFT operation has been exhibited in Fig. 7. Different FFT lengths and the corresponding Power Delay Product for the existing FFT [15] and the proposed FFT architectures are exhibited. As the FFT length increases, Power Delay Product to complete the FFT operation also increases. The analysis of the PDP of the existing and the proposed FFT architectures from the graph proves that the proposed FFT outperforms well in terms of Power Delay Product even though there is an additional requirement on the hardware resources.

Table 11. Performance Metrics of FFT Length = 2048 for MIMO-OFDM

Technique	No of Xtreme DSP Slices	No of Clock Cycles	Frequency (MHz)	Computation (µs)	Total Power (mW)	Power Delay Product (PDP)	Throughput (MSPS)
[15] Single	-	11376	200	56.88	434.44	24,710.95	200
[25] 4x4 MIMO	192	45504	24	-	-	-	24
Proposed Pipelined-Streaming 4x4 MIMO	96	25040	2,200	45.528	6,635.28	30,2091.02	2,200

The performance metrics of the proposed FFT with the FFT Length of 2048 at the clock frequency of 550 MHz for LTE-MIMO application has been tabulated in Table 11. The proposed FFT for MIMO-OFDM delivers a maximum throughput of 2,200 MSPS at the clock frequency of 2,200 MHz for the 4x4 MIMO-OFDM Architecture with 4 Antennae whereas the FFT architecture which is proposed in [25] & [26] delivers 24 MSPS only at the clock frequency of 24 MHz. Moreover it utilizes 192 DSP slices and 45504 clock cycles to complete the FFT operation whereas the proposed FFT architecture utilizes 96 Xilinx Xtreme DSP blocks 25040 clock cycles to complete the FFT operation with an excellent throughput of 2200 MSPS with FFT computation time of 45.528 µs.

4 Conclusion

Single path Delay Feedback (SDF) Pipelined-streaming input Variable Length Fast Fourier Transform (FFT) Very Large Scale Integration (VLSI) architectures for Long Term Evolution (LTE)-Multiple-Input-Multiple-Output (MIMO) applications has been presented in this paper. The proposed FFT architecture delivers a throughput of 550 MSPS at the Maximum clock rate of 550 MHz. The proposed FFT support the FFT length of 128, 256, 512, 1024 and 2048 for LTE-MIMO Standard. The proposed FFT architecture has been implemented in Xilinx Artix-7 FPGA Device and the performance metrics have been analyzed.Even though the proposed FFT architecture consumes additional Block-RAMs (BRAM) and quite an amount of Xilinx-Xtreme DSP/ DSP48 resources, the Power Delay Product (PDP) of the proposed FFT is excellent compared to the existing FFT architectures. The proposed Radix-22 SDF 2048 point Pipelined FFT architectures exhibits very less latency of 11.382 µs at 550 MHz clock frequency compared to the existing system with the latency of 56.88 µs at 200 MHz clock frequency. The proposed FFT exhibits an improvement of 2.75 time clock frequency and an improvement of 79.98% in latency. The proposed FFT architecture outperforms well in terms high throughput, low latency and better Power Delay Product with extra hardware as trade-off for both for Single FFT and for MIMO also.

References

1. E. H. Wold and A. M. Despain, “Pipeline and parallel-pipeline FFT processors for VLSI implementations,” IEEE Trans. Comput., vol. C-33, no. 5, pp. 414–426, May 1984.
2. H. L. Groginsky and G. A. Works, “A pipeline fast Fourier transform,” IEEE Trans. Comput., vol. C-19, no. 11, pp. 1015–1019, Nov. 1970.
3. B. Gold and T. Bially, “Parallelism in fast Fourier transform hardware,” IEEE Trans. Audio Electroacoust., vol. 21, no. 1, pp. 5–16, Feb. 1973.
4. A. M. Despain, “Fourier transform computers using CORDIC iterations,” IEEE Trans. Comput., vols. C–23, no. 10, pp. 993–1001, Oct. 1974.
5. G. Bi and E. V. Jones, “A pipelined FFT processor for word-sequential data,” IEEE Trans. Acoust., Speech, Signal Process., vol. 37, no. 12, pp. 1982–1985, Dec. 1989.
6. L. Yang, K. Zhang, H. Liu, J. Huang, and S. Huang, “An efficient locally pipelined FFT processor,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 53, no. 7, pp. 585–589, Jul. 2006.
7. Y.-N. Chang, “An efficient VLSI architecture for normal I/O order pipeline FFT design,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 55, no. 12, pp. 1234–1238, Dec. 2008.
8. X. Liu, F. Yu, and Z.-K. Wang, “A pipelined architecture for normal I/O order FFT,” J. Zhejiang Uni. Sci. C., vol. 12, no. 1, pp. 76–82, Jan. 2011.
9. Z. Wang, X. Liu, B. He, and F. Yu, “A combined SDC-SDF architecturefor normal I/O pipelined radix-2 FFT,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 23, no. 5, pp. 973–977, May 2015.
10. M. Garrido, S.-J. Huang, S.-G. Chen, and O. Gustafsson, “The serial commutator FFT,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 63, no. 10, pp. 974–978, Oct. 2016.
11. Z.H. Derafshi, J. Frounchi, and H. Taghipour, “A high speed FPGA implementation of a 1024-point complex FFT processor” In Second International Conference on Computer and Network Technology (ICCNT), 2010, pp. 312-315, April 2010.
12. K. George and C.-I.H. Chen, “Configurable and expandable FFT processor for wideband communication,” In IEEE Instrumentation and Measurement Technology Conference Proceedings, 2007, IMTC 2007, pp. 1-6, May 2007.
13. Y.-T. Lin, P.-Y. Tsai and T.-D. Chiueh,“Low-power variable-length Fast Fourier Transform processor”, IEEE Proceedings - Computers and Digital Techniques, vol. 152, no. (4), pp. 499-506, July 2005.
14. Bingrui Wang, Qihui Zhang, TianyongAo, and Mingju Huang,“Design of pipelined FFT processor based on FPGA. In Second International Conference on Computer Modeling and Simulation, 2010, ICCMS '10, vol. 4, pp. 432-435, Jan. 2010.
15. Deepak Revanna, “Design and Implementation of Scalable FFT Processor for Wireless Applications”, Master of Science Thesis, Aug.2012.
16. K. Vijayakanthan, M.Anand, M.Janakirani, “Pipelined Fast Fourier Transform for Low Power OFDM Based Applications”, International Journal of Pure and Applied Mathematics, vol. 116, no. (23), pp. 371-376, 2017.
17. Tapsi Gupta and Jankiballabh Sharma, “A High-Speed Single-path Delay Feedback Pipeline FFT Processor using Vedic-Multiplier”, IEEE International Conference on Information, Communication, Instrumentation and Control (ICICIC-2017), pp. 1-6, 2017.

18. K. Malathy and B. Justus Rabi, “VLSI Based New Pipelined Architecture Design for Radix-2 FFT”, Research Journal of Applied Sciences, Engineering and Technology vol. 12, no. (3), pp. 339-346, 2016.
19. Carl Ingemarsson, PetterKällström, Fahad Qureshi and Oscar Gustafsson, “Efficient FPGA Mapping of Pipeline SDF FFT Cores”, IEEE Transactions On Very Large Scale Integration (VLSI) Systems, vol. 25, no.(9), pp. 2486-2497, 2017.
20. Yazan Samir Algnabi, Rozita Teymourzadeh, Masuri Othman and Md Shabiul Islam, “FPGA Implementation of Pipeline Digit-Slicing Multiplier-Less Radix 22 DIF SDF Butterfly for Fast Fourier Transform Structure”,European Conference on Antennas and Propagation (EUCAP2011), pp. 4168-4172, 2011.
21. Seung-Won Yang and Jong-Yeol Lee, “A new low-power butterfly unit for single-path delay feedback FFT architectures”, IEICE Electronics Express, vol. 10, no. (24), pp. 1-6, Aug. 2013.
22. Bin Zhou, Yingning Peng and David Hwang, “Pipeline FFT Architectures Optimized for FPGAs”, International Journal of Reconfigurable Computing, vol. 2009. pp. 1-9, Jan 2009.
23. Mohammed Dali1, Ryan M. Gibson, Abbes Amira, AbderezakGuessoum and Naeem Ramzan, “An Efficient MIMO-OFDM Radix-2 Single-Path Delay Feedback FFT Implementation on FPGA”,NASA/ESA Conference on Adaptive Hardware and Systems (AHS),pp. 1-7, 2015.
24. S. Ranjith and T. Vishnupriya, “Analysis and Design of SDF Architecture for MIMO Application”, Indian Journal of Science and Technology, Vol 9(8), pp. 1-5, Feb. 2016.
25. A. Karachalios, K. Nakos, D. Reisis and H. Alnuweiri, “A new FFT Architecture for 4 × 4 MIMO-OFDMA Systems with Variable Symbol Lengths”,International Conference on Innovations in Information Technology (IIT) pp. 80-84, 2009.
26. K. Hemachandran, G. Lakshman Chandra and H.Raghupathi, “Design of very high throughput with low complexity output MIMO decoder”, 2nd International Conference on Inventive Systems and Control (ICISC), pp.22-25.