Multipath delay cell-based coupled oscillators for $\Sigma\Delta$ Time-to-Digital Converters*

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Abstract. The multipath delay cell-based coupled ring oscillator for $\Sigma\Delta$ time-to-digital converters (TDC) is presented in this work. Unlike the traditional analog integrators, the ring oscillator integrator (ROI) can achieve theoretically infinite dc gain at low frequency. Moreover, the ROI inherently possesses the dynamic element matching (DEM) for shaping the mismatch between the delay cells. Two new multipath designs for coupled oscillators are proposed, which are simulated in UMC65, UMC40 and UMC28 CMOS technologies using Cadence Virtuoso Tools. Because of multipath techniques, the effective propagation delay is reduced well below the technology limit. This enables to achieve fine time resolution with stable phase noise performance for $\Sigma\Delta$ TDC.

Keywords: Sigma-Delta time-to-digital converter ($\Sigma\Delta$ TDC) · time-domain · coupled oscillator · ring oscillator integrator (ROI) · multipath · jitter · fan-out of 4 (FO4) delay · coupling factor · dynamic element matching (DEM).

1 Introduction

In this modern era of electronics, the scaling of process technology has a high impact on the integrated circuits in terms of system performance, fabrication cost and power consumption. The scaling is usually done to increase the integration density of the chip with enhanced functionality. The digital circuits whose performance is not affected by feature size of the device take full advantage of the scaling. With the reduced dimensions of the transistors, these circuits possess high switching speed, less power dissipation and occupy less area [3, 11].

On the contrary, the efficiency of the analog circuits is profoundly degraded with the technology scaling because of the decrease in supply voltage and the intrinsic gain but almost constant threshold voltage [1]. The reduction in the

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feature size of the transistor leads to the various second-order effects such as channel length modulation, velocity saturation, mobility degradation, threshold voltage variations and hot-carrier effects etc. So with the advancement in the process technology, the time-domain circuits are emerging as the best alternative to combat with the scaling-induced performance deterioration of the analog and mixed-signal circuits [3]. The time interval (T_{in}) between the rising edges of two digital signals, namely the *Start* and the *Stop* represents the time variable, as shown in Fig. 1. In a more matured sense, it is the pulse width modulation of the analog signal that it involves [11]. The time-to-digital converter (TDC) is a functional block of utmost importance in most of the analog and mixed-signal processing circuits because of its digital-friendly behavior. It measures the time interval and gives the digital representation of the time input. Initially, it was used in atomic and high-energy physics experiments as a precise time interval measurement unit that involves laser ranging such as in LIDAR (light detection and ranging) for time-of-flight estimation. With the technological advancements, the applications have been extended to all-digital phase-locked loops (ADPLLs) where the TDC acts as a phase-frequency detector (PFD), time-domain analog-to-digital converters (ADCs), temperature sensors and Serializer/Deserializer (SerDes) [11].

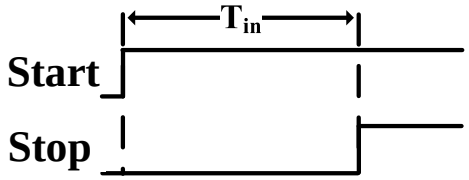

Fig. 1. The typical representation of time signal as the difference between the *Start* and *Stop* events

The Fan-out of 4 (FO4) delay is a technology-dependent parameter [9] used in the CMOS process, for quantifying the digital cell. As the technology scales down, the FO4 delay also becomes finer, leading to fast switching of the device. From Table 1, it is clear that, as the process scales from UMC65 to UMC28, the FO4 delay decreases from 31.35 ps to 18.12 ps.

Table 1. FO4 delay of the inverter in UMC technologies

Technology*	**FO4 Delay** (ps)
UMC65	31.35
UMC40	23.35
UMC28	18.12

*United Microelectronics Corporation.

Various researchers have investigated design of ring oscillators using multipath techniques [8, 4]. In [5], the precise delay generation with the improved resolution has been shown, which had used an array oscillator with M number of coupled ring oscillators. It has achieved the delay resolution of 101 ps at 141 MHz operating frequency. The oscillation frequency will be lessened if more output phases are involved. A high-speed ring oscillator was demonstrated in [7] for multiphase clock generation using the skewed delays, which had generated the oscillation frequency 50% higher than the conventional ring oscillators. In [6], low power and high-resolution multiphase generation system for coupled oscillators has been presented, which has achieved the resolution of 32 ps at 490 MHz with the phase accuracy of -1.0 to 0.8 LSB. The first order noise-shaped time-to-digital converter (TDC) using multipath gated ring oscillator was demonstrated in [4], which has attained a resolution of 6 ps with the oversampling rate of 50 MS/s. In [10], the second-order noise-shaped time-to-digital converter (TDC) using switched ring oscillator (SRO) and gated switched ring oscillator (GSRO) was presented, which has shown high OSR of 400 MS/s.

The subject of the multipath techniques to reduce the propagation delay has not been adequately addressed in the literature. In our present work, we have focused on the study of the multipath delay cell using the coupled ring oscillators in a more qualitative manner. The coupling factor is analysed and compared with the theoretical value. The paper is organized as follows. In Section 2, the details are given about the ring oscillator as an integrator with theoretically infinite dc gain at the sufficiently low operating frequency. Section 3 comprises of the multipath delay cell architecture for two topologies. The simulation results for UMC65, UMC40 and UMC28 CMOS technologies are compared and analysed in Section 4, and lastly, the conclusions are drawn in Section 5.

2 Ring Oscillator as an Integrator

The ring oscillators are widely used in phase-locked loops (PLLs), TDCs, time-domain ADCs, temperature sensors and SerDes to generate precise delays at high operating frequency because of their high delay linearity [3, 11]. If the delay of each inverter of the ring oscillator is identical, then the total oscillation period is uniformly divided into precise sub-delays. The inverter delay is equal to the period of oscillation divided by the twice of the number of inverters in the ring oscillator [9]. Although ring oscillators can generate high precision and high linearity delay, their resolution is limited to the inverter delay (τ_P) [8].

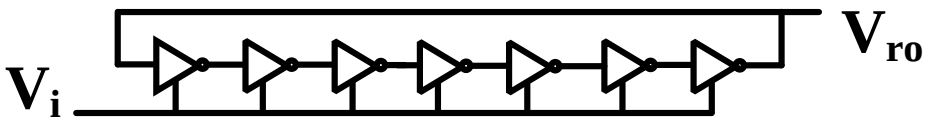

Fig. 2. Ring oscillator as V-to-ϕ integrator

The ring oscillator shown in Fig. 2 can be seen as an ideal voltage-to-phase (V-to-ϕ) integrator with theoretically infinite dc gain at low frequency and low supply voltages [2]. As the process scales down, the analog integrators such as G_m-C integrator or op-amp-RC integrator, which uses OTAs as the building block suffer from high non-linearity as their gain is limited to $g_m r_o$, since the output impedance of the operational amplifier drastically deteriorates. Moreover, the reduction of supply voltage significantly affects the voltage swing, therefore making it very difficult to improve the gain of the analog integrators. The efficiency of the analog integrators, which mostly relies on operational amplifiers, is highly compromised. Also, analog integrators are power-hungry. In contrary to the above integrators, the CMOS inverter-based ring oscillator that scales well with technology can act as an integrator in the phase domain. Also, these oscillators perform signal processing in the time-domain, so there is no issue of shrinking of voltage headroom and no performance loss due to scaling-induced imperfections. The ring oscillator integrator (ROI) consists of a ring oscillator with inverter delay stages, as shown in Fig. 2. The relationship between the output oscillator frequency (ω_{ro}) and input voltage (V_i) is given by the oscillator gain (A_{ROI}) and can be written as

$$A_{ROI} = \frac{d\omega_{ro}(t)}{dV_i(t)} \tag{1}$$

where A_{ROI} is the gain of the ring oscillator integrator. Since, we know that

$$\phi_{ro}(t) = \int w_{ro}(t)\, dt \tag{2}$$

Substituting (1) in (2), we get

$$\phi_{ro}(t) = A_{ROI} \times \int V_i(t)\, dt \tag{3}$$

Taking the Laplace Transform of the above equation, then the transfer function will be

$$H_{ROI}(s) = \frac{\phi_{ro}(s)}{V_i(s)} = \frac{A_{ROI}}{s} \tag{4}$$

From the above equation, it is evident that the transfer function of the output phase to the input voltage is inversely proportional to frequency. Hence, the ring oscillator integrator (ROI) can achieve theoretically infinite dc gain at low frequency irrespective of the variations in the device parameters or non-idealities due to the reduction of the output impedance of the transistor as noticed in the analog integrators. Thus, it acts as a lossless integrator, with transfer function independent of the transistor parameters. The modulus of the transfer function in the dB scale is plotted in Fig. 3. In the ring oscillator integrator (ROI), the mismatch between the delay-cells is first-order shaped. It achieves the dynamic element matching (DEM) by following the barrel shifting algorithm for delay cell selection [8, 4], as shown in Fig. 4. So the ring oscillator integrator (ROI) can be considered as the basic building block for the time-domain signal processing, which scales well with the CMOS technology.

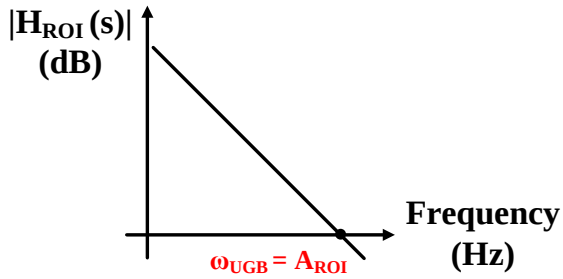

Fig. 3. Bode plot for the ring oscillator integrator (ROI)

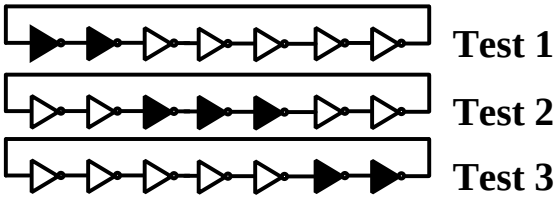

Fig. 4. Barrel shifting of ROI delay cells for dynamic element matching

3 Multipath Delay Cell

The delay cell is a crucial component in the design of the ring oscillator. The delay generated by adjusting the control voltage of the delay generator should appropriately be defined for the delay stages. There are some factors, such as supply and substrate voltages that affect the precision and linearity of the delay cell. The supply and substrate voltage give rise to the output jitter or phase-noise that will hamper the efficiency of the oscillator. Hence, the circuit should be less susceptible to the supply and substrate-induced noise. It can be done by using the coupled ring oscillator [5], which shows better phase noise for a particular oscillation frequency as compared to the traditional ring oscillator. The oscillation period (T_{osc}) of the conventional ring oscillator is defined as

$$T_{osc} = 2N \times \tau_P \tag{5}$$

where τ_P is the propagation delay of the delay cell and N is the number of stages of the ring oscillator. The minimum measurable time (T_{LSB}) of $\Sigma\Delta$ TDC can be expressed as [4]

$$T_{LSB} = \frac{T_{osc}}{2N} = \tau_P \tag{6}$$

From the above equation, it is clear that the T_{LSB} is limited to τ_P. Hence, the multipath technique is employed to reduce the effective propagation delay of the oscillator, which takes the inputs from not only previous output but also the past outputs [8, 4]. For the ring oscillator to operate correctly, the number of

inverters in the loop should be odd and preferably be prime. It is observed that the odd-prime number of delay cell in the loop gives better phase noise [8, 4].

Multipath ring oscillators are a selective type of ring oscillator used to increase the performance of the traditional ring oscillator. As already described that in multipath technique, the oscillator accepts input from the previous output as well as from the past outputs. In conventional ring oscillator, each stage of the delay cell changes its state only when the last stage has changed the state. However, in multipath delay cell oscillator, each stage tries to change its state well before the complete state changeover of the previous stages depending on the coupling. In order to verify this conjecture, we have proposed two designs, namely delay cell1 (DC1) and delay cell2 (DC2), as shown in Fig. 5. In DC1 architecture, the delay cell takes outputs from the just preceding stage Y_{i-1} as well as from the other previous stage outputs too, i.e., from Y_{i-3}, Y_{i-5}, Y_{i-7} and Y_{i-9} as shown in the Fig. 5(a). In a similar manner for DC2 topology, the delay cell accepts the outputs from Y_{i-1}, Y_{i-3}, Y_{i-5}, Y_{i-7}, Y_{i-9} and Y_{i-11} as illustrated in Fig. 5(b). Note that the larger widths are assigned to the MOSFETs which are relatively far from the current delay cell. In DC1 architecture, the MOSFET with Y_{i-1} input is just the previous stage, whereas Y_{i-9} is the farthest one. So, the MOSFET with Y_{i-1} input is assigned with a smaller width, whereas Y_{i-9} is assigned with a larger width for offering a low resistive path. The same strategy is followed for DC2 architecture too.

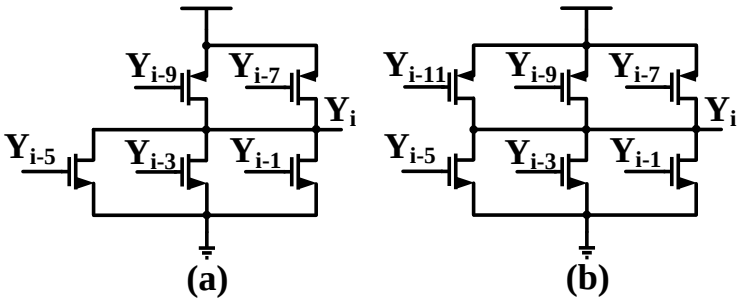

Fig. 5. Proposed delay cells (a) DC1, (b) DC2

The reduction in the delay of the multipath delay cell can be illustrated intuitively in Fig. 6. Suppose the multipath delay cell has M inputs. The effective propagation delay of the multipath delay cell is decided by the input, which is leading in phase. The $V_{in,M}$ input, which is leading in phase, provides the effective propagation delay of the ring oscillator. The multipath ring oscillator with M number of inputs is equivalent to the M number of coupled ring oscillators. In M number of coupled ring oscillators, the effective propagation delay $\tau_P{}'$ reduces by a factor of M, i.e.,

$$\tau_P{}' = \frac{\tau_P}{M} \tag{7}$$

In the proposed designs; DC1 topology, the coupling factor M = 5, whereas

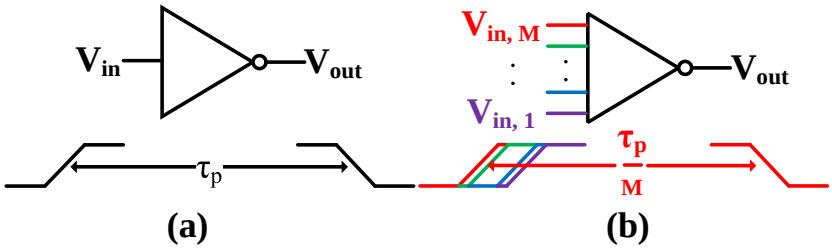

Fig. 6. Propagation delay: (a) Traditional Delay Cell, (b) Multipath Delay Cell

for the DC2 topology M = 6. The designer may be tempted to increase the coupling factor for achieving better resolution. In an N-stage ring oscillator, it is advised to choose the coupling inputs to a maximum of $\frac{N-1}{2}$ previous connections; otherwise, the oscillator will oscillate entirely out of the phase. This, in turn, increases the delay of the circuit [4]. For instance, in 47-stage multipath ring oscillator, the multipath connections that we can connect to the present delay cell would be $\frac{47-1}{2} = 23$ previous outputs connection only.

4 Results and Discussion

The proposed multipath delay cells for $\Sigma\Delta$ TDC are designed and simulated in UMC65, UMC40 and UMC28 CMOS processes using Cadence Virtuoso ADE. The proposed designs are utilised in the design of 47-stage ring oscillators. The performance summary of the multipath delay cell-based coupled oscillators for both DC1 and DC2 topologies in different technologies is compared in Table 2 where $T_{LSB_{MP}}$ is the T_{LSB} with multipath connections, T_{LSB_T} is the T_{LSB} in the conventional manner. For DC1 and DC2 designs, the resolution is improved as we move from UMC65 to UMC28. This demonstrates the advantages of CMOS technology scaling in resolution. The actual value of the coupling factor is nearly matching with the theoretical value and is given by

$$M = \frac{T_{LSB_T}}{T_{LSB_{MP}}} \tag{8}$$

The theoretical value of the coupling factor (M) for FET5 architecture is 5 and for FET6 architecture, it is 6.

The proposed designs are subjected to the number of stages of parametric simulations. From Fig. 7(a), it can be seen that as the number of delay cells (N) in the ring oscillator increases, the oscillation period increases. So, the frequency of oscillation decreases, which improves the phase noise around 1 MHz offset from the carrier. The proposed designs are subjected to the number of multipath

Table 2. Comparison of the proposed designs in UMC65, UMC40 and UMC28 CMOS technologies

Topology	**Technology**	$T_{LSB_{MP}}$ (ps)	T_{LSB_T} (ps)	**Phase noise** (dBc/Hz)	**Coupling factor** (M)
DC1	UMC65	2.40	11.86	81.04	4.94
	UMC40	1.83	9.02	79.5	4.93
	UMC28	0.98	5.27	73.88	5.38
DC2	UMC65	2.17	11.99	81.35	5.52
	UMC40	1.63	8.94	79.84	5.48
	UMC28	0.91	5.37	74.30	5.93

connections parametric simulation. From Fig. 7(b), as the number of multipath connections in the oscillator increases, the frequency of oscillation will increase, whereas the phase noise around 1 MHz offset from the carrier decreases.

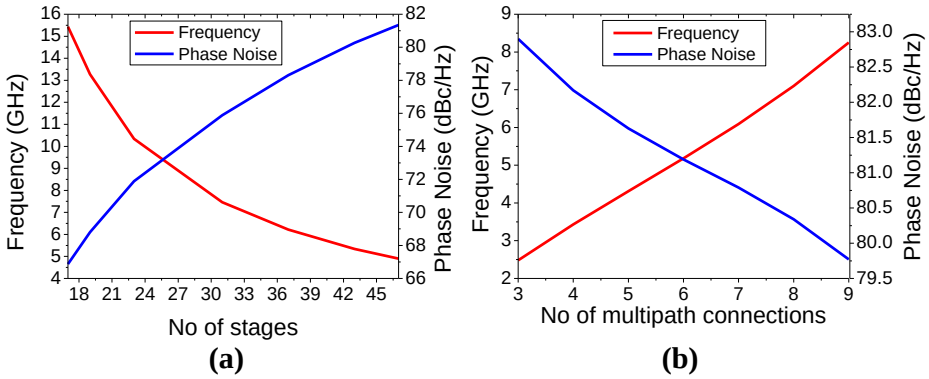

Fig. 7. Frequency and phase noise vs (a) the number of stages (b) the number of multipath connections

From the above extensive parametric simulations, we can draw the following conclusions. As the number of stages in the ring oscillator increases, the oscillation frequency comes down. Whereas the number of multipath connections increases, the oscillation frequency also increases. The phase-noise is inversely proportional to the operating frequency. The designer has to trade-off between the number of stages and the number of multipath connections, for achieving the desired operating frequency and phase-noise.

5 Conclusion

The coupled ring oscillators for $\Sigma\Delta$ TDCs have been demonstrated in this paper using the multipath techniques in UMC65, UMC40 and UMC28 CMOS process

technologies. The ring oscillator integrator (ROI) is projected as the basic building block for the time-domain signal processing, which scales well with the CMOS technology. The qualitative analysis on multipath technique for improving the resolution of $\Sigma\Delta$ TDC has been established. The effective propagation delay was reduced below τ_P by the factor of the number of multipath connections (M), without the requirement of array oscillators. The effective propagation delay for DC1 architecture has been reduced to $\frac{\tau_P}{5}$, whereas for DC2 architecture, it is $\frac{\tau_P}{6}$.

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