A Survey on Adiabatic Logic

* S.Nagaraj
Research Scholar
Department of ECE
JNTUA Anantapuramu,AP
Email:nagarajsubramanyam@gmail.com

† Dr. G.M.Sreerama Reddy
Principal
CBIT Kolar,KA
Email:gmsreeramareddy@gmail.com

‡ Dr. S.Aruna Mastani
Asistant Professor
Department of ECE
JNTUA Anantapuramu,AP
Email:aruna_mastani@yahoo.com

***Abstract*—As the VLSI Technology is growing the total number of transistor count on the chip is increasing but as the total number of transistors are increasing on the chip the power dissipation and heat dissipated is also increasing and the heat removal is becoming difficult and expensive. Hence to decrease or reduce the power dissipation adiabatic logic can be used since the energy is not dissipated. So designing CMOS logic with adiabatic logic reduces power consumption for low power VLSI applications. This paper presents a survey on two different logics. In this survey paper we have studied and analysed on adiabatic logic and (AAL) Asynchronous adiabatic logic.**

***Index Terms*—CMOS, Adiabatic Logic, CAL, PFAL, SCRL, PAL, 2PASCL, SCAL.**

I. INTRODUCTION

VLSI processing technology is developing and the number of transistor count or gates per chip area is increasing and the necessity for low power VLSI is increasing. Moreover we are using many portable devices in todays world. The battery power used in portable devices need to be used more efficiently. This papper focus mainly on reducting the power consumption by using several techniques. Adiabatic logic implementation was proved to be better in comparison with CMOS conventional logic. There has been many researches carried out on Adiabatic logics and better results are obtained. The disadvantage in CMOS logic is overcomed by Adiabatic technology by decreasing the power dissipation and the energy lost is recycled to power supply. The power also effects directly on the system cost.

II. ADIABATIC LOGIC

Adiabatic Logic Circits can be classified in to two types
1. Fully Adiabatic Circuits
2. Partially Adiabatic Circuits

Fully Adiabatic Circuits are very slow but dissipates less energy.
The following Logics comes under Fully Adiabatic Logic
1. PAL(Pass transistorAdiabatic Logic)
2. SCRL(Split level Charge Recovery Logic)
3. 2PASCL(Phase adiabatic static CMOS logic)

In Partially Adiabatic Circuits some part of energy is recovered so it has been named as Partially adiabatic.
The following Logics comes under Partially Adiabatic Logic
1. 2N2P/2N-2N2P
2. CAL(Clocked CMOS Adiabatic Logic)
3. TSEL(True Single Phase Adiabatic Logic)
4. SCAL(Source Coupled Adiabatic Logic)
5. Efficient charge recovery logic(ECRL)
6. Positive feedback adiabatic logic(PFAL)
7. NMOS energy recovery logic (NERL).

Takahashi, Yasuhiro, et al. [12] proposed (2PADCL) two phase drive adiabatic dynamic CMOS logic which uses twosinusoidal complementary power clock supply signals. The simulation results have shown 75% of less power consumption compared to static CMOS at 1MHz frequency.

Ye, Yibin, and K. Roy. [10] used two complementary sinusoidal supply clock signals in QSERL. Presented highly efficient circuit to generate required two complementary sinusoidal clock signals. An carry save multiplier is designed simulated using two phase clocks and sinusoidal QSERL logic. The simulation results have shown energy savings upto 37% over static CMOS multiplier at 100MHZ frequency.

Chang, Meng-Chou, and Chia-Chang Tsai. [97] HQAL (handshaking quasi adiabatic logic) that uses the adiabatic logic blocks and HCC(handshake control chain). The power supply to adiabatic logic in HQAL is supplied and controlled by the HCC. The results has shown 33.1% less power dissipation as compared to CMOS technology at 700MHZ frequency and 72.5% less power dissipation at 10MHZ frequency.

Lau, K. T., and F. Liu. [87] praposed 4 phased improved adiabatic adiabatic psuedo domino logic(IAPD-4ϕ). They have implemented 4-bit shift register using IAPDL and IAPDL-4ϕ the results has shown IAPDL-4ϕ has improvement in speed of operation , decrease in power dissipation by 65% at 200MHZ frequency as compared to IAPDL.

Arsalan, Muhammad, and Maitham Shams [77]AAL is proposed that reduces the problem of clock generator so this AAL does not need power clock generator (PCG) and are more power efficiency logic.

Adiabatic Dynamic Logic(ADL) designed by Dickson and

Denker (1994) [6] had shown reduction in power consumption compared with the CMOS conventional circuit design.

Adiabatic Pseudo Domino Logic(APDL) is obtained by combining adiabatic theory and CMOS domino logic which has been proposed by wang & Lau 1995 [8] this has recovered energy dissipation of over 80% in conventional static CMOS Logic design.

Quasi Adiabatic ternary logic was proposed by Mateo & Rubio (1996) that reduces expensive silicon area requiremnets. This logic has shown 65% of area savings for a half adder when compared with adiabatic binary logic.

CMOS positive feedback amplifier based on dual rail logic had been presented by vetuli et. al (1996) [17]to ensure high noise immunity and energy recovery process.

Fully Adiabatic MOS (AADMOS) and CAMOS (Complementary Adiabatic MOS) was proposed by De & Meindl (1996 a & b) that implements quasi adiabatic and quasi adiabatic reversible computing. The authors have presented static and dynamic energy recovery logic and have acheived significant energy savings compared with conventional static and dynamic CMOS.

The quasi static energy recovery logic (QSERL) using two complementary sinusoidal supply clocks had been proposed by Ye et. al (1997) and acheived 37% of energy over static CMOS multiplier at 100MHz.

APDL(Adiabatic Pseudo domino logic) had been proposed by Lau & Liu(1997) that gives high performance with simple clock supplies and reduces up to 75% of power disssipation.

RERL (Reversible Energy Recovery Logic) was proposed by Kwon & Chae (1998) and acheived considerable amount of energy savings.

ADCPL(Adiabatic Differential Cascode voltage switch with Complementary Pass Transistor Logic Tree) was proposed by Lo & Chan (1998) and obtained power reduction of 50% to 70% by recovering energy in recovery phase of supply clock in pipelined ADCPL carry look ahead adder.

Liu & Lau(1998a) has implemented 2x1 Multiplexer with pass transistor adiabatic logic with NMOS pull down configuration and acheived significant power savings.

Takahashi & Mizunuma (2000) proposed adiabatic dynamic CMOS logic (ADCL) circuit for super low power consumtion and acheived considerable amount of energy savings.

CP-BCRL (complement type pass transistor bootstrapped charge recovery logic) has been presented by Jiajun et. al (2001) and acheived less energy consumption, acheived efficient energy transfer and recovery.

ADCVSL(Adiabatic differntial cascode voltage swing logic) uses two phase non overlapping clock proposed by suvakovic & salama (2000) addressed the issues related to resonant circuits and design sequential adiabatic logic circuits preventing adiabatic system implementations from outperforming conventional CMSO designs in terms of energy efficiency.

EACRL(Efficient adiabatic charge recovery logic) was proposed by varga et. al (2001 a & b) eliminates non adiabatic loss during the charge phase.

IPGL(improved pass gate adiabatic charge recovery logic) was proposed by varga et. al that efficiently uses power consumption with moderate reversibility overhead for frequencies below 400 MHz.

CPERL(Complementary pass transistor energy recovery logic) was proposed by chang et. al(2002) implemented 10-stage CPERL inverter which consumed 48.8% of energy dissipation at 125 MHz.

IAPDL(Improved adiabatic pseudo domino logic) was proposed by widjaja & Lau(2003) with reduction of one diode and acheived considerable area savings and reduced power dissipation at lower supply voltages.

Dinesh Kumar novel adiabatic SRAM using split level charge recovery logic (SCRL). The proposed SRAM cell consumes 8.7 times less power as compared to the conventional 6T SRAM cell at 100MHz.

Reddy, N. S. S., et al. [22]has proposed adibatic circuits using single clock input to control charging and discharging of capacitive load instead of two complement clock signals. They have implemented basic gates and JK flip flop using the proposed method and has got energy savings upto 50% as compared with CMOS circuits.

III. Fully Adiabatic Circuits

A. PAL(Pass transistorAdiabatic Logic)

PAL means Pass transistor Adiabatic Logic has less gate complexity and uses dual rail it operates on two phase power clock. The figure 1 shows PAL gate. It consists of NMOS functional blocks and crocc coupled PMOS latch. There are two NMOS functional blocks that consists of true and complementary pass transistors. The sinusiodal power is supplied from the power source (PC). When the power source (PC) rises the conduction path is established through one of the conduction blocks to the corresponding output node and it follows the power clock. The other output node will be at tri-state and it is close to 0V by the load capacitance. In turn this will make one of the PMOS transistor to start conducting

and this charges the node that will go to one of the states and to the peak of power (PC). The output at the peak of the power clock(PC) is the valid output.The power clock will decrease slowly to zero and the energy stored in the output node capacitance is recovered.
PAL (Pass transistorAdiabatic Logic) has advantage in terms of saving energy and switching noise but it has disadvantage of low speed and uses high supply voltage.

Pass transistor adiabatic logic(PAL) with single power clock supply had been deisgned by oklobdzija et. al(1997) and acheived considerable amount of energy savings.

Arsalan, M., and M. Shams [89] implemented NAND gates using 2N-2P,2N-2N2P,PFAL,PAL,CAL,IPGL,CAL,PAL logics and compared the results. PAL logic has more advantageas compared to other adiabatic logic in terms of complexity of circuit and energy efficiency. PAL operates using only two clock phases and at lower frequency PAL does not function properly.
Jianping Hu This paper presents low-power complementary passtransistor adiabatic logic (CPAL) using two-phase powerclocks instead of four-phase ones. SPICE simulations show that the two-phase CPAL flip-flops consume less power than 2N-2N2P and CMOS implementation.

Jianping Hu paper presents low-power complementary passtransistor adiabatic logic (CPAL) using two-phase powerclocks instead of four-phase ones. SPICE simulations show that the two-phase CPAL flip-flops consume less power than 2N-2N2P and CMOS implementation.

Hu Jianping presented complementary pass-transistor adiabatic logic (CPAL) Simulation results with SPICE show that the CPAL inverter chain is 2.5 to 3 times more energy efficient than 2N-2N2P and 3 to 9 times less dissipative than the static CMOS for clock rates ranging from 25 to 300Mhz.

Lau, K. T., and F. Liu. [87] has proposed PAL-2N pass transistor adiabatic logic with NMOS pull down transistors they have designed and simulated 2x1 MUX using the proposed method and have shown energy savings up to 80% as compared with 2N-2N2P logic circuits.

Oklobdzija, V. G., et al. [14]presented a new PAL which operates using single clock power supply. PAL shift register has been designed and simulated the results has shown less energy consumption.

Adiabatic CPL (complementary pass transistor logic) is used Dai, Jing, et al. [92] with two phased power clocks consisting of only NMOS transistors. D flip flop and JK flip flop are implemented using adiabtic CPL has shown less no of transistors as compared to two phase CPAL, PAL-2N,2N-2N2P and CMOSTG logics.

Kumar, A.Kishore, and Robert Bosch [88] implemented multiplier using CMOS and CPTAAL(complemetary pass transistor asynchronous adiabatic logic) the results have shown energy savings in the range of 50% to 74% for clock frequency in the range of 100MHZ to 300MHZ as compared to conventional CMOS technology

Hu, Jianping, et al. [81]implemented power gating scheme in adiabatic logic for sequential circuits. Flip flops are designed using CPAL logic and results have shown power gating technology has gretaer reduction in energy loss of adiabatic sequential circuits.

CPAL(Complementary pass transistor adiabatic logic) was proposed by Jianping et. al(2003)r92 this has shown 2.5 to 3 times more efficient than 2N-2N2P and 3 to 9 times less than static CMOS for clock rates ranging from 25 to 300MHz.

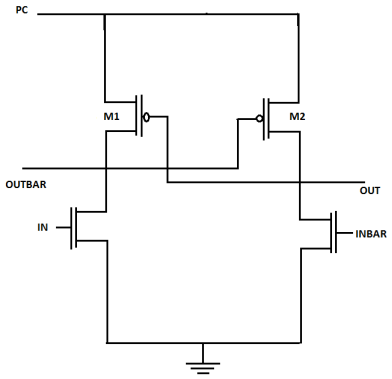

Fig. 1. PAL

B. SCRL(Split level Charge Recovery Logic)

In SCRL(Split level Charge Recovery Logic) the transfer of charge with in between the nodes wil takes palce quasi statically. The relation between operating frequency and energy dissipation changes due to this quasi statically operation. In conventional CMOS the operating frequency and the power consumption are linearly related whereas in this it is quadratically related that is power consumption decreases quadraticallly wit the frequency of operation.Reversible pipeline logic gate is used explicitly in this new family of circuit technique.The necessary information required to recover the energy is used to compute value is provided by the computing its logical inverse. whereas the enrgy required to uncompute the inverse is obtained from the subsequent inverse logic stage.

Dinesh Kumar novel adiabatic SRAM using split level charge recovery logic (SCRL). The proposed SRAM cell consumes 8.7 times less power as compared to the conventional 6T SRAM cell at 100MHz.

Kumar, S.Dinesh, and S. K.Noor Mahammad [86] implemented SRAM cell using SCRL and results has shown 8.7 times less power as compared to conventional 6T SRAM cell at frequency of 100MHZ.

C. 2PASCL(Phase adiabatic static CMOS logic)

The figure 2 shows inverter circuit in 2PASCL. It is two diode circuit, Diode D1 is placed between the output node and power supply ϕ and Diode D2 is placed next to NMOS transistor and connected to another power supply$\overline{\phi}$. These two MOSFET diodes serve the purpose of recycling charge from the output node. It also improves the speed of discharge. The 2PASCL uses two phase clocking that splits sinusoidal power supply where one clock is in phase and other is out of phase. The difference in between the voltage levels of ϕ and $\overline{\phi}$ is Vdd/2. The circuit operation has evaluation and hold phase. During the evaluation phase the power supply ϕ goes swing up and whereas the power supply $\overline{\phi}$ swings down. During the hold phase the power supply $\overline{\phi}$ swings up and whereas the power supply ϕ swings down.

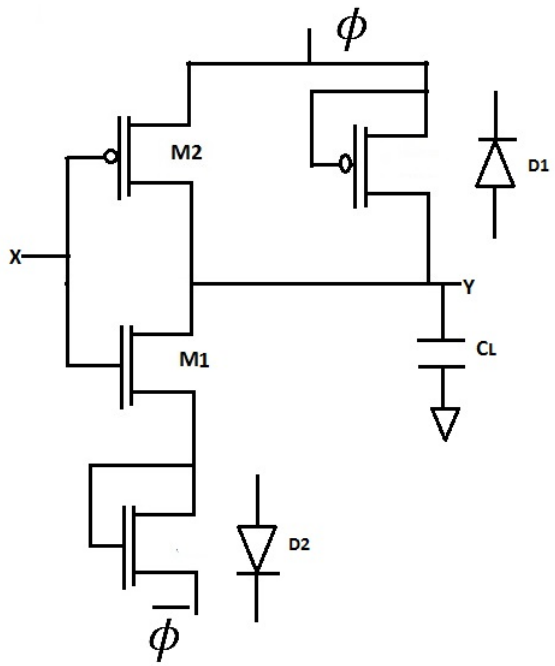

Fig. 2. 2PASCL

Anuar, Nazrul, et al. [86] proposed two-phase clocked adiabatic static CMOS logic (2PASCL) D flip flop and simulation results have shown 55.5% of less energy dissipation than static CMOS at frequency of 10-100 MHz.

Dinesh kumar 2018 designed full adder using (2PASCL) two phase clocked adiabatic static CMOS logic and the results has shown 92.66% decrease in power dissipation as compared with full adder using transmission gates.
Anuar, Nazrul, et al. [72] proposed two-phase clocked adiabatic static CMOS logic (2PASCL) 4-bit ripple-carry adder (RCA) and simulation results have shown 71.3% less energy dissipation than static CMOS at frequency of 10-100 MHz.

Nazrul Anuar proposed two-phase clocked adiabatic static CMOS logic (2PASCL) basic logic gates and simulation results have shown 97% less energy dissipation than static CMOS RCA at frequency of 10-100 MHz.

Nazrul Anuar proposed two-phase clocked adiabatic static CMOS logic (2PASCL) D flip flop and simulation results have shown 55.5% of less energy dissipation than static CMOS RCA at frequency of 10-100 MHz.

Nazrul Anuar proposed two-phase clocked adiabatic static CMOS logic (2PASCL) inverter chain and simulation results have shown 2PASCL 4 inverter chain gives energy savings upto 79% as compared to static CMOS logic at frequency of 1-100 MHz.

Nazrul Anuar proposed two-phase clocked adiabatic static CMOS logic (2PASCL) 4-bit ripple-carry adder (RCA) and simulation results have shown 71.3% less energy dissipation than static CMOS RCA at frequency of 10-100 MHz.

Nazrul Anuar 2009 proposed (2PASCL) two phase clocked adiabatic static CMOS logic using technique of energy recovery and adiabatic switching. They implemented by removing diode at charging path and achieved high amplitude of output and power consumed by diode is eliminated. The results have shown 97% of energy savings compared to static CMOS logic.

Takahashi, Yasuhiro, et al. [12]proposed new 2 phase driven adiabtic dynamic CMOS logic circuit(2PADCL) which uses two sinusoidal power supply which are complementary. The results has shown betterment in speed and power consumption and 97% eficient.

Maurya, Atul Kumar, and Gagnesh Kumar [18] proposed usage of two phase clocked adiabatic logic for energy recovery in adder circuit. They have designed and simulated full adder in CMOS,PFAL and 2PASCL the results has shown power savings upto 70% as compared with the propopsed design and CMOS logic at 10 to 200MHZ frequency range.

IV. Partially Adiabatic Circuits

A. 2N2P/2N-2N2P

The figure 3 below shows 2N-2P inverter gate. The circuit uses poer clock(PWR). It has two inputs IN,INBAR and two outputs OUT and OUTBAR. When the inputs are applied suppose that IN is high and INBAR is low and the power

clockis applied from 0 to VDD. SO the output OUT remains at low and OUTBAR follows the power clock. When the power clock reaches VDD th eoutput OUT and OUTBAR has the values of zero and VDD respectively. These outputs can be used as inputs for the next stage. When the power clock changes from VDD to zero then the output OUTPUTBAR returns its energy to power clock and hence the charge delivered is recovered. In ECRL the charge delivered by power clock is efficiently recovered using 4 phase clocking rule.

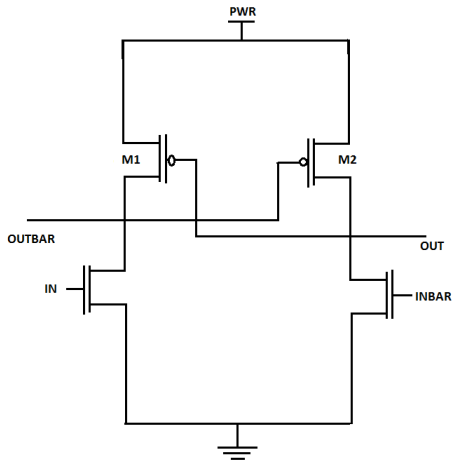

Fig. 3. 2N2P

The second order adiabatic computation with 2N-2P and 2N-2N2P logic was proposed by Kramer et. al(1995) to acheive adiabatic power savings without increaing size and complexity much.

Kramer, Alan, et al. [16]presented 2N-2P and 2N-2N2P adiabatic logic families the results have shown better energy savings compared to standard static CMOS.

Tamilselvan, G. M. [103]implemented (2N-2P) inverter and have achieved 57% of energy savings as compared with the conventional CMOS.

B. 2N-2N2P

The coupling effect is 2N-2P is reduced using this 2N-2N2P logic. This is derived from the 2N-2P logic family. The 2N-2N2P is made from latch which has two NMOS FETs and two PMOS FETs where as an 2N-2P consists of only two PMOS FETS and this is the majordifference between 2N-2P and 2N-2N2P logic. The addition of 2 extra NMOS FETs which arecross coupled gives non-floating outputs for a larger part of phase recovery.

Diode based complementary logic of adiabatic computing(2N-2N2D) using pairs of NMOS and diodes by Kramer et al(1994) [7] has shown considerable amount of energy savings.

He, Y., et al. [94] proposed 2N-2N2P2D adibatic logic the results has shown power savings about 40% as compared to 2N-2N2D logic and power savings up to 70% compared to the conventional CMOS logic.
Kramer, A., et al. [**?**]2N-2N2D is new adiabatic logic and the simulation results has shown power savings of three times approximately.

C. CAL(Clocked CMOS Adiabatic Logic)

CAL(Clocked CMOS Adiabatic Logic) is a Dual rail logic. CAL operates on AC power clock with single phase supply. CAL in adiabatic mode generates power clock using on chip switching transisitor and an inductor of small value connected externally between low voltage DC supply and the chip.

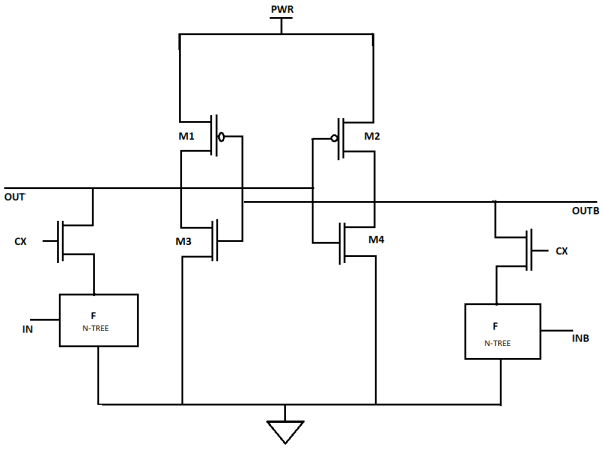

Fig. 4. CAL

The figure 4 shows an CAL inverter circuit. It consists of cross coupled CMOS inverters. CAL requires extra timing control clock signal CX in order to implement an adiabatic inverter or any other logical functions using a single power clock. The timing control signal controls the transistors that are in series with the logic trees representing the functional blocks F and FBAR. This control signal also enables the device operation with a single power clock power.

Clocked CMOS Adiabatic Logic(CAL) is low power with integrated single AC power supply had been designed by Maksimovic et. al (1997) [13]. It performs true and complementary logic functions to present constant capacitive load to power clock generator. The simulation results at 40MHz frequency has shown better energy savings compared to non-adiabatic system.

D. TSEL(True Single Phase Adiabatic Logic)

TSEL is partially adiabatic it is related to 2N2P and 2N-2N2P, CAL family of circuits. TSEL gates power is supplied

by a sinusoidal single phase power clock. TSEL consists of alternate PMOS and NMOS gates in cascade. It has two DC reference voltages this gives high efficiency and high speed operation. TSEL gates can be cascaded as in NP-Domino style. TSEL is more energy efficient across broad range of operating frequency. TSEL is dual rail which provides balanced load on clock generation. The figure 5 shows TSELP using PMOS.

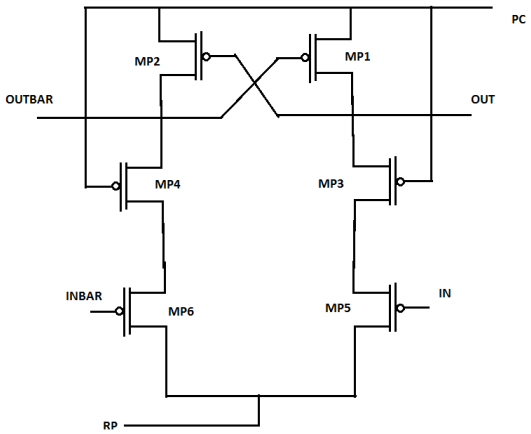

Fig. 5. TSEL

E. SCAL(Source Coupled Adiabatic Logic)

SCAL is partially adiabatic dynamic logic family.SCAL is energy efficient oner a wide range of frequencies of operation. It is acheived by using individual current sources which are tunable at each gate. All the TSEL's positive features are retained by SCAL. Tunable current sources are used to control rate of charge flow in to or out of each gate by which SCAL energy efficiency is increased. This adiabatic circuit avoids a no of problems that are associated complexity, clock skew, more energy dissipation and multiple power clocks. The figure6 below shows SCAL using PMOS.

SCAL(Single phaase source coupled adiabatic logic) family had been proposed by Kim & Papaefthymiou(1999) [40] and designed an energy efficient SCAL adder.

F. Efficient charge recovery logic(ECRL)

Efficient charge recovery logic(ECRL) was proposed by Moon & Jeong (1996). It is techinque for low energy adiabatic logic circuit and had acheived four to six times power reduction with practical loading.

In this logic two PMOS transistors are cross coupled along with N-functional blocks consisting of NMOS transistors. ECRL gates uses AC power supply for reuse and recover supplied energy. There are two outputs OUT and OUTB so that constant load capacitance independent of input signal can be driven. Two cross coupled PMOS transistors produces

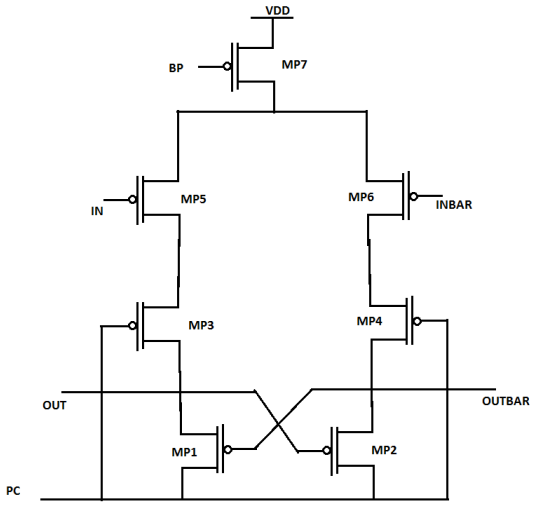

Fig. 6. SCAL

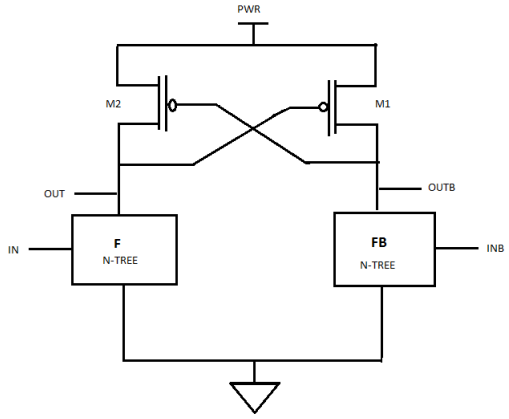

Fig. 7. ECRL

full output voltage swing in precharge and recovery phases. But the threshold voltage of PMOS transisitors gives rise to non-adiabatic loss both in recovery and precharge phases. Thus ECRL always boost the charge for full swing of output. But when the supply clock voltage is near to threshold voltage Vtp the PMOS transistor will be switched off. Thus the path is disconnected and as a result the recovery is incomplete. The figure7 below shows ECRL circuit.

Liu & Lau(1998b) [33] proposed an improved structure for efficient charge recovery logic (IECRL) and acheived significant power performance than ECRL coupled with an improved output.

Hooda, Jyoti, and Shweta Chawla [90] implemented 4x1 MUX using ECRL the results have shown less power dissipation compared to CMOS conventional logic.

Marina, S.Amalin, et al. [104]Implemented Full Adder

on different adiabatic logic styles and compared the power at different frequencies. The results have shown that ECRL (Efficient charge recovery logic) consumes less power about 69% less than CMOS logic at low frequency whereas SQAL (Secured quasi adiabatic logic) power is 71.8% large power than CMOS logic at higher frequency.

G. Positive feedback adiabatic logic(PFAL)

Positive feedback adiabatic logic(PFAL) is partial energy recovery logic. PFAL energy consumption is low as compared with other related similar families. If the technological parameters vary then PFAL can adjust or adapt to the changes. PFAL recoveres energy partially with dual rail circuit. The figure 8 shows a PFAL circuit.

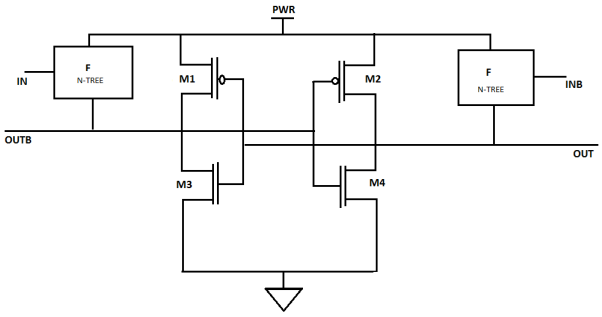

Fig. 8. PFAL

The heart of PFAL circuit is adiabatic amplifier and latch made by two PMOS transistors M1-M2 and two NMOS transistors M3-M4 which avoids degradation of logic levels on the output nodes OUT and OUTB. The logic function is realized by the two n-trees. The functional blocks are in parallel with the PMOSFETS in adiabatic amplifier and forms a transmission gate. The outputs generated by this logic family is both positive and negative. In ECRL the latch is made up of two PMOSFETS whereas in PFAL it is made up of two PMOSFETS and two NMOSFETS.

I-PFAL(Improved PFAL) proposed by fischer et. al(2004) [30] obtained significant reduction of energy dissipation, where all n- and p-channel devices are swapped so that the charge can be recovered through an n-channel MOSFET lower the power consumption and achieve better performance.

Bhaaskaran, V. S.Kanchana [98] 8-bit APFAL(Assymetrical PFAL) multiplier at 500MHZ frequency and obtained 22.5% of energy savings compared to PFAL 8-bit PFAL multiplier.

Chaudhuri, Arpan, et al. [99]designed 4x1 MUX using CMOS,2N-2N2P, ECRL and PFAL logics at high frequencies and PFAL has shown better results as compared to other logics.

Kushawaha, Shiv Pratap Singh, and Trailokya Nath Sasamal [101] ued modified PFAL (MPFAL) and implemented basic logic gates and results has shown that there is reduction in average power in MPFAL as compared to PFAL at 10 to 500 MHZ range of frequency.

Singh, Shashank, and Trailokya Nath Sasamal [102] designed and implemented 2x2 vedic multiplier using CMOS,ECRL and PFAL and their power consumption are compared PFAL has shown 64% less power consumption compared to CMOS and PFAL is more efficient than CMOS and ECRL.

Vetuli, A., et al. [17]proposed logic that uses CMOS positive feedback amplifier the use of positive feedback amplifier gives better noise immunity and it takes part in the process of energy recovery.

Rakesh Kumar Yadav [31] praposed two logic families, ECRL (Efficient Charge Recovery Logic) and PFAL (Positive Feedback Adiabatic Logic) are compared with conventional CMOS logic for inverter and 2:1 multiplexer circuits. PFAL shows better energy shavings than ECRL at the high frequency and high load capacitance.

H. NMOS energy recovery logic (NERL)

NERL uses NMOS transistors ,six-phase clocked power.NERL area, energy consumption are less as compared with fully adiabatic logic system.NMOS bootstrapped switches simplifies NERL circuits. NERL is most suitable adiabatic logic for the applications where high performance is not required but low energy is to be consumed.

V. Asynchronous Adiabatic Logic

Asynchronous Low power logic design praposed by Willingham and Kale(2004) [3] uses the benefits of low power to drive data path of quasi adiabatic elements and achieved more efficient data path widths.There was 63% reduction in energy losses by using reversable, positive feedback adiabatic logic circuit by these authors implementation on universal Toffoli gates.

Asynchronous adiabatic logic was proposed by Arsalan & Shams(2007) [77] that had overcomed problems related to synchronous clock routing and generation of clock in adiabatic systems which used advantages of adiabatic logic circuits with asynchronous logic systems.

VI. conclusion

The study on various Adiabatic logic circuits has shown a way to reduce decrease the energy dissipation as compared to conventional switching logic under certain circumstances. The input signals undergo transition in the form of ramp in adiabatic circuits.Whereas in the conventional CMOS logic

the inputs have only changes in final logic state. The logic switching should not be instantaneous it should be changed gradually for reducing power dissipation. The rise time and fall times cannot be increased by the various circuits we have discussed in this paper but the power dissioation can be decreased to lower level.We have seen that fully adiabatic circuits have very complex design but power consumption is reduced significantly. Partially adiabatic circuits have less complexity in design and cannot reduce power consumption as effieciently as fully adiabatic circuits. Asynchronous adiabatic logic overcomes problem of clock generation and synchronous routing it combines the benefits of adiabatic logic and asynchronous logic.

REFERENCES

[1] Willingham, DJ & Kale, I 2004, Asynchronous, quasi- adiabatic (asynchrobatic) logic for low power very wide data width applications, Proceedings of International Symposium on Circuits and Systems, vol. 2, pp. 257-260.

[2] Willingham, DJ & Kale, I 2008a, An asynchrobatic, radix-four, carry look-ahead adder, Proceedings of PhD Research in Microelectronics and Electronics, pp. 105-108.

[3] Willingham, DJ & Kale, I 2008b, A system for calculating the greatest common denominator implemented using asynchrobatic logic, Proceedings of Norchip, pp. 194-197.

[4] Willingham, DJ & Kale, I 2008c, Using positive feedback adiabatic Logic to implement Reversible Toffoli Gates, Proceedings of Norchip,pp. 5-8.

[5] Willingham, DJ & Kale, I 2011, A Ternary adiabatic logic (TAL) implementation of a four-trit full-adder, Proceedings of Norchip, pp.1-4.

[6] Dickinson, AG & Denker, JS 1994, "Adiabatic dynamic logic, IEEE Journal of Solid State Circuits, vol. 30, no. 3, pp. 311-315.

[7] Kramer, A, Denker, JS, Avery, SC, Dickinson AG & Wik, TR 1994, Adiabatic computing with the 2n-2n2p logic family, Symposium on VLSI Circuits-Digest of Technical Papers, pp. 25-26.

[8] J.M.Rabaey,"Digital Integrated Circuits", Prentice Hall, Engelwood Cliffs,NJ,1996.

[9] Anuar, Nazrul, et al. Adiabatic Logic versus CMOS for Low Power Applications. ITC-CSCC:International Technical Conference on Circuits Systems, Computers and Communications, 2009, pp. 302305.

[10] Ye, Yibin, and K. Roy. QSERL: Quasi-Static Energy Recovery Logic. IEEE Journal of Solid-State Circuits, vol. 36, no. 2, 2001, pp. 239248.

[11] Pan, W. D., and M. Nalasani. Reversible Logic. IEEE Potentials, 2005.

[12] Takahashi, Yasuhiro, et al. 2PADCL: Two Phase Drive Adiabatic Dynamic CMOS Logic. APCCAS 2006 - 2006 IEEE Asia Pacific Conference on Circuits and Systems, 2006, pp. 14841487.

[13] Maksimovic, D., et al. Clocked CMOS Adiabatic Logic with Integrated Single-Phase Power-Clock Supply. IEEE Transactions on Very Large Scale Integration Systems, vol. 8, no. 4, 2000, pp. 460463.

[14] Oklobdzija, V. G., et al. Pass-Transistor Adiabatic Logic Using Single Power-Clock Supply. IEEE Transactions on Circuits and Systems Ii: Analog and Digital Signal Processing, vol. 44, no. 10, 1997, pp. 842846.

[15] Anuar, Nazrul, et al. Two Phase Clocked Adiabatic Static CMOS Logic and Its Logic Family. Journal of Semiconductor Technology and Science, vol. 10, no. 1, 2010, pp. 110.

[16] Kramer, Alan, et al. 2nd Order Adiabatic Computation with 2N-2P and 2N-2N2P Logic Circuits. Proceedings of the 1995 International Symposium on Low Power Design, 1995, pp. 191196.

[17] Vetuli, A., et al. Positive Feedback in Adiabatic Logic. Electronics Letters, vol. 32, no. 20, 1996, pp. 18671869.

[18] Maurya, Atul Kumar, and Gagnesh Kumar. Energy Efficient Adiabatic Logic for Low Power VLSI Applications. 2011 International Conference on Communication Systems and Network Technologies, 2011, pp. 460463.

[19] Takahashi, Yasuhiro, et al. 2PADCL: Two Phase Drive Adiabatic Dynamic CMOS Logic. APCCAS 2006 - 2006 IEEE Asia Pacific Conference on Circuits and Systems, 2006, pp. 14841487.

[20] Anuar, Nazrul, et al. Two Phase Clocked Adiabatic Static CMOS Logic. 2009 International Symposium on System-on-Chip, 2009, pp. 8386.

[21] Arsalan, Muhammad, and Maitham Shams. Charge-Recovery Power Clock Generators for Adiabatic Logic Circuits. 18th International Conference on VLSI Design Held Jointly with 4th International Conference on Embedded Systems Design, 2005, pp. 171174.

[22] Reddy, N. S. S., et al. Cascadable Adiabatic Logic Circuits for Low-Power Applications. Iet Circuits Devices & Systems, vol. 2, no. 6, 2008, pp. 518526.

[23] Liu, F., and K. T. Lau. Pass-Transistor Adiabatic Logic with NMOS Pull-down Configuration. Electronics Letters, vol. 34, no. 8, 1998, pp. 739741.

[24] Takahashi, Kazukiyo, and Mitsuru Mizunuma. Adiabatic Dynamic CMOS Logic Circuit. Electronics and Communications in Japan Part Ii-Electronics, vol. 83, no. 5, 2000, pp. 5058.

[25] Dickinson, A. G., and J. S. Denker. Adiabatic Dynamic Logic. Proceedings of IEEE Custom Integrated Circuits Conference - CICC 94, vol. 30, no. 3, 1994, pp. 282285.

[26] Inoue, K., et al. Simulation and Experimental Demonstration of Logic Circuits Using an Ultra-Low-Power Adiabatic Quantum-Flux-Parametron. IEEE Transactions on Applied Superconductivity, vol. 23, no. 3, 2013, pp. 13011051301105.

[27] Tulasi, G.Ram., et al. Design & Analysis of Full Adders Using Adiabatic Logic. International Journal of Engineering Research and Technology, 2012.

[28] Choi, Byong-Deok, et al. Symmetric Adiabatic Logic Circuits against Differential Power Analysis. Etri Journal, vol. 32, no. 1, 2010, pp. 166168.

[29] Avital, Moshe, et al. DPA-Secured Quasi-Adiabatic Logic (SQAL) for Low-Power Passive RFID Tags Employing S-Boxes. IEEE Transactions on Circuits and Systems, vol. 62, no. 1, 2015, pp. 149156.

[30] Fischer, J., et al. Improving the Positive Feedback Adiabatic Logic Family. Advances in Radio Science, vol. 2, no. 8, 2005, pp. 221225.

[31] Yadav, Rakesh Kumar, et al. Adiabatic Technique for Energy Efficient Logic Circuits Design. 2011 International Conference on Emerging Trends in Electrical and Computer Technology, 2011, pp. 776780.

[32] Morrison, Matthew, and Nagarajan Ranganathan. Synthesis of Dual-Rail Adiabatic Logic for Low Power Security Applications. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 33, no. 7, 2014, pp. 975988.

[33] Lau, K. T., and F. Liu. Improved Adiabatic Pseudo-Domino Logic Family. Electronics Letters, vol. 33, no. 25, 1997, pp. 21132114.

[34] Amirante, Ettore, et al. Variations of the Power Dissipation in Adiabatic Logic Gates. 2001.

[35] Chanda, Manash, et al. Implementation of Subthreshold Adiabatic Logic for Ultralow-Power Application. IEEE Transactions on Very Large Scale Integration Systems, vol. 23, no. 12, 2015, pp. 27822790.

[36] Bhaaskaran, V. S.Kanchana, and J. P. Raina. Differential Cascode Adiabatic Logic Structure for Low Power. Journal of Low Power Electronics, vol. 4, no. 2, 2008, pp. 178190.

[37] Priya, Anu, and Amrita Rai. Adiabatic Technique for Power Efficient Logic Circuit Design. 2014.

[38] Takeuchi, Naoki, et al. Novel Latch for Adiabatic Quantum-Flux-Parametron Logic. Journal of Applied Physics, vol. 115, no. 10, 2014, p. 103910.

[39] Takahashi, Yasuhiro, et al. VLSI Implementation of a 4 x 4-Bit Multiplier in a Two Phase Drive Adiabatic Dynamic CMOS Logic. IEICE Transactions on Electronics, vol. 90, no. 10, 2007, pp. 20022006.

[40] Kim, Suhwan, and Marios C. Papaefthymiou. Single-Phase Source-Coupled Adiabatic Logic. Proceedings. 1999 International Symposium on Low Power Electronics and Design (Cat. No.99TH8477), 1999, pp. 9799.

[41] Takeuchi, N., et al. Reversible Logic Gate Using Adiabatic Superconducting Devices. Scientific Reports, vol. 4, no. 1, 2015, pp. 63546354.

[42] Li, He, et al. Clocked CMOS Adiabatic Logic with Low-Power Dissipation. SoC Design Conference (ISOCC), 2013 International, 2013, pp. 6467.

[43] Hu, Jianping, et al. Low-Power Adiabatic Sequential Circuits with Complementary Pass-Transistor Logic. 48th Midwest Symposium on Circuits and Systems, 2005., 2005, pp. 13981401.

[44] Zhang, Y., et al. 0.8 V CMOS Adiabatic Differential Switch Logic Circuit Using Bootstrap Technique for Low-Voltage Low-Power VLSI. Electronics Letters, vol. 38, no. 24, 2002, pp. 14971499.

[45] Xu, Q., et al. Design of an Extremely Energy-Efficient Hardware Algorithm Using Adiabatic Superconductor Logic. 2015 15th International

Superconductive Electronics Conference (ISEC), vol. 2015, no. 2, 2015, pp. 13.

[46] Tiwari, Mukesh, et al. Adiabatic Improved Efficient Charge Recovery Logic for Low Power CMOS Logic. IJEIR, vol. 1, no. 4, 2012, pp. 350354.

[47] Takahashi, Yasuhiro, et al. Two-Phase Clocked CMOS Adiabatic Logic. 2009.

[48] Liao, Nan, et al. Low Power Adiabatic Logic Based on FinFETs. Science in China Series F: Information Sciences, vol. 57, no. 2, 2014, pp. 113.

[49] Chanda, M., et al. Design of Sequential Circuits Using Single-Clocked Energy Efficient Adiabatic Logic for Ultra Low Power Application. 2014 18th International Symposium on VLSI Design and Test (VDAT), 2014, pp. 12.

[50] Marjonen, Jouko, and Markku berg. A Single Clocked Adiabatic Static Logic–A Proposal for Digital Low Power Applications. Signal Processing Systems, vol. 27, no. 3, 2001, pp. 253268.

[51] Teichmann, Philip. Adiabatic Logic: Future Trend and System Level Perspective. 2011.

[52] Houri, Samer, et al. Comparing CMOS-Based and NEMS-Based Adiabatic Logic Circuits. RC13 Proceedings of the 5th International Conference on Reversible Computation, 2013, pp. 3645.

[53] Bhaaskaran, V. S.Kanchana, and J. P. Raina. TWO-PHASE SINUSOIDAL POWER-CLOCKED QUASI-ADIABATIC LOGIC CIRCUITS. Journal of Circuits, Systems, and Computers, vol. 19, no. 2, 2010, pp. 335347.

[54] Takeuchi, Naoki, et al. Energy Efficiency of Adiabatic Superconductor Logic. Superconductor Science and Technology, vol. 28, no. 1, 2015, p. 15003

[55] Kato, Kazunari, et al. Two Phase Clocking Subthreshold Adiabatic Logic. Circuits and Systems (ISCAS), 2014 IEEE International Symposium On, 2014, pp. 598601.

[56] Kumar, S.Dinesh, et al. Design Exploration of a Symmetric Pass Gate Adiabatic Logic for Energy-Efficient and Secure Hardware. Integration, vol. 58, 2017, pp. 369377.

[57] Teichmann, Philip, et al. Power-Clock Gating in Adiabatic Logic Circuits. Power and Timing Modeling Optimization and Simulation, 2005, pp. 638646.

[58] Lo, Chun-Keung, and Philip C. H. Chan. An Adiabatic Differential Logic for Low-Power Digital Systems. IEEE Transactions on Circuits and Systems Ii: Analog and Digital Signal Processing, vol. 46, no. 9, 1999, pp. 12451250.

[59] Lim, Joonho, et al. Reversible Energy Recovery Logic Circuit without Non-Adiabatic Energy Loss. Electronics Letters, vol. 34, no. 4, 1998, pp. 344346.

[60] Willingham, David J., and Izzet Kale. A Ternary Adiabatic Logic (TAL) Implementation of a Four-Trit Full-Adder. 2011 NORCHIP, 2011, pp. 14.

[61] Saxena, Praveer, et al. MODIFIED TWO PHASE DRIVE ADIABATIC DYNAMIC CMOS LOGIC. 2012.

[62] Wang, W. Y., and K. T. Lau. Adiabatic Pseudo-Domino Logic. Electronics Letters, vol. 31, no. 23, 1995, pp. 19821983.

[63] Khatir, Mehrdad, et al. Improving the Energy Efficiency of Reversible Logic Circuits by the Combined Use of Adiabatic Styles. Integration, vol. 44, no. 1, 2011, pp. 1221.

[64] Bhati, Preeti, and Navaid Z. Rizvi. Adiabatic Logic: An Alternative Approach to Low Power Application Circuits. 2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT), 2016, pp. 42554260.

[65] Upadhyay, Shipra, et al. DFAL: Diode-Free Adiabatic Logic Circuits. International Scholarly Research Notices, vol. 2013, 2013, pp. 112.

[66] Staroselskii, V. I. Adiabatic Logic Circuits: A Review. Russian Microelectronics, 2001.

[67] Hu, Jianping, et al. Low Power Dual Transmission Gate Adiabatic Logic Circuits and Design of SRAM. The 2004 47th Midwest Symposium on Circuits and Systems, 2004. MWSCAS 04., vol. 1, 2004.

[68] Sajid, Abdul, et al. Design and Implementation of Low Power 8-Bit Carry-Look Ahead Adder Using Static CMOS Logic and Adiabatic Logic. International Journal of Information Technology and Computer Science, vol. 5, no. 11, 2013, pp. 7892.

[69] Anuar, Nazrul, et al. 44-Bit Array Two Phase Clocked Adiabatic Static CMOS Logic Multiplier with New XOR. 2010 18th IEEE/IFIP International Conference on VLSI and System-on-Chip, 2010, pp. 364368.

[70] Nayan, Nazrul Anuar, et al. LSI Implementation of a Low-Power 4 4-Bit Array Two-Phase Clocked Adiabatic Static CMOS Logic Multiplier. Microelectronics Journal, vol. 43, no. 4, 2012, pp. 244249.

[71] Teichmann, Philip. Fundamentals of Adiabatic Logic. 2012, pp. 522.

[72] Anuar, Nazrul, et al. 4-Bit Ripple Carry Adder of Two-Phase Clocked Adiabatic Static CMOS Logic: A Comparison with Static CMOS. 2009 European Conference on Circuit Theory and Design, 2009, pp. 6568.

[73] Singh, Richa, et al. Power Efficient Design of Multiplexer Based Compressor Using Adiabatic Logic. International Journal of Computer Applications, vol. 81, no. 10, 2013, pp. 4550.

[74] Samanta, Samik. Power Efficient VLSI Inverter Design Using Adiabatic Logic and Estimation of Power Dissipation Using VLSI-EDA Tool. 2010.

[75] Willingham, David J., and Izzet Kale. Using Positive Feedback Adiabatic Logic to Implement Reversible Toffoli Gates. 2008 NORCHIP, 2008, pp. 58.

[76] Pillonnet, Gal, et al. Adiabatic Capacitive Logic: A Paradigm for Low-Power Logic. 2017 IEEE International Symposium on Circuits and Systems (ISCAS), 2017, pp. 14.

[77] Arsalan, Muhammad, and Maitham Shams. Asynchronous Adiabatic Logic. 2007 IEEE International Symposium on Circuits and Systems, 2007, pp. 37203723.

[78] Sanadhya, Minakshi, and M.Vinot. Kumar. Recent Development in Efficient Adiabatic Logic Circuits and Power Analysis with CMOS Logic. Procedia Computer Science, vol. 57, 2015, pp. 12991307.

[79] Shukla, Amit, et al. Design of Low Power VLSI Circuits Using Energy Efficient Adiabatic Logic. 2013.

[80] Sharma, Manoj, and Arti Noor. Positive Feed Back Adiabatic Logic: PFAL Single Edge Triggered Semi-Adiabatic D Flip Flop. 2013.

[81] Hu, Jianping, et al. Power-Gating Adiabatic Flip-Flops and Sequential Logic Circuits. 2007 International Conference on Communications, Circuits and Systems, 2007, pp. 10161020.

[82] Chanda, M., et al. Ultra Low-Power Sequential Circuit Implementation by a Quasi-Static Single Phase Adiabatic Dynamic Logic (SPADL). TENCON 2009 - 2009 IEEE Region 10 Conference, 2009, pp. 15.

[83] Bargagli-Stoffi, A., et al. Four-Phase Power Clock Generator for Adiabatic Logic Circuits. Electronics Letters, vol. 38, no. 14, 2002, pp. 689690.

[84] Mahmoodi-Meimand, Hamid, and Ali Afzali-Kusha. Efficient Power Clock Generation for Adiabatic Logic. ISCAS 2001. The 2001 IEEE International Symposium on Circuits and Systems (Cat. No.01CH37196), vol. 4, 2001, pp. 642645.

[85] Monteiro, Cncio, et al. DPA Resistance of Charge-Sharing Symmetric Adiabatic Logic. 2013 IEEE International Symposium on Circuits and Systems (ISCAS2013), 2013, pp. 25812584.

[86] Kumar, S.Dinesh, and S. K.Noor Mahammad. A Novel Adiabatic SRAM Cell Implementation Using Split Level Charge Recovery Logic. 2015 19th International Symposium on VLSI Design and Test, 2015, pp. 12.

[87] Lau, K. T., and F. Liu. Four-Phase Improved Adiabatic Pseudo-Domino Logic. Electronics Letters, vol. 34, no. 4, 1998, pp. 343344.

[88] Kumar, A.Kishore, and Robert Bosch. Low Power Multiplier Design Using Complementary Pass-Transistor Asynchronous Adiabatic Logic. 2010.

[89] Arsalan, M., and M. Shams. An Investigation into Transistor-Based Adiabatic Logic Styles. The 2nd Annual IEEE Northeast Workshop on Circuits and Systems, 2004. NEWCAS 2004., 2004, pp. 14.

[90] Hooda, Jyoti, and Shweta Chawla. Design and Implementation of Low Power 4:1 Multiplexer Using Adiabatic Logic. 2013.

[91] Jianping, Hu, et al. A New Type of Low-Power Adiabatic Circuit with Complementary Pass-Transistor Logic. 2003 5th International Conference on ASIC Proceedings (IEEE Cat No 03TH8690) ICASIC-03, 2003, pp. 12351238.

[92] Dai, Jing, et al. Adiabatic CPL Circuits for Sequential Logic Systems. 2006 49th IEEE International Midwest Symposium on Circuits and Systems, vol. 1, 2006, pp. 713717.

[93] Anuar, Nazrul, et al. Fundamental Logics Based on Two Phase Clocked Adiabatic Static CMOS Logic. 2009 16th IEEE International Conference on Electronics, Circuits and Systems - (ICECS 2009), 2009, pp. 503506.

[94] He, Y., et al. Quasi-Static Adiabatic Logic 2N-2N2P2D Family. Electronics Letters, vol. 42, no. 16, 2006, pp. 905906.

[95] Sharma, Monika. Design and Analysis of CMOS Cells Using Adiabatic Logic. 2012.

[96] Loo, Edward K., et al. Low-Voltage Single-Phase Clocked Quasi-Adiabatic Pass-Gate Logic. 2007 Canadian Conference on Electrical and Computer Engineering, 2007, pp. 16451648.
[97] Chang, Meng-Chou, and Chia-Chang Tsai. Handshaking Quasi-Adiabatic Logic. 2009 52nd IEEE International Midwest Symposium on Circuits and Systems, 2009, pp. 531534
[98] Bhaaskaran, V. S.Kanchana. Asymmetrical Positive Feedback Adiabatic Logic for Low Power and Higher Frequency. 2010 International Conference on Advances in Recent Technologies in Communication and Computing, 2010, pp. 59.
[99] Chaudhuri, Arpan, et al. Implementation of Circuit in Different Adiabatic Logic. 2015 2nd International Conference on Electronics and Communication Systems (ICECS), 2015, pp. 353359.
[100] Tomita, Yuuki, et al. Adiabatic Array Logic. ICSES 2010 International Conference on Signals and Electronic Circuits, 2010, pp. 269272.
[101] Kushawaha, Shiv Pratap Singh, and Trailokya Nath Sasamal. Modified Positive Feedback Adiabatic Logic for Ultra Low Power VLSI. 2015 International Conference on Computer, Communication and Control (IC4), 2015, pp. 15.
[102] Singh, Shashank, and Trailokya Nath Sasamal. Design of Vedic Multiplier Using Adiabatic Logic. 2015 International Conference on Futuristic Trends on Computational Analysis and Knowledge Management (ABLAZE), 2015, pp. 438441.
[103] Tamilselvan, G. M. Design and Analysis of Low Power Multipliers and 4:2 Compressor Using Adiabatic Logic. 2013.
[104] Marina, S.Amalin, et al. Analysis of Full Adder Using Adiabatic Charge Recovery Logic. 2016 International Conference on Circuit, Power and Computing Technologies (ICCPCT), 2016, pp. 16.