Two Dimensional Analytical Expression of Threshold Voltage for Un-Doped Double Gate MOSFET

[1]Narendra K. Garg, [2]Somashekhar Malipatil, [3]Vikas Maheshwari, [4]Rajib Kar

[1]Dept. of ECE, Amity School of Engineering & Technology, Amity University Madhya-Pradesh, Gwalior, India

[2]Dept. of ECE, AVN Institute of Engineering & Technology, Hyderabad, Telangana State, India

[3]Dept. of ECE, Bharat Institute of Engineering & Technology, Ibrahimpatnam, Hyderabad, Telangana State, India

[4]Dept. of ECE, National Institute of Technology Durgapur, West-Bengal, India

[1]narendra.gwl.mits@gmail.com, [2]somashekhar49@gmail.com, [3]maheshwarivikas1982@gmail.com, [4]rajibkarece@gmail.com

Abstract *–In this work, new two-dimensional (2-D) analytical solution of Threshold Voltage (V_{th}) for un-doped (or lightly doped) Double Gate MOSFETs is proposed. In this research work Green's function based techniques are applied to solve the Poisson equations in 2-dimensional and we derived the threshold voltage (V_{th}) expression by using the concept of surface potential. This model is assumed uniform doping profile in Si region. The proposed model is compared with existing literature and experimental results and we got better solutions with previous techniques.*

Index Terms - *Green's function, Minimum surface potential, Threshold Voltage, Symmetric DG-MOSFET, Two dimensional (2D) Poisson equations and Un-doped or lightly doped.*

I. INTRODUCTION

In last two decade, VLSI (very large-scale integration) Technology CMOS has been used as a fundamental building block for low power system designs. Double-Gate (DG) MOSFET is emerging as a latest research domain in VLSI because the scaling of these devices is possible to the minimum channel length L possible for provided process technology parameters [1]. The scaling of MOSFET at deep submicron level has shown new and serious challenges for the designing and fabrication of future integrated circuits. When the MOSFET dimensions are scaled down, both the supply voltage and the gate-oxide thickness must also be scaled down. The short channel effects [2] are controlled by scaling down both the gate-oxide thickness and channel length. The scaling of gate-oxide thickness is limited to about 1 nm because of high gate tunneling current [3-4]. Scaling down the device dimension in nanometer regime, leakage currents plays an important role which needs more attention from the designer. Scalability of DG-MOSFETs is limited by sub-threshold swing which is an important design parameter. Formation of two channels in the symmetric DG MOSFET [5] provides steep sub-threshold swing, high drive current and trans-conductance. The sub-threshold swing and other short channel effects can be optimized by using appropriate gate dielectric [6]. Therefore new MOSFET structures such as Dual Gate and Tri-Gate MOS transistors [7] are proposed to replace conventional planer MOSFET. It is also important that these new structure of MOSFETs are compatible with latest designing and fabrication techniques [8] of silicon integrated circuits. Dual gate MOSFETs also referred as inversion charge transistors have many advantages over conventional MOSFETs. First, there is considerable reduction in the device area. Second, DG MOSFET's miller capacitance and output conductance can be further considerably reduced that makes it useful device for the designing of analog integrated circuits. Third, the breakdown voltage of the device can be made very high by using proper design methodology. Fourth, short channel effects in scaled devices are drastically minimized. Comparable to conventional MOSFET, in case of Dual Gate MOSFET, both gates control the properties of channel from both sides and have better electrostatic control over the channel. Thus more scaling of gate length can be performed in DG MOSFETs. DG MOSFETs are better alternative of conventional MOSFETs because DG MOSFETs have better control on short channel effects. Also DG MOSFETs have higher current density, higher sub threshold swing at low supply voltages. Therefore performance of the devices can be maintained in terms of higher current density and low leakage by employing DG MOSFETs. In DG MOSFETs better control of short channel effects and threshold voltage is achieved ideally without altering the concentration of channel dopants. This technique diminished the statistical dopant fluctuations [9] and also reduces the phenomena of impurity scattering. In addition, depletion charge cannot exist because there are no impurities in the channel. Many structures and techniques have been proposed to reduce short channel effects in SOI devices [10-11]. These limitations can be overcome by using double-gate (DG) MOSFETs. The conventional MOSFET cannot be scaled down below 10 nanometre process technology. Therefore DG MOSFETs are widely employed in the analog electronic circuits where reduced short-channel effects, electronic gain control capability, high breakdown voltages are required. DG MOSFETs are fabricated in below 20nm fabrication process technology by using metal gate technology for both the gates that diminished the poly depletion effects. The adverse effects, such as mobility degradation [12] and random microscopic

fluctuations of dopant atoms are eliminated due to the absence of dopant atoms in the channel material of DG MOSFETs. Due to these advantages, an analytic and simple threshold-voltage model is highly desirable for un-doped DG MOSFETs as one of the key point parameter for the design of such nano-scale devices. More advantages of Dual Gate MOSFETs are improved trans-conductance, early voltage and carrier transport efficiency. Accurate and physics-based computationally efficient formulations are required for implementation of high speed VLSI circuits comprising of compact MOSFET model. Due to these requirements for the device, the un-doped symmetric DG MOSFETs are best suited device structure because of the thin and un-doped nature of the channel. In the situation of surface inversion near oxide-silicon interface, the energy band bends up to $2\Phi_B$ at the silicon-oxide interface. The same phenomena can be utilized for the analysis of the uniformly doped carrier concentration in the substrate. For the analytical modeling of the 2-D characteristics of Double-Gate MOSFETs, the two dimensional Poisson's equations are analyzed by using suitable initial and final boundary conditions. Concept of Green's function techniques are used to get the solution for the two dimensional Poisson's equation considering the uniform doping profile. The analytical modeling of double gate MOSFET's has been reported by several authors [13-19]. For the optimization of the performance of the devices in nano meter regime for low power applications, threshold voltage of the DG MOSFETs should be properly modeled. In the next section, solution of the two dimensional Poisson's equation in substrate regions are discussed using the Green's function technique along with the boundary conditions. The analytical expression for 2-Dimensional threshold voltage in the substrate is derived explicitly and verified by previous existing 2-Dimensional analytical models.

II. STRUCTURE OF DG MOSFET

Figure 1 discusses about the general structure of DG MOSFETs. In this structure of DG MOSFET two gates namely gate-1 and gate-2 are used. Due to double gate structure, gate to channel coupling is enhanced and hence short channel effects are considerably suppressed. DG MOSFETs are categorized as either symmetric DG MOSFET or asymmetric DG MOSFET depending upon the way the voltages are applied to both gates. These two metal gates may

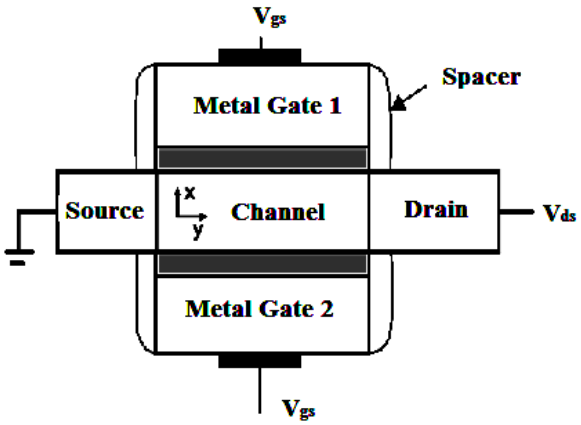

Fig.1 Structure of General DG-MOSFET

or may not have same work functions. The terms symmetric and asymmetric depicts the presence or absence of symmetry of the electric field in the both channel regions of the DG MOSFETs. In this research work analysis is done for symmetric DG MOSFETs. The symmetric DG MOSFETs means that the both the gates have the same work function, the thickness of the top and bottom gate oxide are equal and the same voltage bias is applied to both gates. After application of V_{ds} and V_{gs}, it is assumed that the Quasi-Fermi level is constant along the x direction, current in the channel flows in the y direction and assumed negligible in the x direction as shown in the Figure 1. Where x is the direction across the channel thickness and y is the direction along the channel.

III. MODEL DERIVATION AND VERIFICATION

A. The Basic Analysis:

The cross-sectional view of a thin-film Dual Gate MOS device for 2-Dimensional analytical model is shown in Fig.2. For a rectangular domain, Green's function can be expressed in a hyperbolic-sine form, with some Dirichlet and Neumann boundary condition along the rectangular region. The simplified domains for the analytical solution for the 2D Poisson's equations [20-23] along with the suitable boundary conditions are listed in equation (1). The domain for the solution of the 2-D Poisson's equation in Si region, as shown in Fig. 1, in which t_{ox} is thickness of the front and back gate-oxide region and t_{si} represents thickness of the Si film region. Considering the two-dimensional Poisson's equation in a rectangular coordinate system shown in fig.1, the 2D Poisson equation in silicon region is

$$\Delta^2 \emptyset\,(\mathrm{x,y}) = -\frac{\rho(\mathrm{x,y})}{\varepsilon_{si}} = \frac{qN_A f(y)}{\varepsilon_{si}}\,,\quad 0 \le y \le t_{si}\,, 0 \le x \le L$$

Where N_A is substrate acceptor doping concentration and $f(y)$ is the doping profile in Si region. The 2-D Poisson's equations in the front and back oxide regions are reduced to the 2-D Laplace equations, because charge density is neglected in oxide region.

$$\left.\begin{array}{ll} \emptyset\,(0,\mathrm{y}) = V_{bi}(y) & 0 < y < t_{si} \\ \emptyset(L,y) = V_{bi}(y) + V_{ds} & 0 < y < t_{si} \\ D_{sf}(x,0) = \in_{si} E_y(x,0) & 0 < x < L \\ D_{sb}(x,t_{si}) = \in_{si} E_y(x,t_{si}) & 0 < x < L \end{array}\right\} \quad (1)$$

Where

$$E_y(\mathrm{x},0) = \frac{\partial\phi(\mathrm{x,y})}{\partial y} = \frac{C_{ox}}{\varepsilon_{si}}\left[V_{gs} - V_{fb} - \phi_s - \frac{Q_0}{C_{ox}}\right],\quad E_y(\mathrm{x},t_{si}) = \frac{\partial\phi(\mathrm{x,y})}{\partial y} = -\frac{C_{ox}}{\varepsilon_{si}}\left[V_{gs} - V_{fb} - \phi_s - \frac{Q_0}{C_{ox}}\right] \quad (2)$$

The concept of Green's function technique is utilized for solution of the 2-Dimensional Poisson's potential distribution in Si region with different types of boundary conditions on DG-MOSFET's. The Green's function solution in Si region is used and summarized in equations (4-7). Substituting the Green's function solution into Green's theorem [16], this is given as

$$\emptyset(x,y) = \iint \frac{\rho(x',y')}{\varepsilon} G(\mathrm{x,y};\,x',y')\,dx'dy' + \int G(\mathrm{x,y};\,x',y')\frac{\partial\phi}{\partial n'}ds' - \int \Phi\,(x',y')\frac{\partial G}{\partial n'}ds' \quad (3)$$

Where $G(\mathrm{x,y};\,x',y')$ is the Green's function satisfying $\Delta^2 G = -\delta(\mathrm{x}-x')\,\delta(\mathrm{y}-y')$, n' is the outward normal direction on the boundary surface, and neglecting the free carriers.

$$G_x(x,y;x',y') = \frac{2}{L}\sum_{n=1}^{\infty}\frac{\sin(K_n x')\sin(K_n x)\sinh(K_n y)sinhK_n(t_{si}-y')}{K_n sinhK_n t_{si}}, \mathrm{y} < y' \quad (4)$$

$$G_x(\mathrm{x,y};\,x',y') = \frac{2}{L}\sum_{n=1}^{\infty}\frac{\sin(K_n x')\sin(K_n x)\sinh(K_n y')sinhK_n(t_{si}-\mathrm{y})}{K_n sinhK_n t_{si}}, \mathrm{y} > y' \quad (5)$$

$$G_y(\mathrm{x,y};\,x',y') = \frac{2}{t_{si}}\sum_{m=1}^{\infty}\frac{\sin(K_m y')\sin(K_m y)\sinh(K_m x)sinhK_m(L-x')}{K_m sinhK_m L}, \mathrm{x} < x' \quad (6)$$

$$G_y(\mathrm{x,y};\,x',y') = \frac{2}{t_{si}}\sum_{m=1}^{\infty}\frac{\sin(K_m y')\sin(K_m y)\sinh(K_m x')sinhK_m(L-\mathrm{x})}{K_m sinhK_m L}, \mathrm{x} > x' \quad (7)$$

.

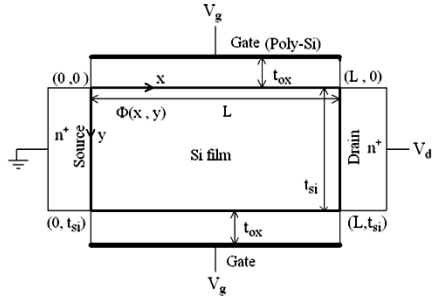

Fig.2 Schematic Cross section of DG-MOSFET

The equation (3) is general expression for electrostatic potential distribution and it can be used for any arbitrary doping profile in the channel region of Si film where $\rho(x',y') = -qN_A f(y')$ defined as the charge density of Si region. For simplicity we are assuming Si film as uniformly doped ($f(y') = 1$) in the following analysis. Two-dimensional potential equation is obtained

$$\emptyset\,(\mathrm{x,y}) = \frac{-\mathrm{q}N_A}{2\varepsilon_{si}}\mathrm{x}(\mathrm{L}-\mathrm{x}) + V_{bi} + V_{ds}\frac{\mathrm{x}}{\mathrm{L}} + \sum_{n=1}^{\infty}\frac{sinK_n x}{\varepsilon_{si}k_n \sinh k_n t_{si}}\left[D_{sf}^m coshk_n(t_{si}-y) - D_{sb}^m coshk_n y\right] \quad (8)$$

where D_{sf}^m and D_{sb}^m is front and back gate electric displacement. The potential $\emptyset\,(\mathrm{x,y})$ must satisfy the boundary conditions at the SiO_2-Si interface,

$$\frac{\partial\phi(\mathrm{x,y})}{\partial x}\Big|_{\mathrm{y}=0^+} - \frac{\partial\phi(\mathrm{x,y})}{\partial x}\Big|_{\mathrm{y}=0^-} = 0 \quad (9)$$

$$-\varepsilon_{si}\frac{\partial\phi(\mathrm{x,y})}{\partial y}\Big|_{\mathrm{y}=0^+} + \varepsilon_{ox}\frac{\partial\phi(\mathrm{x,y})}{\partial y}\Big|_{\mathrm{y}=0^-} = 0 \quad (10)$$

After solving equation (9) & (10) and we can obtain

$$D_{sf}^m = \frac{\varepsilon_{ox}[B.D\varepsilon_{si}k_n \sinh k_n t_{si} - C.sinK_n x]}{[B.\varepsilon_{si}\sinh k_n t_{si} + B.\varepsilon_{ox}\cosh k_n t_{si} - A.\varepsilon_{ox}].sinK_n x} \quad (11)$$

where coefficients

$$A = \frac{sinK_n x}{K_n}\left\{\frac{1}{\varepsilon_{ox}} + \frac{1}{\varepsilon_{si}\tanh k_n t_{si}} - \frac{1}{\varepsilon_{si}\sinh k_n t_{si}}\right\},\qquad B = \frac{sinK_n x}{K_n}\left\{\frac{1}{\varepsilon_{si}\sinh k_n t_{si}} - \frac{1}{\varepsilon_{si}\tanh k_n t_{si}} - \frac{\tanh k_n t_{ox}}{\varepsilon_{ox}}\right\} \quad (12)$$

$$C = \frac{2sinK_m t_{ox}}{t_{ox}K_m \sinh k_m L}\{V_{bi}sinhK_m(L-x) + (V_{bi}+V_{ds})sinhK_m x\},\ D = \frac{4(V_{gs}-V_{fb})sinhK_n x}{n\pi\cosh k_n t_{ox}} + \frac{\mathrm{q}N_A}{2\varepsilon_{si}}\mathrm{x}(\mathrm{L}-\mathrm{x}) - V_{bi} - V_{ds}\frac{\mathrm{x}}{\mathrm{L}} \quad (13)$$

B. Threshold Voltage Model:

The location of the minimum surface potential X_{min} lies on Si surface and can be found by solving

$$\frac{\partial \Phi\,(x,\ y)}{\partial x}\Big|_{x=x_{min},y=0,t_{si}} = 0 \tag{14}$$

From equation (9), the position of the minimum surface potential x_{min} can be obtained as

$$\frac{\varepsilon_{ox} cosh k_n t_{si}}{E}\left\{\frac{qN_A}{\varepsilon_{si}}\frac{x_{min}(L-x_{min})K_n}{tanK_n x_{min}} - \frac{qN_A}{2\varepsilon_{si}}x_{min}(L-2x_{min}) - \frac{V_{ds}}{L} - \frac{2V_{ds}}{L}\frac{x_{min}K_n}{tanK_n x_{min}} - \frac{2V_{bi}K_n}{tanK_n x_{min}} + \frac{4(V_{gs}-V_{fb})}{L.cosh k_n t_{ox} tanK_n x_{min}}\right\} - \frac{qN_A}{2\varepsilon_{si}}x_{min}(L-2x_{min}) + \frac{V_{ds}}{L} = 0 \tag{15}$$

the expression for minimum surface potential $\phi_{sf,min}$ is simplified as from above equation (15)

$$\Phi_{min}(x_{min},0) = \frac{-qN_A}{2\varepsilon_{si}}x_{min}(L-x_{min}) + V_{bi} + V_{ds}\frac{x_{min}}{L} + \sum_{n=1}^{\infty}\frac{sinK_n x_{min}}{\varepsilon_{si}k_n \sin hk_n t_{si}}\left[D_{sf}^{m} cosh k_n t_{si} - D_{sb}^{m}\right] = \Phi_{s,min} \tag{16}$$

The threshold voltage, V_{th} for the DG-MOSFET model is derived from the analytical approach followed in [24]. The threshold voltage definition in terms of surface potential is expressed by

$$V_{th} = V_{fb} + \left\{2\Phi_f + \frac{-qN_A}{2\varepsilon_{si}}x_{min}(L-x_{min}) - V_{bi} - V_{ds}\frac{x_{min}}{L}\right\}\frac{\{sinK_n x_{min}\}^{-1}}{2G_f} - \frac{P}{2G_f} \tag{17}$$

Where

$$G_f = [1-(-1)^n]\frac{R}{d_0}\left[\frac{2}{m\pi cosh k_n t_{ox}} + \sum_{m=1}^{\infty}\frac{t}{(m-.5)\pi}\left[(-1)^m - \frac{1}{(m-.5)\pi}\right]\right],\ R = -\frac{\varepsilon_{si}}{\varepsilon_{ox}}\frac{\tan hk_n t_{ox}}{\sin hk_n t_{si}},\ t = \frac{4}{n\pi}\left[1 + \frac{L^2(m-.5)^2}{{t_{ox}}^2 n^2}\right] \tag{18}$$

$$d_0 = \frac{1}{(\sin hk_n t_{si})^2} - \left\{\frac{\varepsilon_{si}}{\varepsilon_{ox}}\frac{\tan hk_n t_{ox}}{\tan hk_n t_{si}} + \frac{1}{\tan hk_n t_{si}}\right\}^2,\quad P = \frac{1}{d_0}\{[1-(-1)^n]\frac{qN_A L^2}{2\varepsilon_{si}}\frac{8R}{(n.\pi)^3} + T[V_{bi}(1-(-1)^n) + V_{ds}(-1)^{n+1}]\} \tag{19}$$

$$T = \sum_{m=1}^{\infty} 2Rt((m-.5)\pi)^{-2} - \frac{4R}{n\pi} \tag{20}$$

The general short channel V_{th} model is reduced to long channel {(L= ∞) in a long channel threshold voltage model} one

$$V_{th,long} = V_{fb} - \frac{P}{2G_f} \tag{21}$$

The threshold voltage roll-off ΔV_{th} expression is defined as the difference between the values of threshold voltage for short channel and long-channel devices given as

$$\Delta V_{th} = \left\{2\Phi_f + \frac{-qN_A}{2\varepsilon_{si}}x_{min}(L-x_{min}) - V_{bi} - V_{ds}\frac{x_{min}}{L}\right\}\frac{\{sinK_n x_{min}\}^{-1}}{2G_f} \tag{22}$$

IV. Results and Discussion

Figure 3 and Figure 4 show the various levels of Threshold voltage roll-off ΔV_{th} in the substrate along the channel length for various values of Si film thickness t_{si}= (1.5, 5, 10, and 25nm) at Gate oxide thickness $t_{ox} = 1nm$ and $t_{ox} = 1.5nm$ at same V_{ds} = *0.05V and* $N_a = 10^{17} cm^{-3}$ for proposed analytical model and Chen [24]. It can be seen from the graph that threshold voltage roll-off ΔV_{th} is sensitive to devices parameters like channel length, gate oxide thickness, Si film thickness, channel doping concentration and drain bias voltage. It can be seen that by reducing the channel length of the device, the threshold voltage roll-off can be increased. The thickness of Si film increases, threshold voltage roll-off also increases, as it is directly proportional to it. Here gate to gate potential distribution in parabolic type and uniform doping concentration. The curves in this case shifted right side with the increasing Silicon film thickness for constant drain to source biasing V_{ds} = 0.05V and constant gate oxide thickness $t_{ox} = 1nm$ and $t_{ox} = 1.5nm$. The result obtained from our model show the value of Threshold Voltage roll-off ΔV_{th} is 5-7% higher than Chen model.

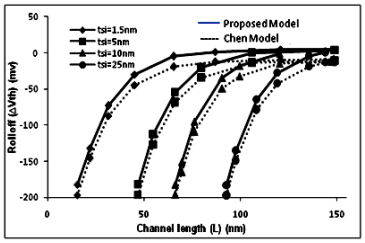

Fig.3. Comparison of the Chen [24] and proposed model for the DG-MOSFET, $t_{ox} = 1nm$

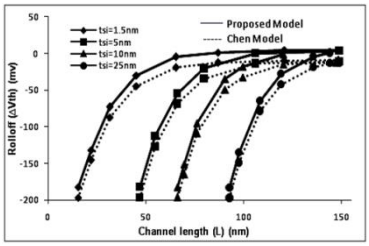

Fig.4 Comparison of the Chen [24] and proposed model for the DG-MOSFET, $t_{ox} = 1.5nm$

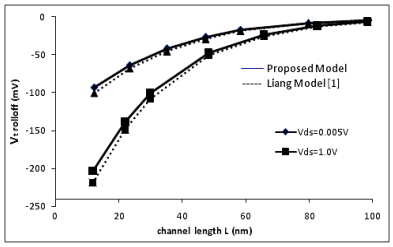

Fig. 5 Comparison of the Liang [1] and proposed model for the DG-MOSFET. $t_{si} = 10nm$ and $t_{ox} = 1.5nm$

Figure 5, shows the parametric analysis for threshold voltage roll-off along the channel length for various drain bias voltages V_{ds}= (0.005, 1.0V). The values of other parameters are gate oxide thickness $t_{ox} = 1.5nm$ and silicon film thickness $t_{si} = 10nm$. Above figure shows the threshold voltage roll-off ΔV_{th} for both low drain and high drain bias voltages. It can be observed that for higher drain bias, the roll-off is also higher. This is because for a fixed high

drain bias voltage, the shift in threshold voltage is higher for a long channel device as compared to the short channel device. Our proposed threshold voltage model variation with different parameter in 5-7% with existed Liang [1] model. It has been observed that the proposed model accurately predicts the device behavior and is in well agreement with the existing analytical model such as Liang [1] and Chen [24], with 3-5% more accurate.

V. CONCLUSION

The two dimensional Poisson's equations has been analytically derived using the concept of Green's function incorporating suitable initial and final boundary conditions in Silicon region. The accuracy of the proposed model in the substrate (Si-film) is analyzed and verified by existing models. The above model is valid for uniform doping profile in Si region. Due to the symmetry of DG-MOSFETS, the distributions of analytic potential for both sides of the surfaces in the substrate are same. It is obvious from simulation results so as to iterative method can only be used to find the position of the minimum surface potential. It can be easily analyzed that better results are obtained between the proposed model and Chen model analysis for parametric analysis of device structure for various biasing. The proposed analytic voltage model can be applied as a basic concept for high-speed physical analysis of the short-channel effects. It will define the deep-sub micrometer optimized scaling rule for thin-film Silicon on Insulator based MOS transistor in ULSI Technology.

REFERENCES

[1] Chunsheng Jiang, Renrong Liang,a Jing Wang, and Jun Xu, "A Two-Dimensional Analytical Model for Short Channel Junctionless Double-Gate MOSFETs" AIP ADVANCES vol 5, Issue 5, 0571223-13, 2015.

[2] Kiran Agarwal Gupta, Dinesh K. Anvekar, Venkateswarlu V., "Modeling of Short Channel MOSFET Devices and Analysis of Design Aspects for Power Optimization", International Journal of Modeling and Optimization, Vol. 3, No. 3, pp. 266-271, June 2013.

[3] Uygar E. AVCI, Daniel H. Morris, Ian A. Young, "Tunnel Field-Effect Transistors: Prospects and Challenges", Journal of the Electron Devices Society, Volume 3, No. 3, pp. 88-95, May 2015.

[4] A. Narendiran, K. Akhila, B. Bindu, "A Physics-Based Model of Double-Gate Tunnel FET for Circuit Simulation", IETE Journal of Research, Volume 62, Issue-3, 2016.

[5] Reza Hosseini, "Analysis and Simulation of a Junctionless Double Gate MOSFET for High-Speed Applications", Volume 67, Issue 9, pp 1615–1618, 2015.

[6] M. Salmani-Jelodar, H. Ilatikhameneh, S. Kim, K. Ng, G. Klimeck, "Optimum High-k Oxide for the Best Performance of Ultra-scaled Double-Gate MOSFETs", IEEE Transaction on Nanotechnology, pp. 1-5, 2015.

[7] Erdin Ture, Peter Brückner, Birte-Julia Godejohann, Rolf Aidam, Mohamed Alsharef, Ralf Granzner, Frank Schwierz, Rüdiger Quay, Oliver Ambacher, "High-Current Submicrometer Tri-Gate GaN High-Electron Mobility Transistors With Binary and Quaternary Barriers", Journal of the Electron Devices Society, Volume 4, No. 1, pp. 1-6, 2016.

[8] Stephen J. Bauman, Eric C. Novak, Desalegn T. Debu, Douglas Natelson, Joseph B. Herzog, "Fabrication of Sub-Lithography-Limited Structures via Nanomasking Technique for Plasmonic Enhancement Applications", IEEE Transactions on Nanotechnology, vol. 14, no. 5, pp. 790-793, 2015.

[9] Samar K. Saha, "Modeling Statistical Dopant Fluctuations Effect on Threshold Voltage of Scaled JFET Devices", IEEE Access Journal, Volume 4, pp. 507-513, 2016.

[10] Qian Xie, Chia-Jung Lee, Jun Xu, Clement Wann, Jack Y.-C. Sun, Yuan Taur, "Comprehensive Analysis of Short-Channel Effects in Ultrathin SOI MOSFETs", IEEE Transaction on Electron Devices, Vol. 60, No. 6,pp. 1814-1819, 2013.

[11**]** Jean-Pierre Colinge, "Multiple-gate SOI MOSFETs", Solid-State Electronics, Elsevier, Volume 48, Issue 6, June 2004, pp. 897–905, 2004.

[12**]** A. Cros, K. Romanjek, D. Fleury, S. Harrison, R. Cerutti, P. Coronel, B. Dumont, A. Pouydebasque, R. Wacquez, B. Duriez, R. Gwoziecki, F. Boeuf, H. Brut, G. Ghibaudo, T. Skotnicki, "Unexpected mobility degradation for very short devices : A new challenge for CMOS scaling", IEEE International Electron Devices Meeting, pp. 663—666, 2006.

[13] Z. Rajabil, A. Shahhoseini2, and R. Faez3, "The Non-Equilibrium Green's Function (NEGF) Simulation of Nanoscale Lightly Doped Drain and Source Double Gate MOSFETs" IEEE International Conference on Devices, Circuits and Systems (ICDCS), Coimbatore, India, pp. 25-28, March 2012.

[14] T. A. Karatsori, A. Tsormpatzoglou, C. G. Theodorou, E.G Ioannidis, S.Haendler, N.Planes,G., "Development of Analytical Compact Drain Current Model For 28nm FDSOI MOSFETs", 4th International conference on Modern Circuits and Systems Technologies, Thessaloniki Greece, page 1-4,14-15 May 2015.

[15] Suman Lata Tripathi, Madhuraj Kumar, R. A. Mishra, "3-D Channel Potential Model For Doped Symmetrical Ultra-Thin Quadruple Gate-All-Around MOSFET", Journal of Electron Devices, Vol. 21, pp. 1874-1880, May 2015.

[16] F.Ávila-Herrera, A.Cerdeira, B.C.Paz, M.Estrada, B.Íñiguez, M.A.Pavanello," Compact Model for Short-Channel Symmetric Double-Gate junction-less Transistors" Solid-State Electronics, vol 111,pp. 196–203, June 2015.

[17] Guang-Ming Zhang, Yi-Kai Su, Hsin-Yi Hsin, Yao-Tsung Tsai, "Double Gate Junctionless MOSFET Simulation and Comparison with Analytical Model" IEEE Regional Symposium on Micro and Nanoelectronics (RSM-2013), Langkawi, Malaysia, pp 410-413, 25-27 Sept, 2013.

[18] Vimal Kumar Singh Yadav, Ratul Kr. Baruah, "An Analytic Potential and Threshold Voltage Model for Short- Channel Symmetric Double-Gate MOSFET", International Symposium on VLSI Design and Test, Coimbatore, India, 16-18 July, 2013.

[19] Mini Bhartia. and Arun Kumar Chatterjee, "Modeling the Drain Current and its Equation Parameters for Lightly Doped Symmetrical Double-Gate MOSFETs", Journal of Semiconductors, Vol. 36, No. 4, 1-7, April 2015.

[20] Xiaoping Liang, Yuan Taur, "A 2-D Analytical Solution for SCEs in DG MOSFETs", IEEE Transactions on Electron Devices, Vol. 51, no. 9, pp.1385 – 1391, 2004.

[21] Shih-Ching Lo, Yiming Li and Shao-Ming Yu, "Analytical Solution of Nonlinear Poisson Equation for Symmetric Double-Gate MOSFET", Mathematical and Computer Modeling, Vol. 46, no. 1-2, pp. 180-188, 2007.

[22] TK Chiang, "A Novel Scaling-Parameter- Dependent Sub Threshold Swing Model for Double-Gate (DG) SOI MOSFETs: Including Effective Conducting Path Effect (ECPE)", Semiconductor Science and Technology, vol. 19, no. 12, pp. 1386 -1390, 2004.

[23] Huaxin Lu, Yuan Taur, "An Analytic Potential Model for Symmetric and Asymmetric DG-MOSFETs" IEEE Transactions on Electron Devices, Vol. 53, no. 5, pp.1161 – 1168, May 2006.

[24] Qiang Chen, E.M. Harrell, J.D. Meindl, "A Physical Short-Channel Threshold Voltage Model for Undoped Symmetric Double-Gate MOSFETs", IEEE Transactions on Electron Devices, Volume: 50 , Issue: 7 , July 2003.