Low Complex Parallel Adder Design with Reduced Delay

Abstract

The main focus of this paper is to implement parallel prefix adders by using majority gate. These structures reduce the delay and circuit complexity, and also verify the functionality for the arithmetic logical operations which are used in the processors and DSP applications. Parallel prefix adders are flexible and widely used for binary addition. These high performance parallel adders by using AND-OR logic, requires the logarithmic number of stages. Moreover, based on the majority gate, the emerging new and improved device technologies are possible and these adders based on the best existing majority gate has a delay of $(2*\log_2 n-1)$ of the n^{th} carry. This is better than the AND-OR logic has a delay of $(2*\log_2 n+1)$. This paper shows output carry is caused due to delay, to overcome this problem two novel recursive techniques are proposed in terms of majority gate. The first one is the new formation of majority gate based equation in the used group generation and propagation. These results are used to reduce the carry calculations thus reducing the delay. And second one is the recursive property of majority gate. This property describes a new method to redesign the basic operator. It is used in parallel prefix graph to reduce the delay as well as circuit complexity. The overall the proposed technique results in reducing the delay and circuit complexity of the output carry of n-bit adder in terms of majority gate.