An 18-bit incremental Zoom ADC with Reduced Delay Overhead Data Weighted Averaging for Battery Measurement Systems

***Abstract*—The paper presents a systematic implementation of 18-bit incremental zoom ADC for stacked lithium-ion battery voltage monitoring system with a reduced dynamic range analog front-end that comprises a resistive level shifter. A comparative study of the incremental zoom ADC and its incremental ADC counterpart, for a given modulator order, is presented in detail. The choice of incremental zoom ADC is demonstrated to be a best fit for an 18-bit resolution of the target application. Multi-bit DAC non-linearity is proven to be major bottleneck for the ADC performance. The performance of data weighted averaging (DWA) dynamic element matching (DEM) technique for improvising modulator linearity with 0.1 percent DAC component mismatch is analysed. DWA DEM is confirmed to meet an in-band SNDR of 108dB, operating on a 250kHz oversampled clock frequency, required for 18-bit modulator linearity with a 5-bit DAC. An SNR of 114dB is achieved with the first stage integrator thermal noise limited to 3.3 μV_{rms} over process voltage and temperature variations (PVT) using 0.35 μm CMOS process.**

Keywords*—Feed-Forward Sigma-Delta Modulator, Incremental zoom ADC, Incremental ADC, SAR ADC, Data Weighted Averaging, Battery Monitoring System.

I. Introduction

To reduce the CO_2 emissions in automotive vehicles future is to use electric vehicles (EVs) and hybrid electric vehicles (HEVs). Batteries play important role in the EVs and HEVs. Li-ion battery chemistry makes an attractive choice for the EVs and HEVs [1]. Depending upon the system requirements li-ion cells will be stacked to get the required voltage ranges up to 400V. In stacked system each cell needs to be monitored individually with the help of proper battery management system (BMS).

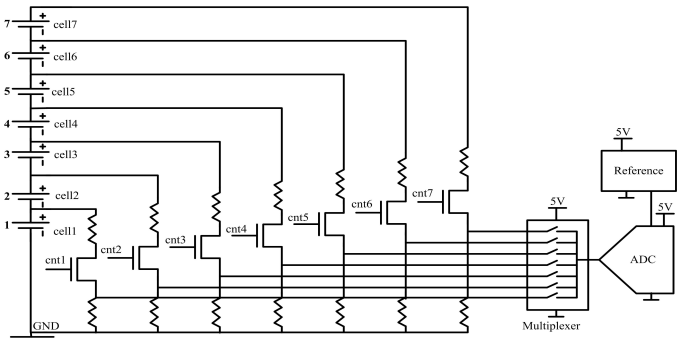

Fig. 1. Block diagram of the proposed battery measurement system

Based on the IC technology 5 to 12 stacked cells will be monitored using a single device. However, it is not so efficient to incorporate a dedicated ADC for every channel. In the current work, an area efficient solution for DC battery voltage monitoring system (BMS) of stacked lithium-ion (Li-ion) cells is proposed. It comprises a single ADC multiplexed across several channels as shown in Fig. 1. However, a resistive analog level shifter is used to attenuate the cell voltages into a single 5V domain. This attenuated input dynamic range from analog front-end presents very high accuracy and ADC resolution requirements for a given system resolution.

Incremental data converters (IADCs) are the traditional means of achieving high accuracy and high resolution systems for instrumentation and measurement systems [2]-[4] as these applications require absolute accuracy and cannot tolerate offset and gain errors. The static input nature, high resolution requirements and need to multiplex, altogether, best suits an incremental ADC (IADC) for the target application. A recently proposed incremental zoom ADC [5] is chosen for the target application due to its high energy efficiency. This paper presents the design of an ADC for 18-bit resolution at 8ms throughput rate to suit the requirements of targeted BMS.

The rest of the paper is organised as follows. Section II presents a comparative study that presents the pros and cons of incremental zoom ADC over its incremental ADC counterpart. The measures taken to address ADC design challenges are summarised in section III. Section IV describes the circuit implementation of the ADC. Simulation results are discussed in section V. Finally, section VI concludes the paper.

II. Comparative Study

A. Conventional Incremental ADC

The conventional incremental ADC comprises of a front-end sigma-delta modulator (SDM) and a decimator at back-end, like sigma-delta ADCs. It is the incremental operation of IADCs that distinguishes them from their free running sigma-delta ADC counterparts. The architecture of IADCs establishes input and output mapping to ensure high absolute accuracy. The mapping process involves resetting of all the memory elements that includes integrators of the modulator and back-end decimator. As a result, the IADCs can be readily multiplexed which makes it a suitable choice for portable sensor applications due to its compact realization.

The low distortion feed-forward sigma delta modulator (FFSDM) topology is chosen for the modulator implemen-

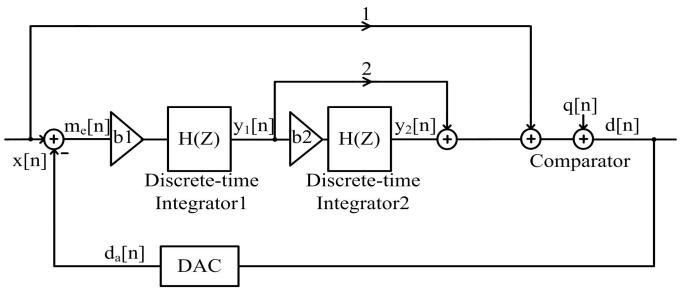

Fig. 2. Block diagram of second-order FFSDM of IADC2

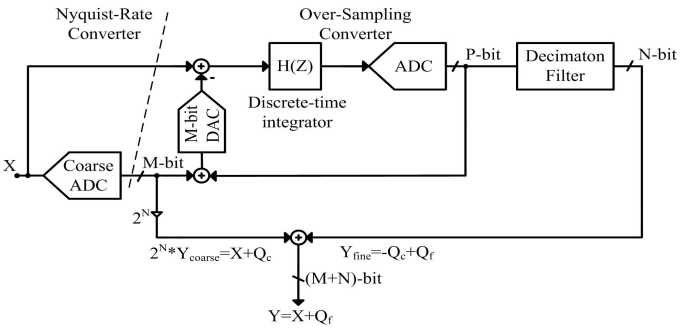

Fig. 3. Block diagram of 1^{st} order incremental zoom ADC

tation. FFSDM topology offer several advantages over conventional SDM. It presents relaxed distortion requirements on the integrators, for a given resolution, as it eliminates the need for integrators to operate on high-pass filtered input signal [6]. Moreover, the FFSDM relax the integrator output swings, compared to conventional modulator where integrators are to operate on superposition of high-pass filtered input and quantization error of the loop comparator. It offers reduced area overhead due to elimination of dedicated feedback DAC for each integrator in the modulator.

The second order IADC (IADC2) can be considered for the target 18-bit resolution as first order implementation severely limits the ADC throughput rate, whereas the higher order implementations present severe stability concerns. The second order FFSDM modulator incorporated into the design of IADC2 is shown in Fig. 2. The oversampling ratio (OSR) required for IADC2 for 18-bit operation can be best derived from time domain analysis. Eq. (1) expresses the output of

$$y_2(N) = b1.b2 \sum_{m=0}^{N-1} \sum_{n=0}^{m-1} (x[n] - d[n]) \tag{1}$$

$$|({}^{N}C_2)\bar{x} - \sum_{m=0}^{N-1} \sum_{n=0}^{m-1} d[n]| = \frac{V_{max}}{b1.b2} \tag{2}$$

second stage integrator of modulator on its Nth cycle, which is double summation of the weighted modulator error (m_e). Through the choice of proper integrator gain coefficients(i.e b1,b2), the incremental operation can exercise a maximum bound on the second stage integrator output(i.e. +/- Vmax). Eq. (2) outlines the conversion principle of an IADC2 as it defines a bound on error between unknown input signal and an expression made out of known digital bit stream values (i.e. d[n]) of the modulator. Thus by choosing an higher OSR (N) the quantization error associated with a sample can be brought down to realize higher resolutions. For an 18-bit resolution, with the ADC operating on a maximum input of 80 percent of 2.5V reference, the OSR required is calculated to be about 1280, with following numericals (i.e. V_{max}=1V , b1=.33 and b2=.5). This shows IADC2 results only in a moderate throughput rate.

The critical building blocks that affect the overall performance of IADC2 include operational amplifier (op-amp) used in the first stage integrator (Int1). The impact of op-amp non-idealities such as offset, finite gain, and bandwidth on the modulator linearity is analysed. It is found that in addition to auto-zeroing for Int1, minimum op-amp gain of 100dB and a bandwidth that corresponds to a settling error of one-fourth LSB is necessary for target 18-bit resolution. The thermal noise of the op-amp of the first stage integrator is another anomaly that can potentially limit [7] the resolution attainable from IADC2. In fact, the fractional gain coefficients (i.e. attenuation factors) make the constraints on output referred noise of the integrator more severe due to amplified input-referred noise. This in turn requires more power to meet the noise requirements for a given resolution.

B. Incremental Zoom ADC

The architecture of 1st order incremental zoom ADC is shown in Fig. 3. It comprises of a coarse nyquist-rate converter and fine over-sampling converter. The final digital output of the zoom ADC is a resultant of fine and coarse conversions. The zoom architecture is a hybrid that encompasses the principles of two-step ADC and is robust to its non-idealities. It eliminates the need to compute the residue. In fact, both coarse and fine converters operate on the same input signal. However, following coarse conversion, the coarse code is used by the fine converter's DAC to dynamically zoom into a coarse LSB reference range around the input signal to eliminate the residue computation. Moreover, this considerably relaxes the resolution requirements of the back-end over-sampling converter and further improves its energy efficiency due to reduced voltage swings at internal nodes.

The second-order incremental zoom ADC (IZADC2) is considered for the target requirements of 18-bit resolution. The coarse ADC is realized with energy efficient successive approximation register (SAR) architecture and the fine over-sampling converter is chosen with architecture of IADC2 discussed in the earlier section. However, the resolution of the IADC2 of zoom architecture is quite relaxed that alters the design constraints on its critical buildings blocks and also provides higher throughput rate. More importantly the reduced internal node swings enable the op-amp to be better optimized for linearity and noise performance.

A 5-bit resolution (i.e. M=5) is chosen for coarse ADC, which is sufficient enough to relax the swing and resolution requirements of back-end IADC2. The circuit level behavioural implementation is built to analyze the impact of non-idealities on the performance of IZADC2. The simulations substantiate that only a gain of 60dB for the op-amp of the first stage

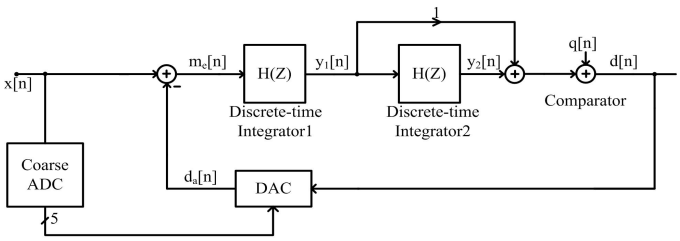

Fig. 4. Block diagram of modified 2^{nd} order FFSDM for IZADC2

integrator is sufficient to ensure 18-bit resolution of IZADC2. The thermal noise constraints of the first stage integrator are also considerably reduced as the zoom architecture no longer requires the IADC2 to employ fractional gain coefficients for its first stage integrator. Simulations show that the IZADC2 requires an over-sampling ratio (OSR) of about 280 for the target SQNR of 118dB, thereby, to get atleast thermal noise limited SNR of about 108dB.

Hence the IZADC2 is chosen for the target application as it is more robust and energy efficient solution compared to its conventional counterpart, IADC2. However, it presents different set of challenges due to the presence of multi-bit feedback DAC of over-sampling converter, which can limit the overall resolution of the zoom ADC. This is usually addressed with dynamic-element-matching (DEM) techniques that significantly reduce the non-linearity associated with DAC component mismatch.

III. Systematic Design Considerations

The IADC2 discussed in the earlier section requires adaptation for the requirements of the zoom ADC with subtle changes as shown in Fig. 4. It doesnt require the input feed-forward branch as the internal signal swings are reduced as a result of zooming.

The coarse conversion carried out with SAR ADC does suffer non-idealities such as offset due to component mismatch. In order to avoid the effect of the non-idealities on the subsequent fine conversion, redundancy is incorporated between and fine and coarse conversion. This is practically realized by making the fine converter to operate on two LSB coarse reference range. However, this results in an increased OSR for a given resolution. Simulations indicate an OSR of about 380 is required for the target 118dB SQNR. To ease the design of back-end decimator, an OSR of 512 is chosen [5]. The final ADC output incorporating a one-bit overlap between coarse and fine conversion results is expressed as follows:

$$Y = 2^{N-1} * Y_{coarse} + Y_{fine}. \tag{3}$$

The back-end decimation filter is chosen to be a sinc^2 filter, rather than cascaded-integrator-comb (CIC) filter, due to its symmetrical transfer function which makes it more resilient to the ripple introduced in the output bit stream as a result of DEM techniques. However, it requires the modulator to work for double the theoretical OSR (i.e. 1024).

Auto-zeroing (AZ) technique is incorporated into first stage integrator as an offset correction technique. However,

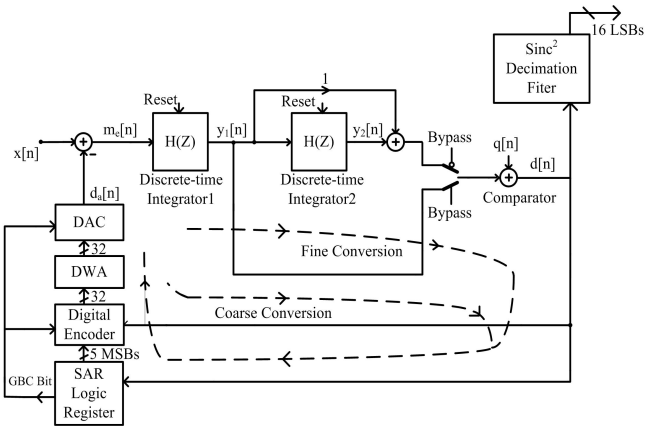

Fig. 5. Block diagram of resource shared 2^{nd} order incremental zoom ADC

simulations indicate that AZ in itself is not sufficient to achieve the targeted accuracy of 16-bits. Thus chopping at system level is incorporated into the design which requires the ADC to resolve the same input twice with swapped input polarities and take the final result as a difference average of the two results. This makes the required OSR to about 2048.

The multi-bit feedback DAC incorporated into IADC2 for fine reference generation can potential limit the overall linearity of the modulator due to component mismatch. Thus data weighted averaging (DWA) is incorporated into the design as a dynamic element matching technique which averages the component mismatch by a rotation methodology, as will be described later, thereby improving the linearity of the modulator. DWA introduces a propagation delay in the modulator loop, however, this is minimal as compared to multi-bit sigma-delta implementations, as the fine converter operates on only two consecutive LSB reference range throughput its operation.

IV. Circuit Implementation

The resourced shared circuit implementation proposed in [5] is employed due to its compact and efficient realization as shown in Fig. 5. It enables the reconfiguration of the same building blocks as coarse SAR ADC and fine IADC2 to optimize on chip area by eliminating the redundant circuitry.

During coarse conversion, the first stage integrator of the modulator is made to operate as a sample-and-hold (S/H) amplifier, which is facilitated by the same reset signal required for the incremental operation of the modulator. The output of the S/H amplifier is bypassed to the input of the comparator, which drives the SAR logic that completes the loop as required by SAR ADC. It resolves one bit at a time using binary search algorithm. Hence it requires M clock cycles to perform coarse conversion. This conversion time is far negligible as compared to over-sampling required for subsequent fine conversion.

At the end of SAR conversion, one more guard band conversion (GBC) cycle is carried out in zoom architecture. During which one more bit (i.e. GBC Bit) is resolved which indicate whether the input lies in the lower-half or upper-half of the coarse LSB. This helps us make a better choice of two LSB reference range for subsequent fine conversion that always safely keep the input at mid-reference range. For example, if the coarse SAR conversion gives an output code

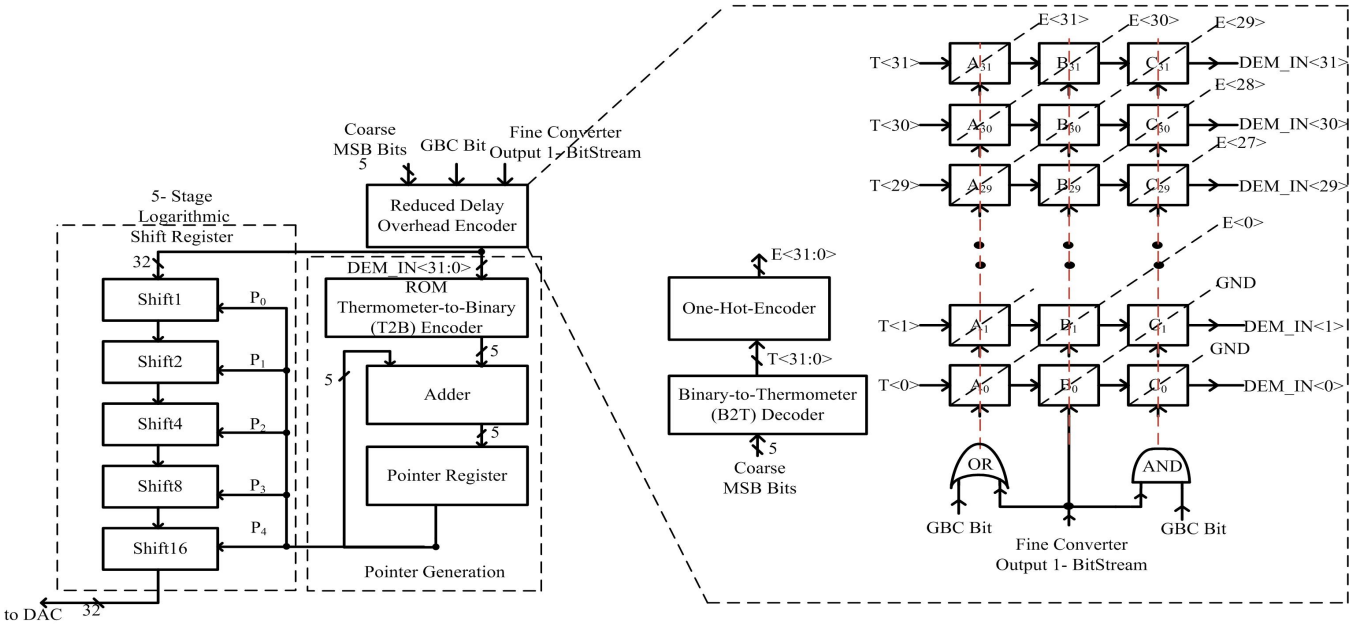

Fig. 6. Block diagram of proposed reduced delay overhead DWA realization

that corresponds to a k^{th} LSB of the reference. Then, if GBC bit is 0 (i.e. current input lies in lower-half LSB), the two LSB reference range for fine conversion is chosen as (k-1)th LSB and (k+1)th LSB. Otherwise, if GBC bit is 1, then k^{th} LSB and (k+2)th LSB is chosen. Thus, the guard band correction avoids input overloading and prevents the modulator output from saturation.

The component mismatch induced non-linearity of DAC is the major bottleneck that limits the overall linearity of the modulator. There are various DEM techniques that are used to improve the linearity of DAC. Tree structured DEM is most area efficient solution available in the literature [8], with second-order DAC noise shaping. However, it doesnot suit applications that target resolutions as high as 18-bit. Data weighted averaging (DWA) DEM technique particularly suits resolutions greater than 18-bit [9] with just first-order DAC noise shaping.

DWA algorithm involves cyclic rotation of the unary elements in the DAC by choosing the next available unused element in it. This requires the knowledge of past history of input codes to the DAC, which is often kept track of using a DWA pointer. An efficient implementation [10] of the DWA DEM is shown in Fig. 6. It comprises of a pointer generator (PGR) and a logarithmic shifter. The accumulator used for the pointer generation performs the binary addition. Hence, it requires a thermometer-to-binary (T2B) decoder to change the thermometer code, which feeds the unary-weighted DAC, into binary format. T2B decoder is realized using an efficient ROM based implementation. The cyclic rotation is implemented using an area-efficient 5-stage logarithmic shifter. The PGR of DWA is usually decoupled from the signal feedback path to avoid delay overhead on feedback signal path.

However, for the IZADC2, the thermometer code for reference selection is not readily available, unlike in multi-bit sigma-delta ADCs. The back end fine converter references are selected based on single-bit modulator output and previous coarse conversion result along with GBC bit. This reference selection circuitry is now part of the feedback signal path. If not addressed, the associated delay overhead can stretch the required integration period, thereby, limit the modulator throughput. This reference selection can possibly be made using an n-bit binary Adder/Subtractor followed by binary-to-thermometer code generator. However, this is not an efficient way due to the huge propagation delay associated and area overhead.

A novel reduced delay overhead encoder for reference selection, shown in Fig. 6, is incorporated into DWA of IZADC2. It comprises of a binary-to-thermometer (B2T) encoder, one-hot-encoder and three sequentially connected layers of multiplexers. Each of these layers comprises a stack of thirty-two two-input analog multiplexers to enable true thermometer encoding required for DWA. The output of the B2T decoder is held constant throughout the fine conversion due to the fact that back end references just straddles across known coarse code. The one-hot-encoder generates the control signals, E<31:0>, for the multiplexers such that the vertical inputs are feed forward, whenever it generates a control signal high, otherwise, horizontal inputs are feed forward. Table. I gives a numerical example for a input binary code of 4. The LSB of

TABLE I. REDUCED DELAY OVERHEAD ENCODER FUNCTIONALITY

GBC	BitStream	Coarse MSBs	T<0:31>	E<0:31>	D<0:31>
0	0	00100	01111000..(4)	00001000..	01110000..(3)
0	1	00100	01111000..(4)	00001000..	01111100..(5)
1	0	00100	01111000..(4)	00001000..	01111000..(4)
1	1	00100	01111000..(4)	00001000..	01111110..(6)

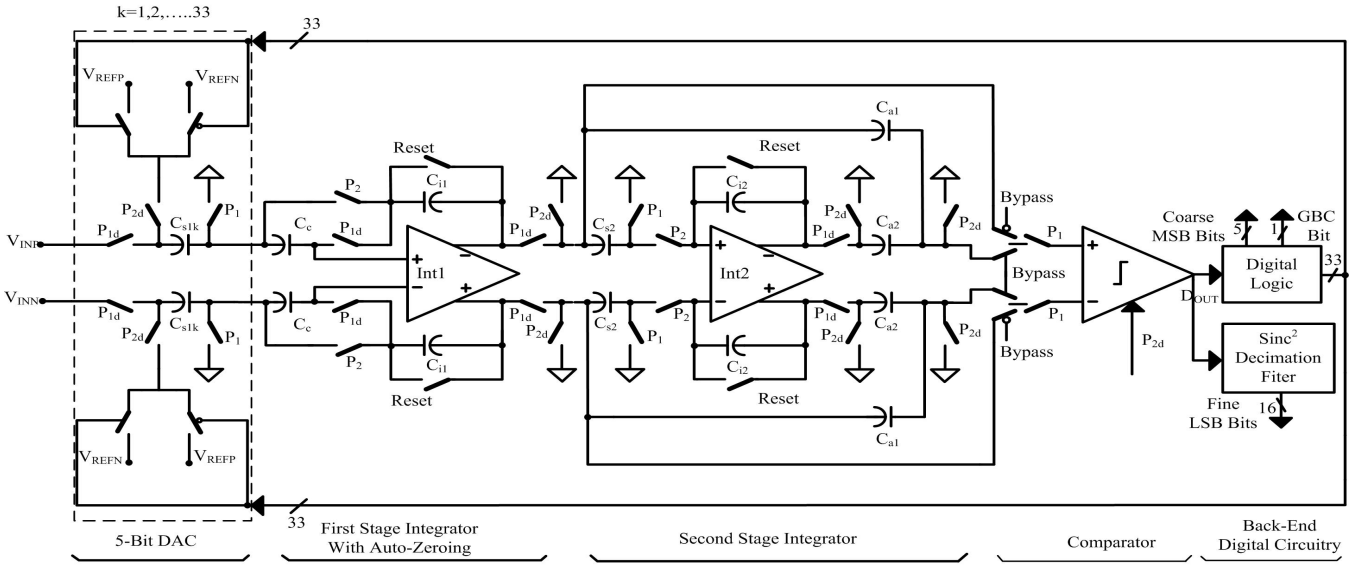

Fig. 7. Circuit implementation of 2^{nd} order incremental zoom ADC

the thermometer code T<0> is always tied to zero to facilitate binary search algorithm used for SAR coarse conversion. Thus, for any arbitrary input code k, on a range of 1 to 29, the encoder maps the output to a true thermometer code of either k-1, k, k+1 or k+2 depending on the GBC and BitStream inputs.

A fully differential circuit implementation of the second order incremental zoom ADC is shown in Fig. 7. It requires two phase non-overlapping clock generation for its operation. Due to relaxed op-amp gain requirements of only about 60dB, for first stage integrator, it can easily be realized with simple folded-cascode architecture. Moreover, the relaxed integrator swings is another reason to limit the op-amp architecture just to a single stage implementation.

The first stage integrator sample capacitor C_{s1} in itself requires to be operated as a 5-bit DAC in the integration phase followed by sampling phase. This requires the sample capacitor C_{s1} to be split into 32 identical unit elements of 375 fF each which is sufficient enough to ensure atmost 0.1 percent mismatch required for DWA. The differential input to the modulator (i.e. $V_{IN} = V_{INP} - V_{INN}$) is sampled on to all the 32 elements in the sampling phase. In the following integration phase, reference (i.e. $V_{REF} = V_{REFP} - V_{REFN}$) is differentially sampled on to k-elements of the DAC. The reference with opposite polarity (i.e.-V_{REF}) is sampled on to rest of the (32 - k) elements. As a result of these operations, the first stage integrator accumulate the differential voltage represented by the following expression $V_{IN} + ((2k - 32)/32).V_{REF}$ on to its integration capacitor. To facilitate GBC cycle, an extra capacitance element is incorporated into the DAC that is made to sample only reference but not input.

As discussed in the previous section, the thermal noise performance of the first stage integrator is critical for overall attainable resolution. Of the two components of thermal noise, op-amp thermal noise and KT/C of sample capacitors (C_{s1}) shown in Fig. 7, the op-amp noise constraints require the careful choice of op-amp architecture and sufficient quiescent power to be burned. Whereas, the KT/C_{s1} noise can only be limited by choosing a higher capacitance. Thus, the first stage sample capacitance is chosen with a value of 12pF, in order to limit the KT/C_{s1} noise to -120dB across temperature range of -40^{o}C to 125^{o}C with an OSR of 1024. This helps us achieve the op-amp thermal noise limited output of at least 18-bits. An auto zeroing (AZ) technique is incorporated into the first stage integrator (Int1) as a dynamic error correction technique. It eliminates the offset using a compensation capacitance (C_c) that is twice the sample capacitance (i.e. 24pF).

The gain settings of the first and second stage integrator are chosen as 1.23 and 0.5 respectively, in order to limit the integrator swings as required for incremental operation of zoom ADC. In order to meet the throughput requirements of about 8ms for overall ADC conversion, the modulator is chosen to operate with a sample frequency of 250 KHz. Both the integrators are designed with a unity-gain-bandwidth of about 4MHz which is required to ensure the settling error of one-fourth LSB corresponding to overall ADC resolution of 18-bits. The Int1, with a scaling factor of four, is adopted for second stage integrator (Int2). A latched comparator preceded by a preamplifier is chosen which can easily ensure atmost half-LSB comparator offset required for fine conversion.

V. SIMULATION RESULTS

The second order incremental zoom ADC is implemented in Cadence environment using AMS 0.35 μm process on a 5V power supply. All the analog building blocks are implemented at transistor level. Whereas the design of digital building blocks is restricted to circuit level behavioural implementation. The linearity of the op-amp is characterized by configuring the first stage integrator as a sample and hold amplifier. Spectral

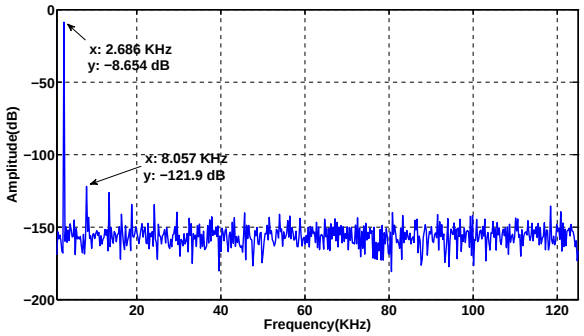

Fig. 8. 1024-point output PSD of first-stage integrator configured as S/H amplifier

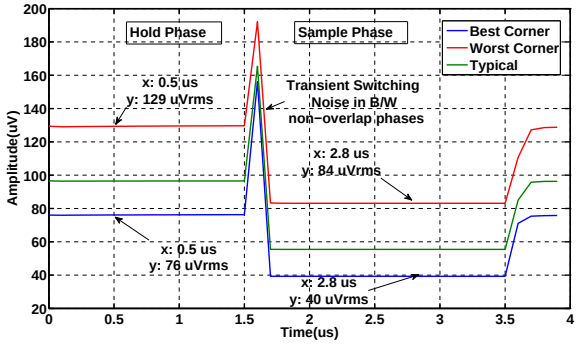

Fig. 9. output integrated RMS noise of first stage integrator across PVT corners

analysis is carried out on the amplifier output, whose PSD density is shown in Fig. 8. The amplifier is found to have an SFDR of about 113 dB.

The noise analysis of first-stage integrator is carried out using PSS+PNOISE simulations by configuring it as S/H amplifier to facilitate PSS simulation. The integrated output RMS noise of the integrator for the two non-overlap phases is shown in Fig.9 across corners with a maximum of 129 μV_{rms}. This output RMS noise, with an integrator gain of 1.23, if referred to the input gets about 104 μV_{rms}. This noise power corresponds to an SNR of 113.6 dB, with an OSR of 1024, with ADC operating on a differential input of$\pm$2.25 V. Thus, dominant first stage integrator thermal noise limited ADC output realizes a resolution of about 18.3 bits.

In order to analyze the impact of component mismatch of the capacitive DAC, a random mismatch of maximum 0.1 percent is incorporated into the DAC. With DWA DEM turned off, the mismatch induced DAC noise results in a much elevated noise floor of 103dB in the PSD of free running modulator shown in Fig. 10. With DWA averaging turned on, the in-band noise is spectrally shaped to ensure required 18-bit operation. The performance of DWA is observed to be coarse code or input dependent. DWA ensures superior performance at lower coarse codes as compared to higher codes. The DWA ensured a worst case SNDR of about 108.3 dB, with the modulator operating on a maximum DC differential input of 2.25V.

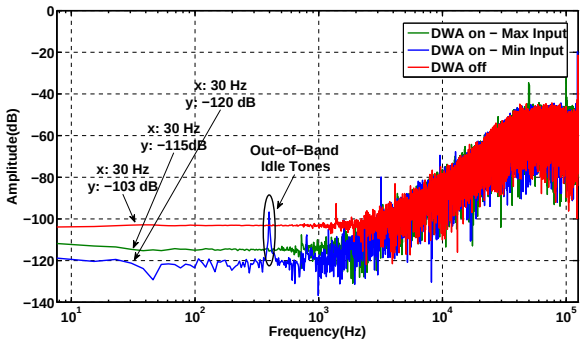

Fig. 10. 32768-point output PSD of the free-running modulator with 0.1 percent DAC capacitive mismatch

VI. Conclusion

The design of an 18-bit incremental zoom ADC in AMS 0.35 μm CMOS process is presented. The choice of incremental zoom ADC is demonstrated to be a best fit for the target application. An SNR of 114dB is achieved with the first stage integrator thermal noise limited to 3.3 μV_{rms} over PVT variations. The non-idealities that affect the ADC performance are analyzed in detail. Dynamic-error-correction techniques are incorporated to address the non-idealities. A novel DWA encoder realization, for incremental zoom ADC, with reduced delay overhead is proposed for high throughput required. DWA DEM ensured an in-band SNDR of 108dB, with a maximum differential DC input of 2.25V, operation on 250 kHz oversampled clock frequency.

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