Design and Implementation of an Efficient VLSI Architecture for 10T Full Adder used in Ultra Low Power Applications

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ABSTRACT:

Full adder is an important digital design for development of many digital systems. For an efficient digital system design an area efficient and high speed full adder is very much needed. This full adder is very much needed for ultra low power applications. In this paper an efficient VLSI Architecture is proposed for the 10T full adder. The proposed VLSI architecture consumes less power, less area and operates at higher speed. This VLSI architecture has been implemented using 180nm technology using Generic Process Design Kit(GPDK) with the help of Cadence Design suite. The VLSI architecture can be synthesised with reduction in power and high speed. The proposed VLSI architecture has been compared with different full adder cells.The proposed full adder architecture performance can be analyzed by using parameters such as energy,propogation delay, leakage power and total power.

Keywords: 10T Full adder, Propagation delay, Power consumption.

I. INTRODUCTION

The full adder is an important building block in any digital system. Full adder is a basic element in circuits such as comparators, multipliers, shifters etc.[1]. Adder is also useful in the design of digital signal processors, micro processors to implement arithmetic operations. Any digital design performance can be analysed depending on several parameters such as delay, speed, power consumption, area, estimation of critical path etc. In this paper the full adder performance can be analysed by estimating the delay and power consumption. The main purpose of this work is to reduce the delay so as to achieve high speed and minimizes the power consumption [5]. This work is carried out under cadence EDA environment in 90nm technology. The objective of this work is to design an efficient full adder which can be used for ultra low power applications [2].

Power consumption is an important parameter which is depends on the supply voltage V_{DD}. Reduction in power consumption can be obtained by scaling V_{DD} using scaling factor 1/β. Power reduction can also be done by using power down mode concept [3]. Delay is another important parameter to assess the performance of any digital circuit design [6]. During the measurement of delay, estimation of critical path delay is very important. This delay is entirely responsible to estimate the speed of the digital systems. In this paper both delay and power [4] are estimated using cadence EDA environment. The typical circuit diagram of 1-bit full adder is shown in figure 1.

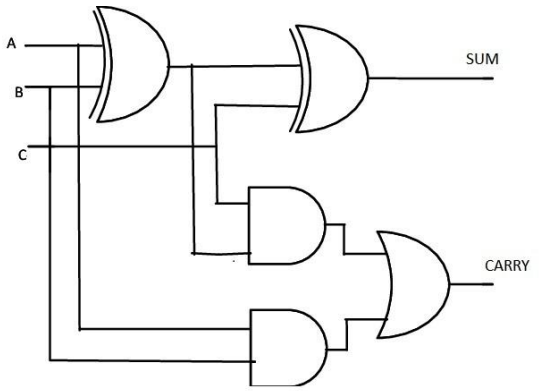

Fig 1. Circuit diagram of full adder

SUM = A xor B xor C

CARRY= AB + BC + CA

The truth table for one bit full adder is shown in table I.

Table I . Truth table for 1 bit full adder

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

This paper is organized as follows section 1 describes introduction, section 2 discusses the related work, section 3 covers the proposed work, section 4 demonstrates the result, finally section 5 concludes the work.

II.RELATED WORK

In this section, existing full adder circuits [2],[5],[6] are discussed. In the full adder design [2], it exhibits poor functionality in sub threshold region. If they are operated in 1.8V as supply voltage then they are exhibiting different output voltage levels. For example Figure 2 shows the full adder 1 schematic diagram with the a,b,c as inputs and sum, carry as outputs. In the figure 2 it has the output of sum as HIGH when the vector inputs ABC equal to 001, but the output shows 1.2V instead of 1.8 V in the Figure 9. This shows the worst case output of the full adder1.[7] And then next in Figure 3 Full adder 2 is shown. It is designed to reduce the delay with same number of transistors. Here the sum output is LOW when the vector combination of inputs ABC is 110. But the output in Figure 10 shows the sum output as 1V instead of gnd. Hence this shows the worst output case in the full adder 2. To reduce the worst case outputs full adder 3 is designed and is shown in Figure 4. In the figure 4, the full adder 3 has 10 transistors as same as the above full adders and the carry output has to show HIGH, when the vector input ABC equal to 101 but the carry output in Figure 11 shows the 1.3V instead of 1.8V. Hence this case also considered as worst output case for the fulladder3 [8]. In the figure 5, full adder 4 is designed by using an inverter for the input c. Then for the vector ABC equal to 110, the sum output has to show 0 and carry output as 1. Instead of these values carry output showing 1.2V.Hence the full adder 4 is also considered as non functional adder or unacceptable adder. In the figure 6, the full adder5 is shown. This full adder shows 2V as carry output for the vector input case ABC equal to 010. Hence this case also treated as unacceptable. Thus full adder 5 is completely nonfunctional at deep sub threshold levels [9].Hence our normal full adder with the expressions shown above is designed with 28 transistors is shown in figure 7 with the name as full adder 6. Full adder 6 takes more silicon area to design because it has more number of transistors than the above full adders. But the worst case outputs compared to the above full adders is reduced as shown in the figure 14[10]. But the main disadvantage of this circuit is the more consumption of the silicon area. Hence the proposed architecture is designed in the next section.

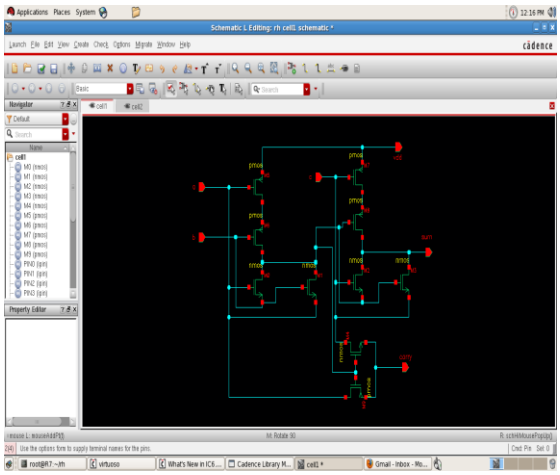

Fig.2 Fulladder1 schematic diagram

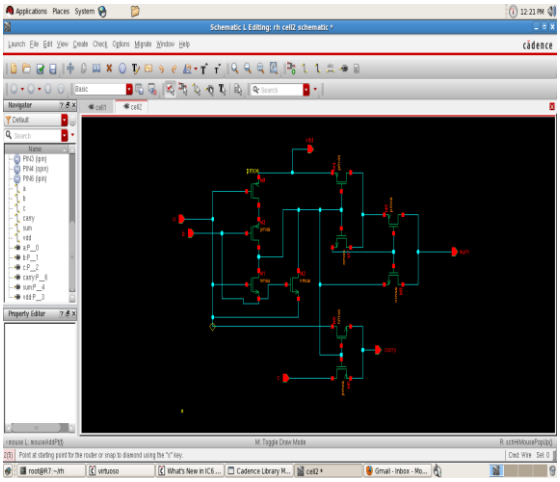

Fig.3 Full adder 2 schematic diagram

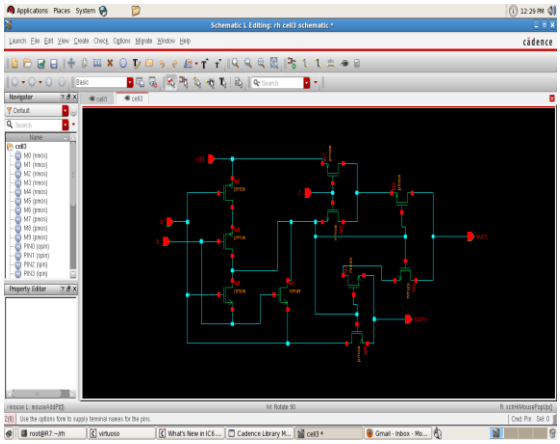

Fig.4 Fulladder3 schematic diagram

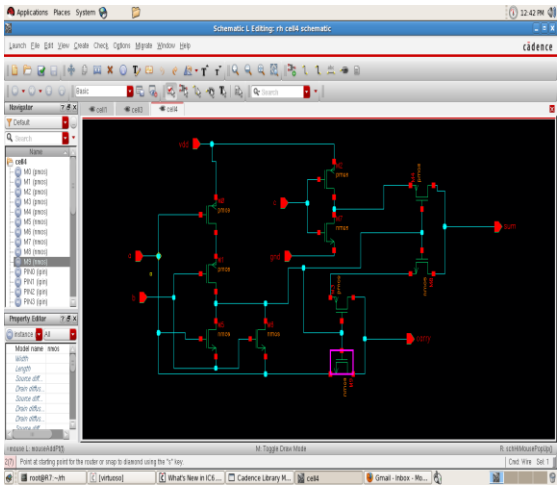

Fig.5 Fulladder4 schematic diagram

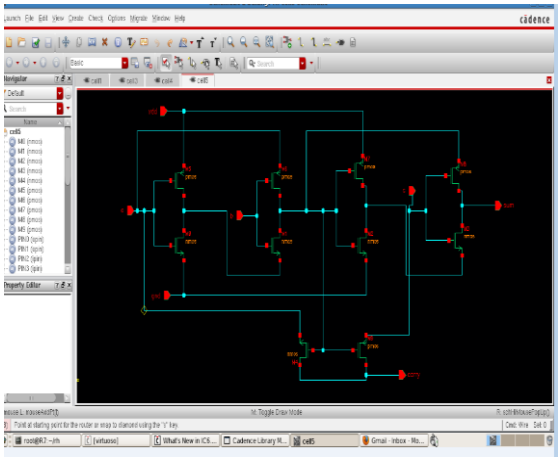

Fig.6 Fulladder5 schematic diagram

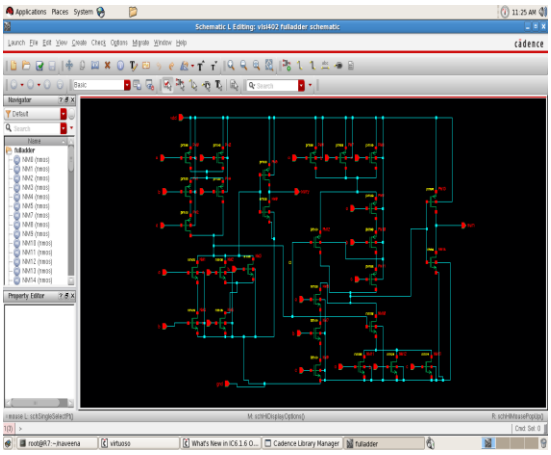

Fig.7 Fulladder6 schematic diagram

III. PROPOSED WORK

The existing designs has no perfect output level at 1.8V for the case of HIGH and no perfect output level of 0V for the case of LOW. This is called degradation of output voltage levels. In order to overcome this drawback, the proposed work incorporates decreasing of W/L ratios of 10 transistors. The technology also changed from 180nm to 90nm to overcome the existing drawback [2]. In order to restore the logic levels, the proposed work introduces device aspect ratio reduction and also reduces the value of β. For ultra low power applications full output voltage swing is required which has been proposed in this work. The proposed full adder circuit is shown in figure 8 consisting of 10 transistors in which uses xor gates. The first 4 transistors is considered as xor gate 1 and the nest four transistors is considered as xor gate 2 and the input c is constructed as back to back transistors. If A xor B is 1 then the output is shown as A or else if A xor B is equal to 0 then the output is C. The Output of the proposed full adder is shown in figure 15.

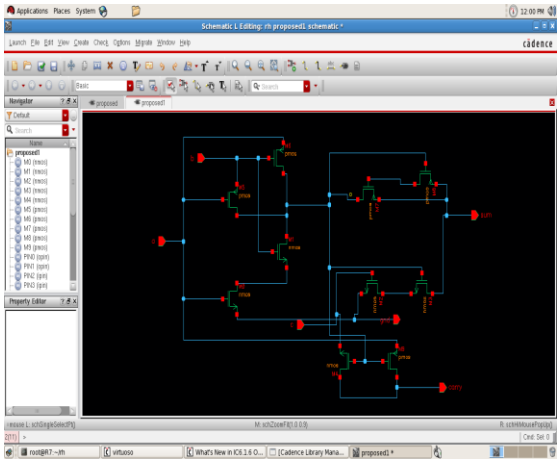

Fig. 8 Proposed Schematic diagram of Full adder

IV RESULTS:

The existing Full adder simulated in cadence EDA tool under 90nm technology. The simulation results for various full adders are shown in figures 9-14. The existing results show that there is a degradation of the output levels of all the full adders.

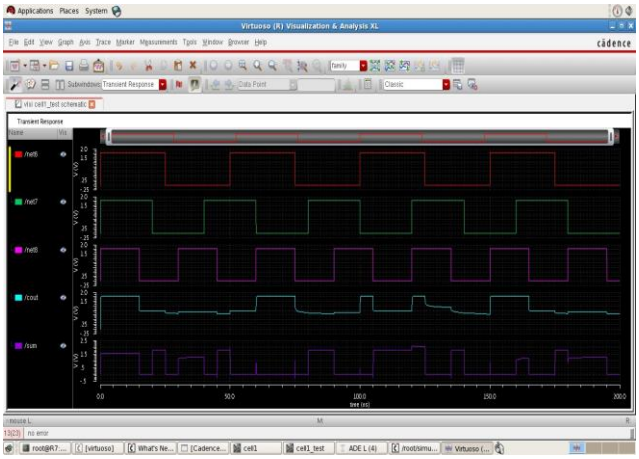

Fig.9 Output Of Full Adder 1 [2]

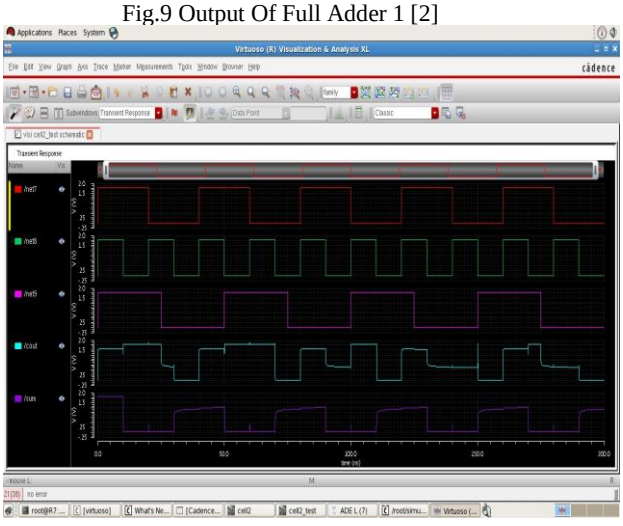

Fig.10 Output Of Full Adder 2 [2]

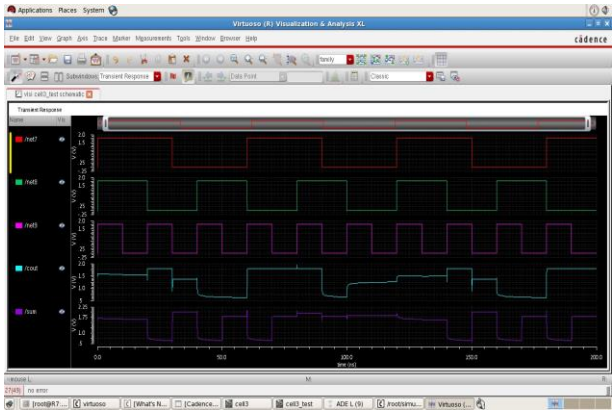

Fig.11 Output Of Full Adder3 [2]

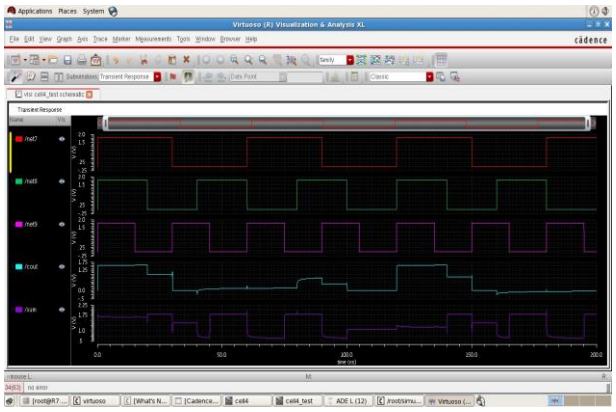

Fig.12 Output Of Full Adder4 [2]

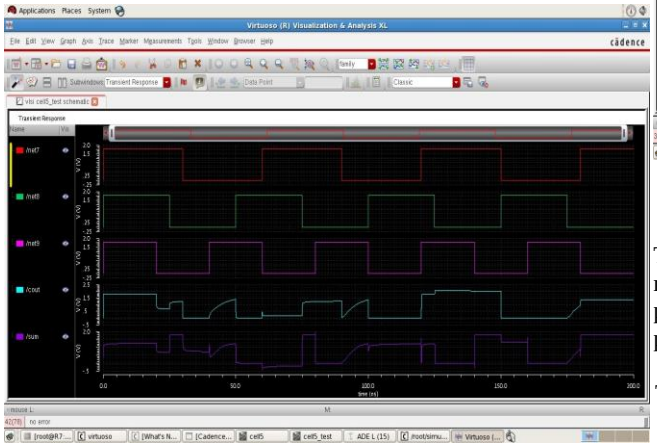

Fig.13 Output Of Full Adder 5[2]

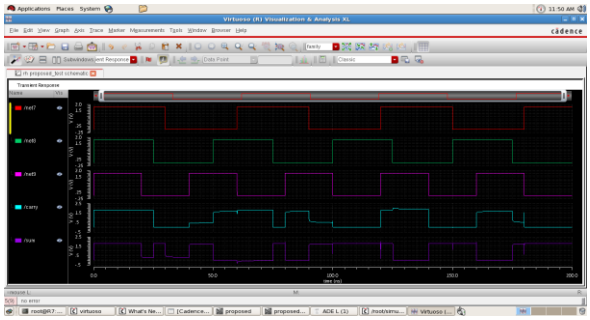

Fig.14 Output Of Full Adder 6 [2]

The proposed work also simulated in cadence EDA tool under 90nm technology. The simulated results are shown in figure 15 for 10T Full adder. The simulation results shows that there is no degradation in the output levels which are suitable for ultra low power applications. The simulation results also free from glitches which reduces the power consumption and also avoids unnecessary transitions in the logic levels. Due to avoiding of unnecessary transitions the power consumption also drastically reduced. The simulation results also show that the signal travels through the shortest critical path from input to the output of the Full adder circuit. This shortest critical path will results in less delay so as to achieve highest speed for Full adder which is required to implement an efficient digital systems. The delay also reduced due to reduction in the width of the transistors which are there in the critical path.

The average power is to be considered as an efficient parameter for estimation of power consumption instead of dynamic power consumption in cadence EDA environment.

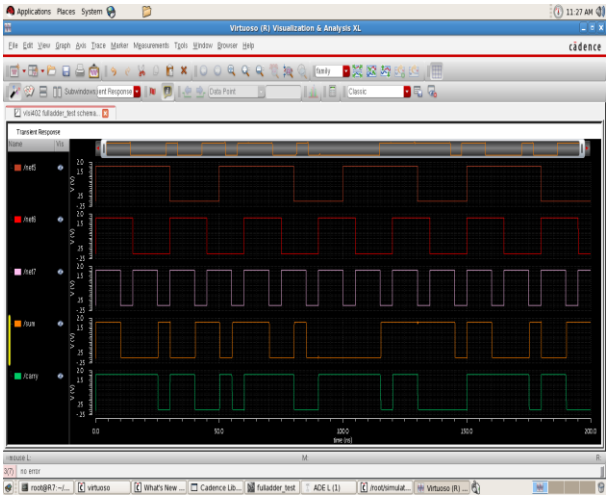

Fig.15 Output of Proposed Method

The comparison has been performed between the existing method and proposed method shown in table II. The proposed results shows that delay and average power proved to be better compared to existing results.

Table II. Comparison of Existing method and proposed method for delay and average power

Full adder	Existing[2]						Full adder (Proposed)
	Full adder 1	Full adder 2	Full adder 3	Full adder 4	Full adder 5	Full adder 6	
Delay (10^{-8} sec)	10.94	10.68	8.50	9.23	9.89	10.60	7.79
Average Power (10^{-10} W)	4.874	4.923	4.762	3.869	5.667	3.678	2.096

The comparison of delay and average power for the existing and proposed work is shown in graphical representation in figures 16 and 17.

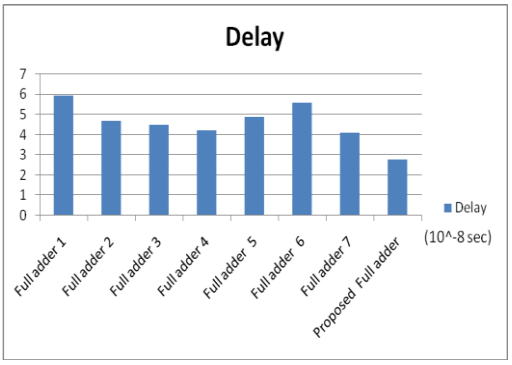

Fig. 16 Comparison of Delay for both proposed and existing full adders

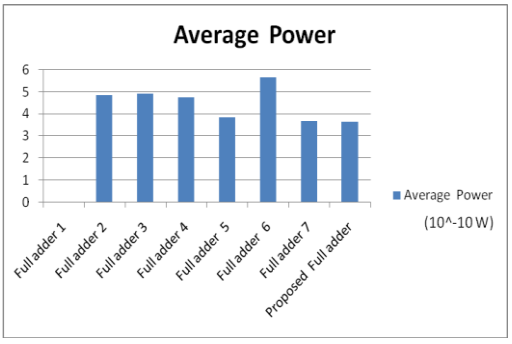

Fig. 17 Comparison of Average power for both proposed and existing full adders

V. CONCLUSION

The proposed full adder has been implemented in 90nm technology under cadence EDA environment. The proposed design proved that it consumes less power and it operates at higher speed by 10% compared to the existing architectures have been developed and standardized collaboratively by using the VLSI architecture. In this paper a one bit full adder using 10T is proposed which uses optimum energy point having transistors W/L ratio equal to 11.1 at 90nm technology. This design is suited for ultra low power applications such as IoT devices, energy harvesting etc.

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