**A Low Power, High Speed 18-Transitor True Single Phase Clocking D Flip-Flop Design In 90nm CMOS Technology**

Low-power VLSI designs are progressing because of the growing interest in mobile applications, such as the Internet of things, Wearable devices or Healthcare associated equipment. In those kinds of battery working equipment, power reduction is a very important issue, and demand for power reduction in VLSI is increasing. Flip-Flop (FF) designs are crucial to the power consumption performance of the system design and may also considerably impact the chip area. The Flip-Flops are mainly used as a memory storing elements in mobile phones, digital camera and tablet PC.

A Conventional Transmission-Gate-based FF (TGFF) is most widely used FF currently. This design suffers from a high capacitive clock loading problem, which indicates sustained power consumption even when the input remains static. This problem also occurs in Conventional SRFF designs. To overcome the power consumption problem, two FF designs employing an Adaptive Coupling technique and a Topologically Compressed (TC) scheme have been proposed. Adaptive Coupled FF (ACFF) design uses a differential latch structure with pass-transistor logic to achieve True Single-Phase Clocking(TSPC) operation. ACFF design can lower the power consumption significantly but suffers from a power leaking problem and has a longer Setup time. The TCFF design based on use the single clock pulse, reduce the number the transistor driven clock, and reduce the total transistor count. TCFF design has significant improvement in the power consumption, timing performance and suffers longer Setup time. A low-power true single-phase clocking flip-flop design achieved using only 19 transistors is proposed using logic structure reduction scheme. It has poor hold time performance.

In the proposed work a low power, high-speed 18-transistor true single-phase clocking D flip-flop(FF) design using complementary pass transistor logic. This design is a master-slave-type logic structure and hybrid logic design consisting of complementary pass-transistor logic style and static CMOS logic style. In existing FF design, 19 transistors were used which increases delay, power consumption, and area of utilization. To reduce the transistor count and to simplify the circuit complexity logic structure reduction scheme is used. In this design state transition is faster in the slave latch which enhances time performance using a virtual VDD technique. The circuit is designed using GPDK 90nm CMOS technology and the simulation results show that the proposed design exceeds in all performance indices such as average power consumption, clock-to-Q delay, data-to-Q delay, PDP and area of utilization.

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