**DESIGN OF LOW- POWER HIGH- PERFORMANCE 2-4 AND 4-16 MIXED-LOGIC LINE DECODERS**

Line decoders are fundamental circuits, widely used in the peripheral circuitry of memory arrays like SRAM, multiplexing structures, implementation of Boolean logic functions and other applications.They are implemented with the mixed-logic methodology in order to improve the performance when compared to single style design.Due to the advantage in favor of the line decoders that are designed mostly suitable for applications where area and power minimization is of primary concern and used in the blocks of design of larger decoders, multiplexers and combinational circuits.

The Existing work is decoders are implemented by using the conventional cmos technology which results in the large transistor count for the implementation of 2-4 and 4-16 decoders. CMOS logic is characterized by robustness against voltage scaling and transistor sizing and thus reliable operation at low voltages and small transistor sizes . Input signals are connected to transistor gates only, offering reduced design complexity and facilitation of cell-based logic synthesis and design. .

The proposed work introduces a mixed-logic design method for line decoders, combining transmission gate logic, pass transistor dual-value logic and static CMOS. Two novel topologies are presented for the 2-4 decoder, a 14-transistor topology aiming on minimizing transistor count and power dissipation and a 15-transistor topology aiming on high power-delay performance. Both a normal and an inverting decoder are implemented in each case, yielding a total of four new designs. Furthermore, four new 4-16 decoders are designed, by using mixed-logic 2-4 pre-decoders combined with standard CMOS post-decoder. All proposed decoders have full swinging capability and reduced transistor count compared to their conventional CMOS counterparts. Finally, the mixed logic design shows that the proposed circuits present a significant improvement in power and delay, outperforming CMOS in almost all cases.