**VLSI Architectures for DWT using efficient MBE**

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**Abstract** In this paper, we analyze the lifting and flipping discrete wavelet transform (DWT) and proposed an hardware efficient lifting 2-D DWT architecture. Large number of multipliers are used in DWT computation so significant saving in multipliers when lifting and flipping 2-D DWT is implemented. We have derived full-parallel lifting-based 2-D DWT structure involves M/2 number of less MBEs than the flipping-based 2-D DWT structure. The proposed lifting-based and flipping-based structures, respectively, involve 6.4 times, 5.8 times less ADP, and 3.8 time 2 times less EPI for block-sizes 32.The flipping scheme only offers area-delay efficient 2-D DWT structures for smaller block sizes less than 4, where lifting-scheme offers area-delay efficient 2-D DWT structures for block size higher than 4.

**Keywords**  VLSI Architecture. Discrete Wavelet Transform (DWT). Multiplier. 2-D DWT

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**1 Introduction**

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WT offers a wide variety of useful features such as adaptive time frequency windows, lower aliasing distortion, multi-resolution signal analysis, and efficient computational complexity. Due to these features one dimensional (1-D) DWT and two dimensional (2-D) DWT are applied in various application such as numerical analysis [1], signal analysis [2], image coding [3, 4], pattern recognition [5], statistics [6], biomedicine [7] and three dimensional (3-D) DWT for video processing, volumetric data compression [8]. Multi-dimensional DWT is computationally intensive and many of its applications demand real-time processing for better performance. Therefore, DWT need to be implemented in dedicated very large scale integration (VLSI) systems for real-time applications. During last two decades, several computation schemes, algorithm mapping, and architectural design methods have been suggested to derive an area-delay efficient VLSI architecture for DWT. Therefore, we discuss here the most commonly used computation schemes in DWT structures.

DWT is a two-channel short-length finite impulse response (FIR) filter-bank, where FIR filters are used in DWT known as wavelet filters satisfy orthogonal property. Most importantly, lifting-based DWT structure involves less arithmetic and memory resources than the convolution based DWT for the same throughput rate implementation [20]-[24]. But, we find that the flipping scheme introduces some design complexities in selected DWT structures which make the structure area-delay inefficient compared to the corresponding lifting-based structure. Therefore, in this paper we made a detail study on lifting and flipping DWT arithmetic computation to find most appropriate multiplier to derive area-delay efficient 2-D DWT structure. we suggest the our multiplier is most efficient to compute area-delay efficient high-throughput 2-D DWT structures. The rest of the paper is organized as: Multiplier unit for lifting and flipping DWT in Section 2. Section 3 discusses lifting and flipping 2-D DWT and the proposed full-parallel lifting and flipping structure are presented in Section 4. Performance comparison presented in Section 5 and Conclusions are given in Section 6.

**2. Lifting 2-D DWT**

Using separable approach 1-D lifting DWT computation is performed row-wise and then column-wise to obtain 2-D DWT output. The multi-level decomposition the low-low sub-band (LL) decomposed into four sub-bands namely low-low (*A*), low-high (*B*), high-low (*C*) and high-high (*D*) sub-bands. The following set of recursive relations are derived for row-wise computation of the multi level 2-D lifting DWT for 9/7 filter are as:

(6)

Where *α*, *β*, *γ* and *δ* are lifting constants. Since the computation of the low-pass and high-pass components of intermediate outputs (*ul*(*m*, *n*) and *uh*(*m*, *n*)), respectively, are of similar form, the computation of those components for column-wise computation is expressed as:

(7)

Where *x*(*m, n*) represents the low-low sub-band components of (*j*-1)-th level. *u*(*m*, *n*) represents the intermediate output corresponding to the input *x* (*m, n*), which could be low-pass and high-pass component *ul*(*m*,*n*) and *uh*(*m*, *n*) respectively.

Similarly, *vh* (*m*, *n*) is the high-pass output corresponding to the intermediate output *ul*(*m*, *n*) and *uh*(*m*, *n*) respectively, which respectively, represents a pair of level sub-bands outputs *B*(*m*, *n*) and *D’*(*m*, *n*). *vl*(*m*, *n*) is the low-pass output corresponding to the intermediate output *ul*(*m*, *n*) and *uh*(*m*, *n*) respectively, represent the other two level sub-band outputs *A’*(*m*, *n*) and *C*(*m*, *n*).

The low-pass and high-pass output of lifting 1-D DWT are scaled to normalize their values.

The scale normalization of row and column lifting DWT can be integrated and performed in one step after the column computation, where sub-band outputs *B*(*m*, *n*) and *C*(*m*, *n*) not required scaling while sub-band outputs *A’*(*m*, *n*) and *D’*(*m*, *n*) are scaled by:

*vll* =

*vhh*  (8)

**3. Flipping for 2-D DWT**

Recursive relations for row-wise computation of the multi level 2-D flipping DWT for 9/7 filter are given as:

(9)

The computation of the low-pass and high-pass components of intermediate outputs (*ul*(*m*, *n*) and *uh*(*m*, *n*)), expressed as:

(10)

The scale normalization of row and column flipping DWT can be performed after the column computation, where sub-band outputs *A’*(*m*, *n*), *B*(*m*, *n*), *C*(*m*, *n*) and *D’*(*m*, *n*) are scaled by:

*vll* =

*vlh* = *B* (*m*, *n*) = *B* (*m*, *n*)

*vhl* =*C* (*m*, *n*) =  *C* (*m*, *n*)

*vhh* = (11)

**4. Proposed efficient multiplier based full-parallel Lifting and Flipping 2-D DWT structures**

Multiplier is the basic arithmetic component to compute the multiplication operations in the lifting and flipping based 2-D DWT structures. Large number of multiplications are using for computation of DWT filter output. Multiplication process needs to large amount of area on the VLSI chip. Therefore we require a efficient area based multiplier unit keep this in mind we have designed a radix-4 based modified Booth multiplier for multiplication of filtering coefficients with input data.

The proposed structure for lifting and flipping 2-D DWT used a multiplier unit is shown in Fig. 8. It consists of one row processor and one column processor. The column processor is composed of one low-pass block and one high-pass block. During every cycle, the row-processor receives 2*M* samples corresponding to two successive columns of input matrix such that the entire input matrix of size (*M* × *N*) is fed to the row processor in *N*/2 cycles. The row processor produces one column of low-pass one column of high-pass intermediate matrices of sizes (*M* × *N*/2) in every cycle. The structure of row-processor for lifting 2-D DWT is shown in Fig, 9 and for flipping 2-D DWT is shown in Fig.10. Both these structure are identical except the lifting and flipping cell.

Fig. 10.emf

**Fig.8** Proposed full parallel structure for lifting and flipping 1-level 2-D DWT

The column processor receives data directly from the row-processor without any data transposition. During every cycle, the column processor receives one column of low-pass intermediate matrix and one column of high-pass intermediate matrix in parallel such that the low-pass block of column-processor receive columns of low-pass intermediate matrix and the high-pass block receive columns of high-pass intermediate matrix. The low-pass block produces one column of each pair of sub-band matrices low-low and low-high, where the high-pass block produces one column of other two sub-bands high-low and high-high. The structure of low-pass block of lifting and flipping 2-D DWT are shown in Fig.11 and Fig. 12, where the structure of high-pass block of lifting and flipping 2-D DWT are shown in Fig.13 and Fig. 14. As shown in Fig.13 and Fig14, both the low-pass and high-pass blocks of lifting and flipping 2-D DWT are identical except the scaling constants. Both the low-pass and high-pass block of lifting 2-D DWT involves *M*/2 multipliers each for scaling the sub-band components while the low-pass and high-pass block of flipping 2-D DWT involves *M* multipliers each for the same operation. Therefore, the full-parallel lifting 2-D DWT structure involves *M* less multipliers than the flipping 2-D DWT structure. Parallel structure for block size *P* < 2*M* (full-parallel structure) also can be derived similar to the proposed full-parallel structure for both lifting and flipping 2-D DWT. In those cases, lifting 2-D DWT structure involves P/2 less multipliers than the flipping 2-D DWT structure. Since, critical-path of lifting cell is marginally higher than flipping cell, area-delay efficiency of lifting 2-D DWT structure would be better than flipping structure for higher block sizes.

Low-pass unit of column processor for lifting scheme require *M*/4 less multiplier than the flipping scheme of the scaling unit. Similarly high pass unit of lifting scheme require *M*/4 less multiplier over flipping scheme also (shown in Fig. 13 and 14). Therefore we have seen that the total number of multiplier saving in lifting scheme *M*/2 over flipping scheme.

**Table. 3** Comparison of Hardware and time complexity of proposed structure and existing lifting and flipping based 2-D DWT structures

hardware complexity table.emf

**6 Synthesis results**

We have coded proposed structures and the structure of [32] in VHDL for block sizes 16 and 32. We also coded the structure of [29] in VHDL. We have assumed 1-level decomposition of the input image of size (512×512) and synthesized all the designs without frame-buffer as the frame-buffer usually external to the chip due to its large size compared to the core. We have considered 8-bit pixel and 12-bit word length for intermediate and output signals. All the designs are synthesized in Synopsys Design Compiler using SAED90nm CMOS library [31]. Area, minimum clock period (MCP) and power reported by the Design Compiler are listed in Table 4 for comparison. Power is estimated at the MCP of respective designs.

**Table. 4** Synthesis results of lifting and flipping based existing and proposed DWT strictures

Results.emf

**LEGEND** : ADP: Area-delay-product, ADP = Core Area × MCP × CT, EPI: Energy per image, EPI = Core power × MCP × CT, CT: computation time = Image size/ Block size

As shown in Table 4, the structure of [29] has lowest MCP than other designs due to smaller critical path as given in the theoretical estimate of Table 3. The proposed lifting-based structure involves 12.67% and 11.7% less area than the proposed flipping-based structure for block size 16 and 32, respectively. This is mainly due to saving in multipliers in the lifting structure. Compared with the lifting structure of [32], the proposed lifting based structures involve 23.8% and 14.2% less area and flipping-based structure involve 8% and marginally less area for block size 16 and 32, respectively. Compared with the flipping structure of [29], the proposed lifting-based structure involves 1.5 and 2.2 times more area and offers 6.84 times and 13.6 times higher throughput, respectively. The proposed flipping-based structure involves 1.7 times and 2.4 times higher area than the structure of [29] and offers 7.15 times and 14.15 times higher throughput than other.

We have estimated area-delay product (ADP) (ADP= Area × MCP × Image-size / block-size) and energy per image (EPI) (EPI = Power × MCP × Image-size / block-size) of all the designs listed in Table 4. The comparison of ADP and EPI values are shown in Fig.15 in terms of bar-chart. As shown in Fig.15, the proposed lifting-based structure involves nearly 8% less ADP and 22.5% less EPI than the proposed flipping-based structure on average for blocks sizes 16 and 32. Compared with the structure of [32], the proposed lifting-based involve 24%, 29% less ADP, and 39%, 44% less EPI for block sizes 16 and 32, respectively. Similarly, the proposed flipping-based structure involve 16%, 14% less ADP and 3%, 22% less EPI than those of [32] for block sizes 16 and 32, respectively. Compared with the structure of [29], the proposed lifting-based structure involves 6.4 times less ADP and 3.8 time less EPI for block-sizes 32. For the same block-size, the proposed flipping-based structure involve 5.8 times less ADP and 2 time less EPI than those of [29].

**7 Conclusion**

In this paper, we made an analysis on the lifting and flipping DWT. We have derived full-parallel lifting-based and flipping-based 2-D DWT structures and shown that the lifting-based 1-level 2-D DWT full-parallel structure involves *M*/2 number of less multiplier than the similar flipping-based 2-D DWT structure. Compared with the structure of [32], the proposed lifting-based structure involves 29% less ADP, and 44% less EPI for block size 32, respectively. Compared with flipping-based structure of [29], the proposed lifting-based and flipping-based structures, respectively, involve 6.4 times, 5.8 times less ADP, and 3.8 time, 2 times less EPI for block-sizes 32. Therefore, flipping-scheme no longer gives an area-delay efficient structure when 2-D DWT implemented in parallel structures for higher block-sizes.

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