Implementation of Single Image Histogram Equalization on Zynq FPGA

**Abstract:** In present days, image processing is very much needed in different fields like medicine, acoustics, forensic sciences, agriculture and industrial applications. These image processing algorithms are most preferably implemented on Field Programmable Gate Arrays (FPGA’s) as they are reprogrammable to perform required operations. This paper describes the implementation of Histogram Equalization on Zynq FPGA which consists of ARM cortexA9 processor along with FPGA’s. To implement this, Intellectual property (IP) cores are generated in vivado High-Level Synthesis (HLS) tool to figure out and equalise the histogram. These IP cores are brought down to vivado to create the required hardware. Finally, the design was programmed into Zynq FPGA. The software application is developed using Software Development Kit (SDK). The results are obtained for an image size of 259x194. The utilization report showing that implemented design has taken less number of hardware resources as compared with the Kintex KC705 evaluation board. The processing time taken for execution is 9.288nsec.