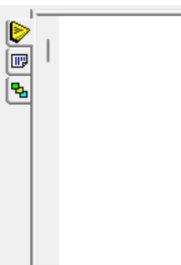


Codes:

Entity	Logic C
FLEX10KE: AUTO	
LabHW2	4 (4)



Tasks
Flow: Compilation

- Task 1: Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (General)
- Classic Timing Analysis
- EDA Netlist Writer
- Program Device (Open)

```

10  always @(w, y)
11  begin
12      case (y)
13      A:  if (w) Y = B;
14          else Y = A;
15      B:  if (w) Y = B;
16          else Y = C;
17      C:  if (w) Y = D;
18          else Y = A;
19      D:  if (w) Y = B;
20          else Y = C;
21
22      default: Y = 2'bxx;
23      endcase
24  end
25
26  always @(negedge resetn, posedge clk)
27  if(resetn == 0) Y <= A;
28  else Y <= Y;
29
30  assign z = (y==D);
31
32  endmodule
    
```

Messages

Type Message

Info: Command: quartus_eda --read_settings_files=off --write_settings_files=off LabHW2 -c LabHW2

Warning: Can't generate output files. Specify command-line options to generate output files, or update EDA tool settings using GUI or Tcl script.

Info: Quartus II EDA Netlist Writer was successful. 0 errors, 1 warning

Info: Quartus II Full Compilation was successful. 0 errors, 5 warnings

System (2) Processing (49) Extra Info Info (44) Warning (5) Critical Warning Error Suppressed (1) Flag /

Message: 0 of 142

Location:

Ln 12, Col 12

Locate

For Help press F1



Simulation:

