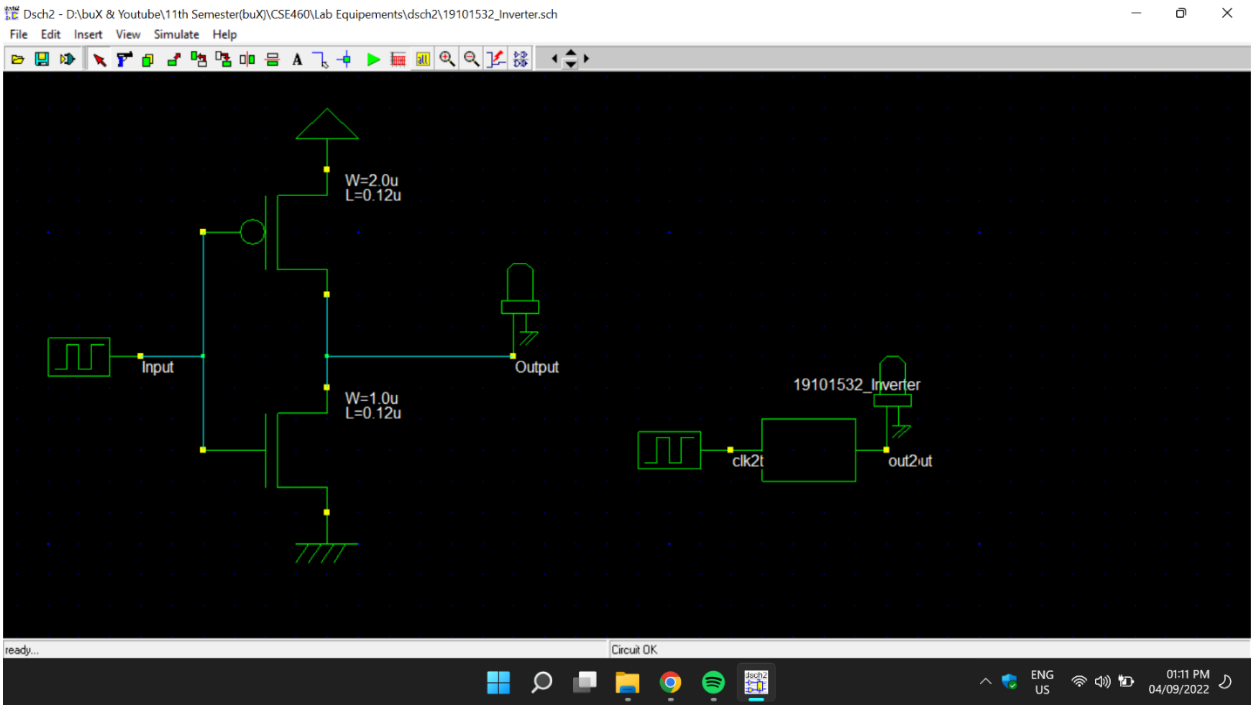
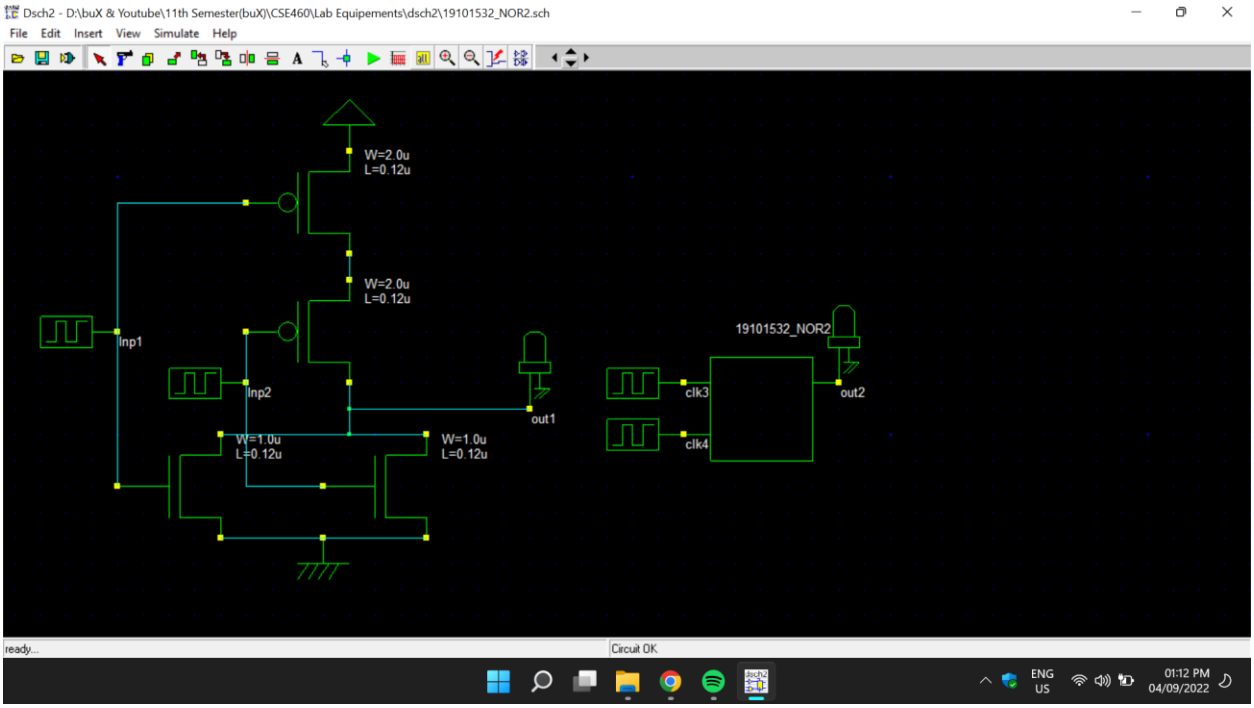
Assignment 3

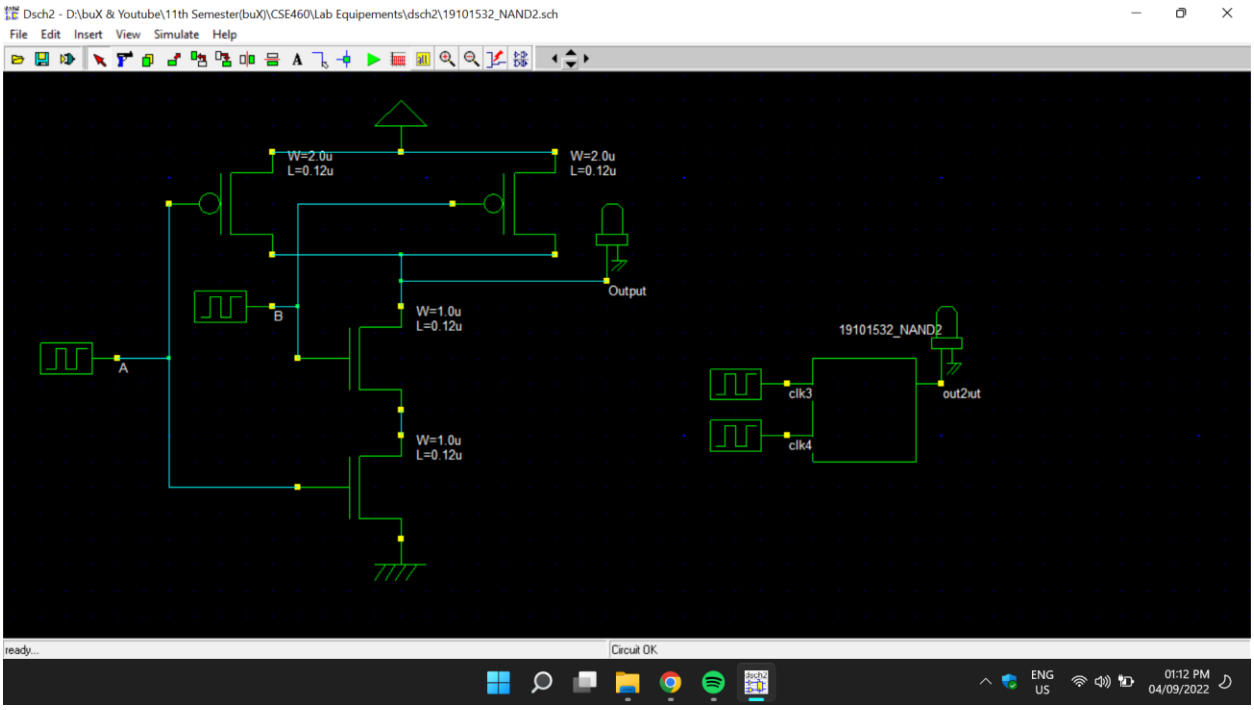
Inverter:



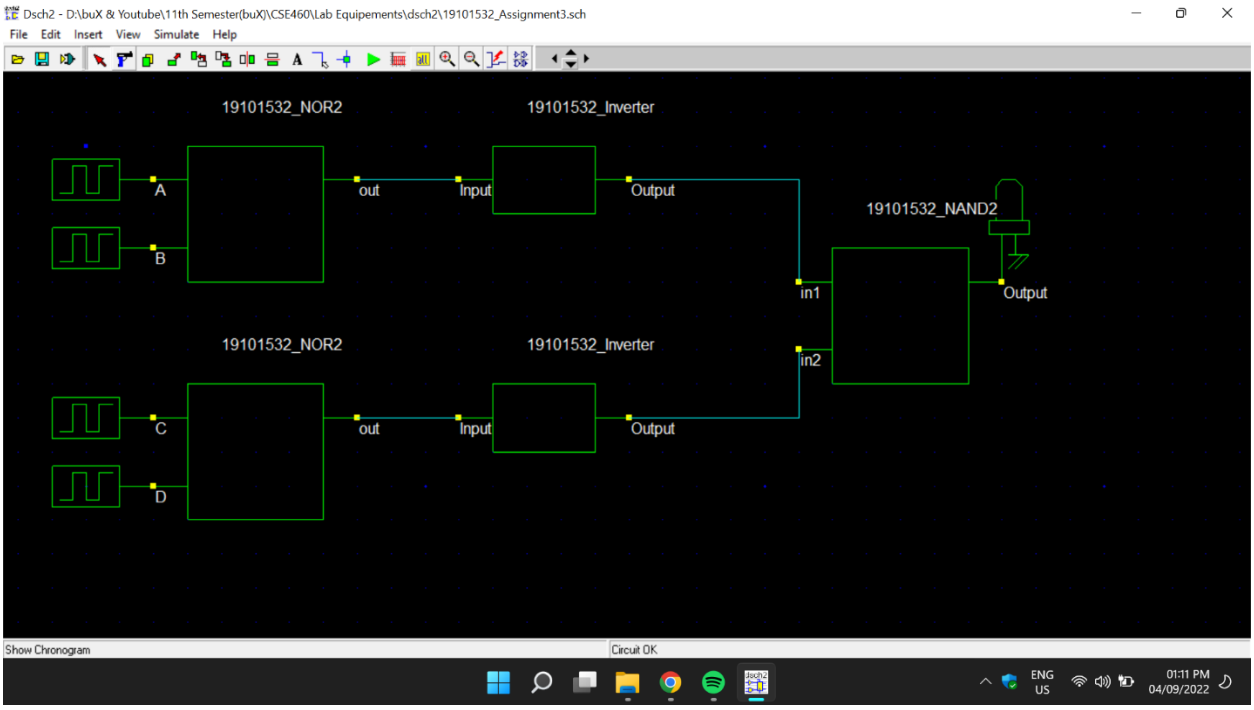
NOR2:



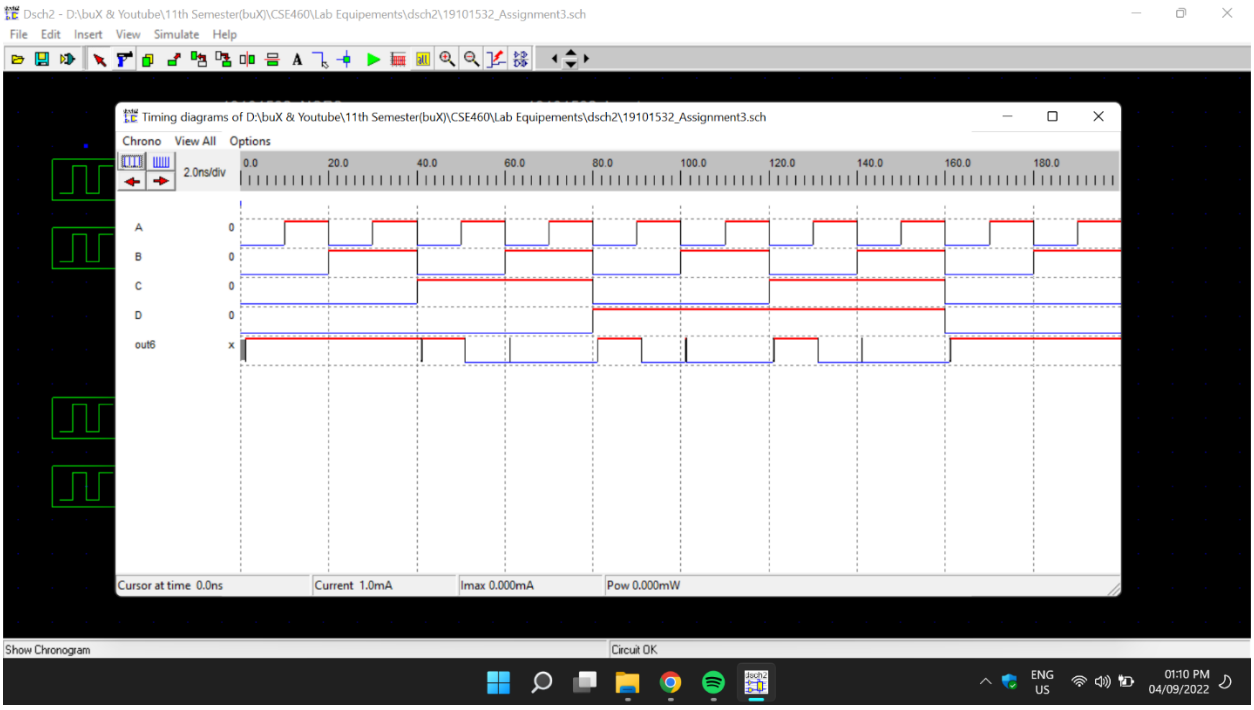
NAND2:


Dsch2 - D:\buX & Youtube\11th Semester(buX)\CSE460\Lab Equipements\dsch2\19101532_NAND2.sch
File Edit Insert View Simulate Help
W=2.0u
L=0.12u
W=2.0u
L=0.12u
Output
B
W=1.0u
L=0.12u
A
W=1.0u
L=0.12u
19101532_NAND2
clk3
clk4
out2ut
ready...
Circuit OK
ENG
US
01:12 PM
04/09/2022

~((A+B)(C+D)):

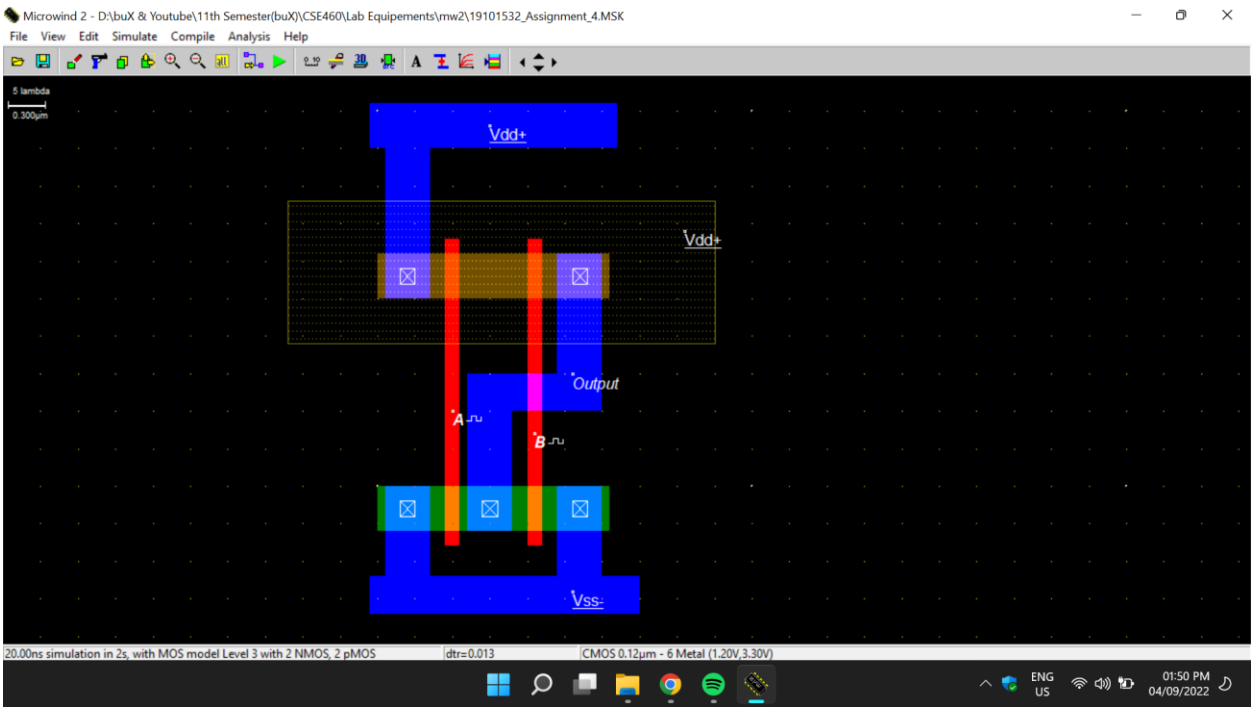

Dsch2 - D:\buX & Youtube\11th Semester(buX)\CSE460\Lab Equipements\dsch2\19101532_Assignment3.sch
File Edit Insert View Simulate Help
19101532_NOR2
19101532_Inverter
A
B
out
Input
Output
19101532_NAND2
in1
Output
19101532_NOR2
19101532_Inverter
in2
C
D
out
Input
Output
Show Chronogram
Circuit OK
ENG
US
01:11 PM
04/09/2022

Timing Diagram:



Assignment 4

Layout Design:



Waveform: