

EE537 Circuit Simulation Lab

Experiment 8

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September 24, 2024

1 Design of an inverting amplifier using a two stage OTA

Target Specifications:

Spec.	Value
Midband gain	20 dB
Bandwidth	> 1 MHz
Input capacitance	1 pF
Load capacitance	10 pF
Slew rate	$\geq 10 V/\mu s$
Gain error	0.1 %
Phase margin	$\geq 65^\circ$
Operating temperature range	0 °C to 70 °C

Figure 1: Target Specifications

1.1 Implement the 2 stage using a miller compensated 2 stage OTA. Show the calculations used for all the specifications and detailed design procedure.

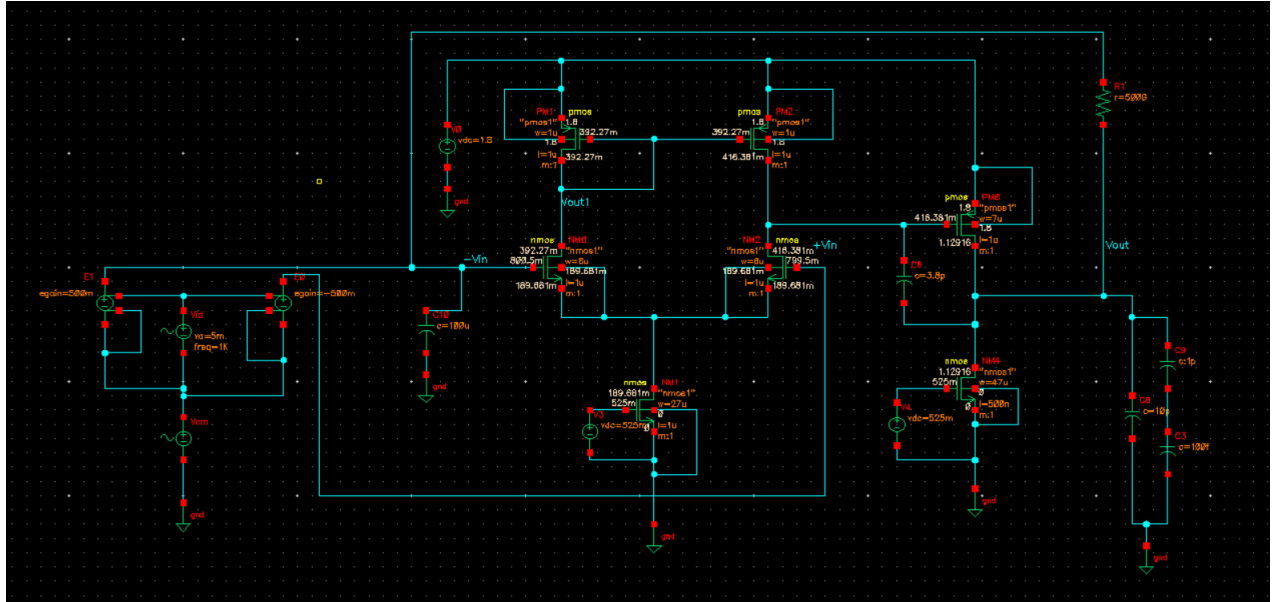


Figure 2: Two Stage OTA

Design :

$$\left| \frac{V_o}{V_i} \right| = \left| \frac{C_1}{C_2} \right|$$

$$20dB = 20\log[C_1/C_2]$$

$$\begin{aligned}
&\mathbf{C1=1pF} \\
&\mathbf{CL=10pF} \\
&1 = \log[1pF/C2] \\
&1 = -12 - \log[C2] \\
&\log[C2] = -13 \\
&\mathbf{C2=0.1pF} \\
&\mathbf{CL'} = \mathbf{CL} + \frac{C1C2}{(C1+C2)} \\
&\mathbf{CL'} = 10p + .1p/1.1p} \\
&\mathbf{CL' = 10.09p} \\
&\frac{V_o}{V_i} = \frac{Aoc(1-s/p_z)}{(1+s/p_1)(1+s/p_2)} \\
&\mathbf{PM} = 180 - \arctan(W_u/p_z) - \arctan(W_u/p_1) - \arctan(W_u/p_2) \\
&p_z = 10W_u \\
&p_z = gm_2/C_c \\
&W_u = gm_1/C_c \\
&p_2 = gm_2/C_L \\
&65 = 180 - 90 - 5.71 - \arctan(W_u/p_2) \\
&\arctan(W_u/p_2) = 19.29 \\
&p_2 = 2.9W_u \\
&C_c = 0.29C_L \\
&C_c = 2.93pF \\
&SR = \frac{I_5}{C_c} \\
&I_5 = SR * C_c = 29.3u \\
&I_1 = I_2 = I_5/2 = 14.65u \\
&SR = \frac{(I_6)}{(C_c+C_L)} \\
&I_6 = (C_c + C_L) * SR = 130u = I_7 \\
&UGB = A_{LO} * W_p = W_u \\
&W_u = \frac{gm_1}{C_c} * \frac{C2}{(C1+C2)} \\
&gm1 = 0.203m \\
&gm1 = gm7 \\
&(W/L)_{12} = gm_1^2/K' * 2 * I_1 = 4.7u = 5u \\
&(W/L)_7 = gm_7^2/K' * 2 * I_7 = 2.6u = 3u \\
&(W/L)_{34} = (W/L)_7 * (I_3/I_7) = 0.6u = 1u \\
&(W/L)_6 = (W/L)_5 * (I_6/I_5) = 88u
\end{aligned}$$

1.2 Show all the plots required to verify the achieved specifications.

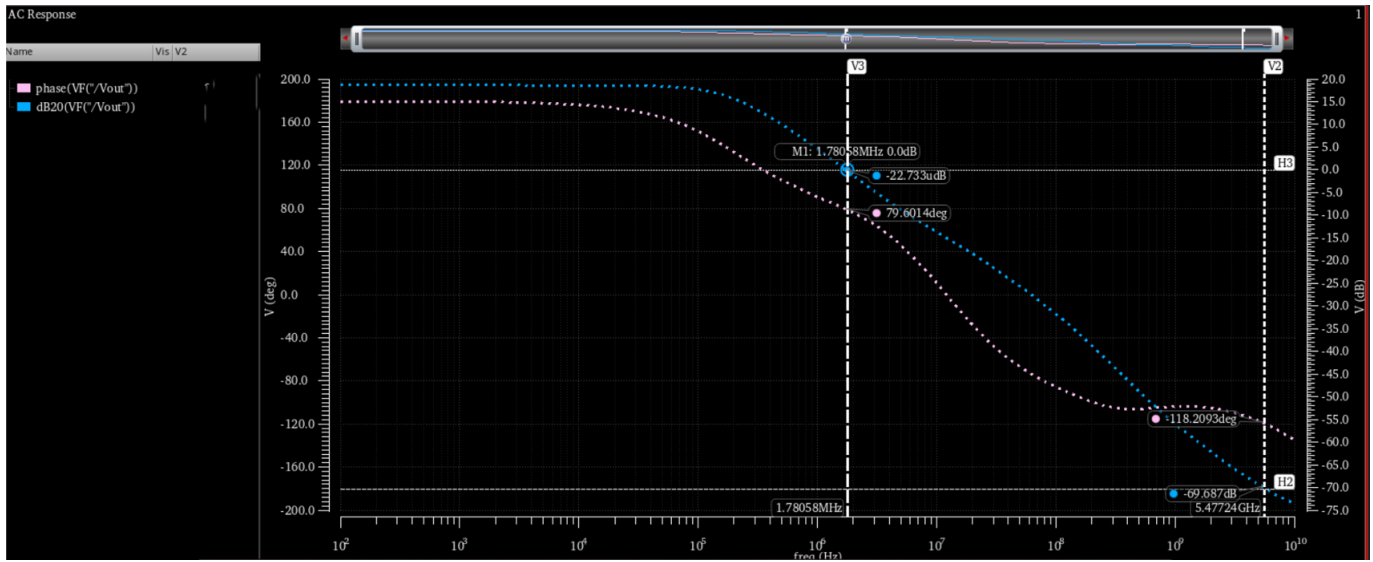


Figure 3: AC Magnitude v/s Phase plot