EE663: Frequency Synthesizers, Clock and Data Recovery Circuits

Course Project

Name: Shamini P R
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Objective: Design a phase-locked loop (PLL) that meets the given criteria, including all sub- blocks (phase frequency detector, voltage-controlled oscillator, loop filters, and divider) using Verilog models and transistor level in Cadence design suit.

1 Design Criteria

Table 1: Design Criteria

Total Capacitance	$\leq 25pF$
Total Power Dissipation	$\leq 15mW$
Charge Pump Current	$\leq 100A$

2 Target Specification

Table 2: Target Specification

Reference Frequency	1.50e+8
Output Frequency	2.40e+9
Divider	16

3 Introduction

A phase-locked loop (PLL) is a circuit designed to align the output signal of an oscillator with a reference or input signal, ensuring synchronization in both frequency and phase within a given system. When in a synchronized or locked state, the phase error between the output signal of the oscillator and the reference signal is either zero or remains constant. If any phase error accumulates, a control mechanism intervenes to minimize it by adjusting the oscillator.

3.1 Schematic Circuit Diagram of PLL

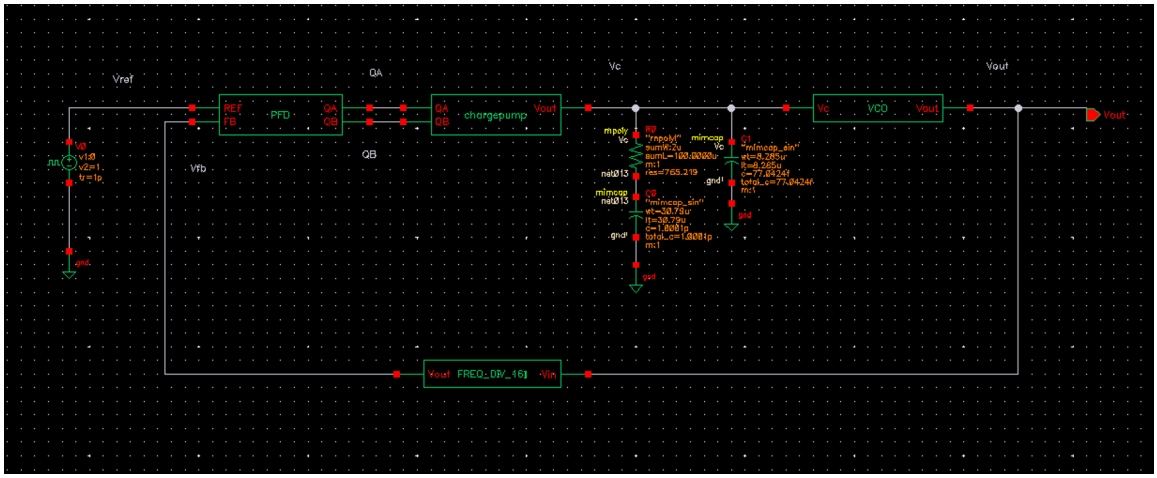

Figure 1: Schematic Circuit Diagram of PLL

Simultion result of PLL meeting Target frequency requirement of 2.40e+9 .

3.2 Simulation Result of PLL Output

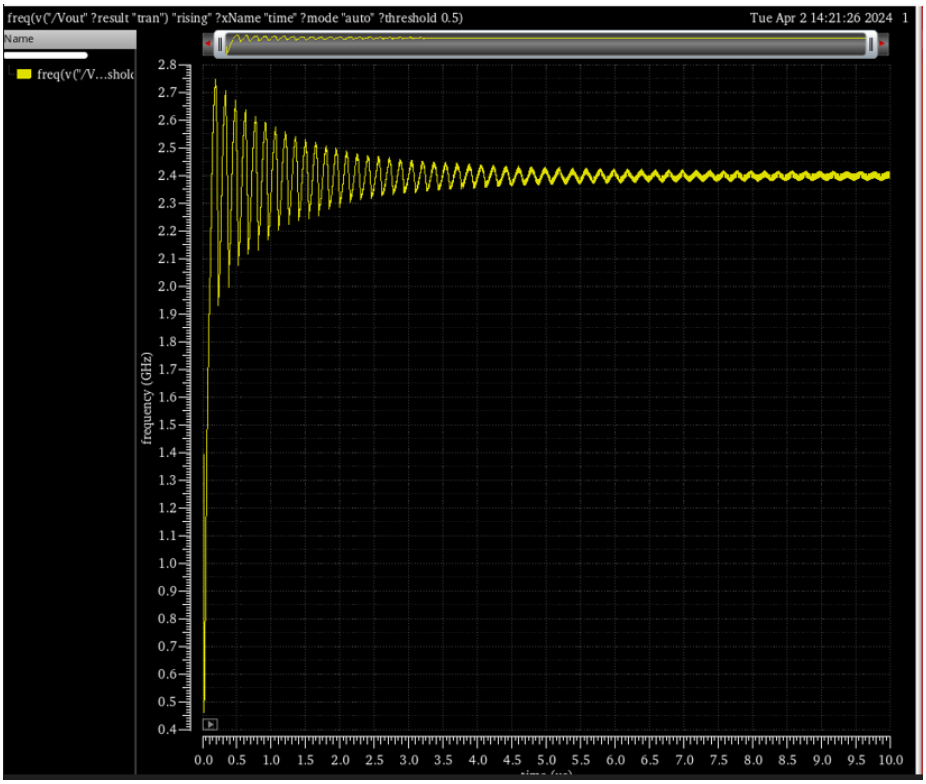

Figure 2: Simulated Plot of PLL Output

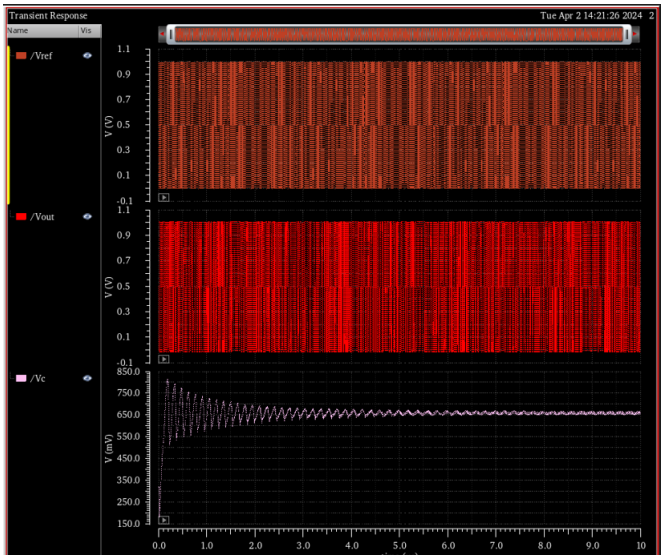

Figure 3: Plot of Vref,Vout,Vcontrol of PLL

The above plot shown the Referance signal if frequency (1.5e+8Hz),Output signal of Target frequency (2.4GHz) and Vcontrol voltage of 660mV.

4 Design of Phase Frequency Detector (PFD)

In a PLL system, the phase-frequency detector plays a critical role by comparing the phases of the reference signal and the feedback signal. This detector translates any phase difference into a voltage or current signal, which then undergoes processing through a Low-Pass Filter (LPF). Subsequently, this filtered signal is converted into the phase control signal for the Voltage-Controlled Oscillator (VCO).

4.1 Schematic Circuit Diagram

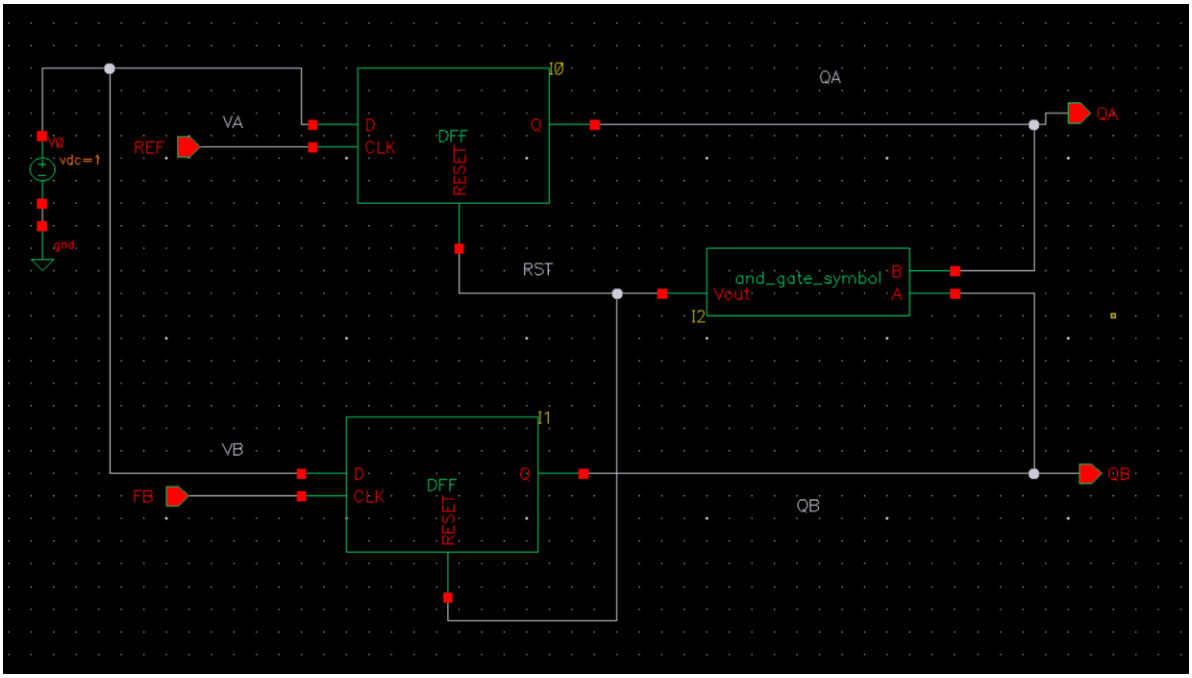

Figure 4: Schematic diagram of PFD

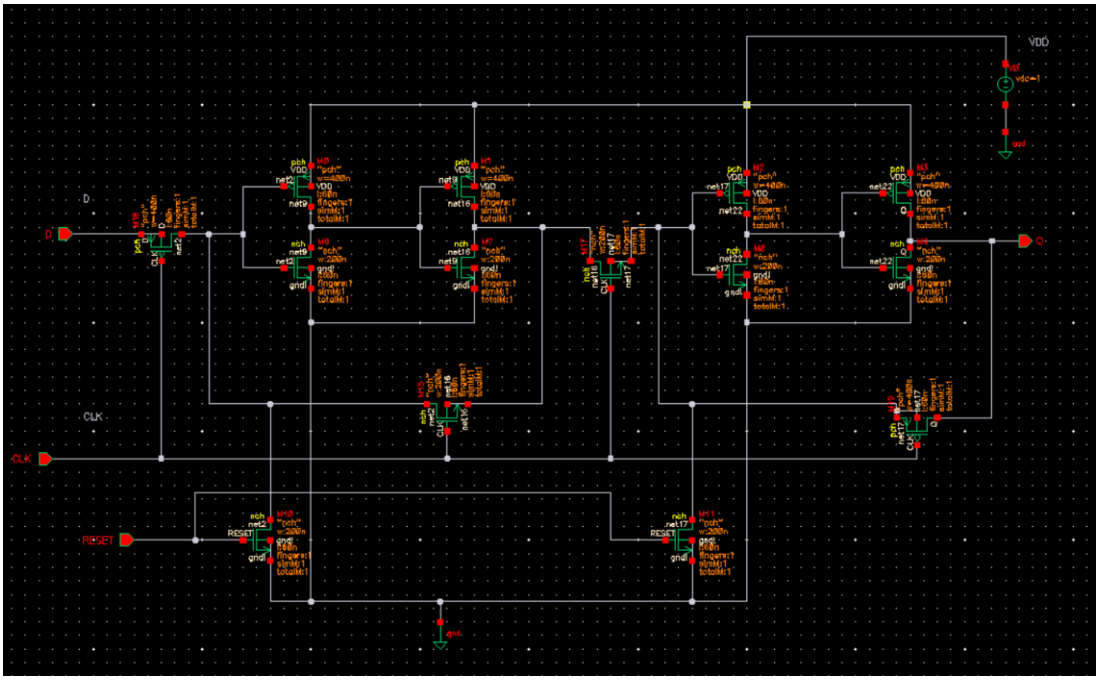

Figure 5: Schematic diagram of D Flip Flop with reset pin used in PFD ciruit.

4.2 Analysis

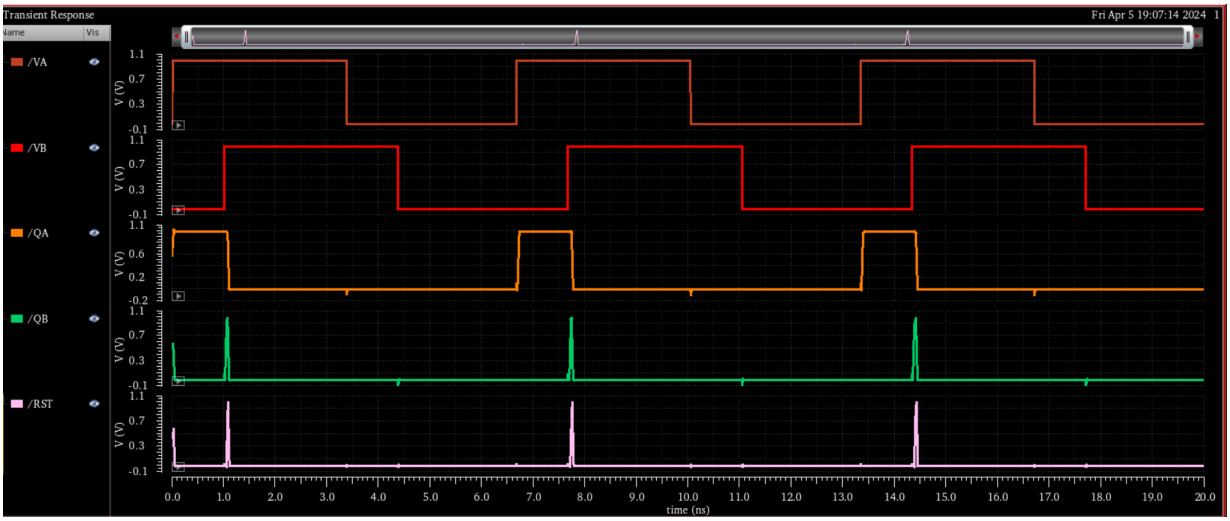

Figure 6: Simulated Plot of PFD output.

5 Design of the Charge Pump and Loop Filter

The charge pump comprises two switches accompanied by two symmetrical current sources. These sources are connected, one each, to positive and negative power supplies. The switches change their states in response to the UP and DN signals. The resultant output from the low-pass filter (LPF), modulated by the UP and DN signals, serves as the control signal for the Voltage-Controlled Oscillator (VCO).

5.1 Schematic Circuit Diagram

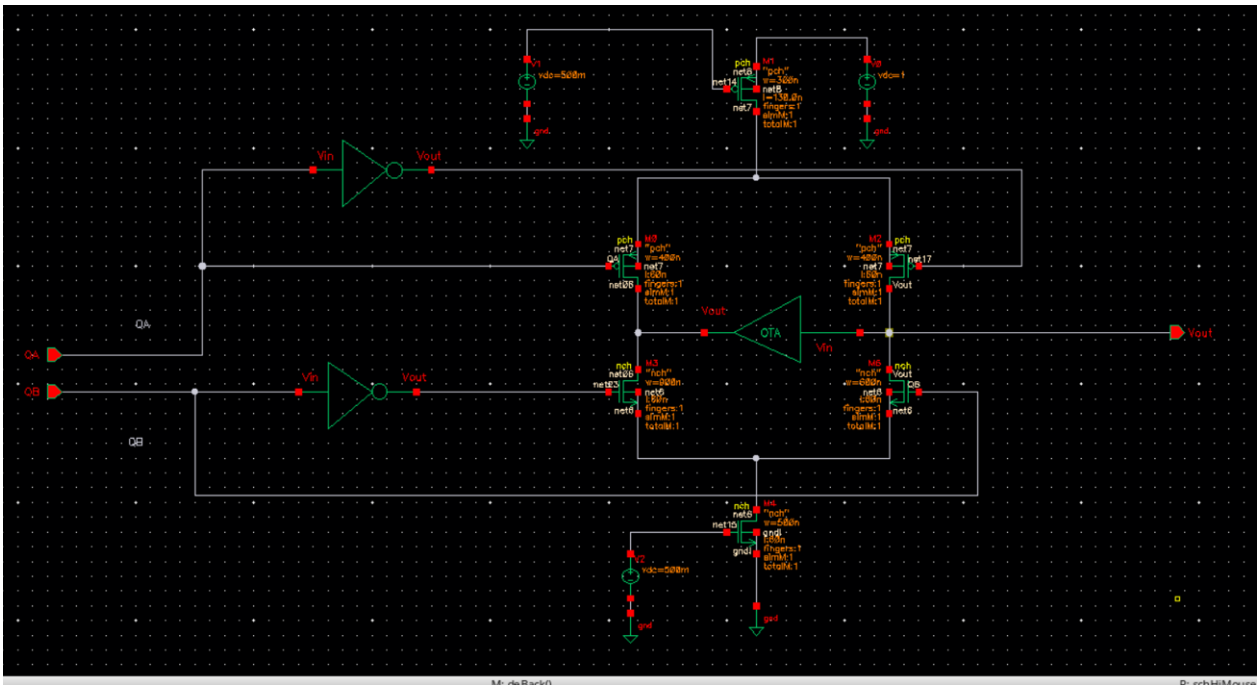

Figure 7: Schematic diagram of Charge Pump

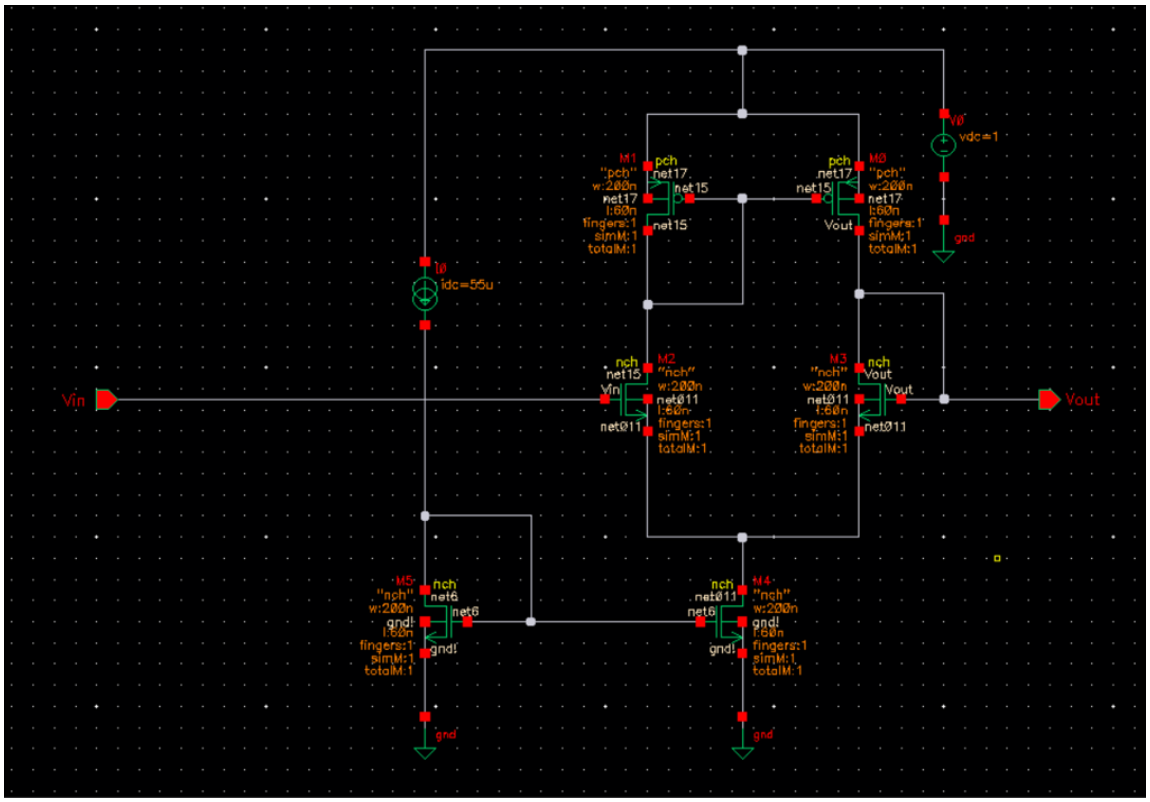

Figure 8: Schematic diagram of OTA used in charge pump

5.2 Analysis

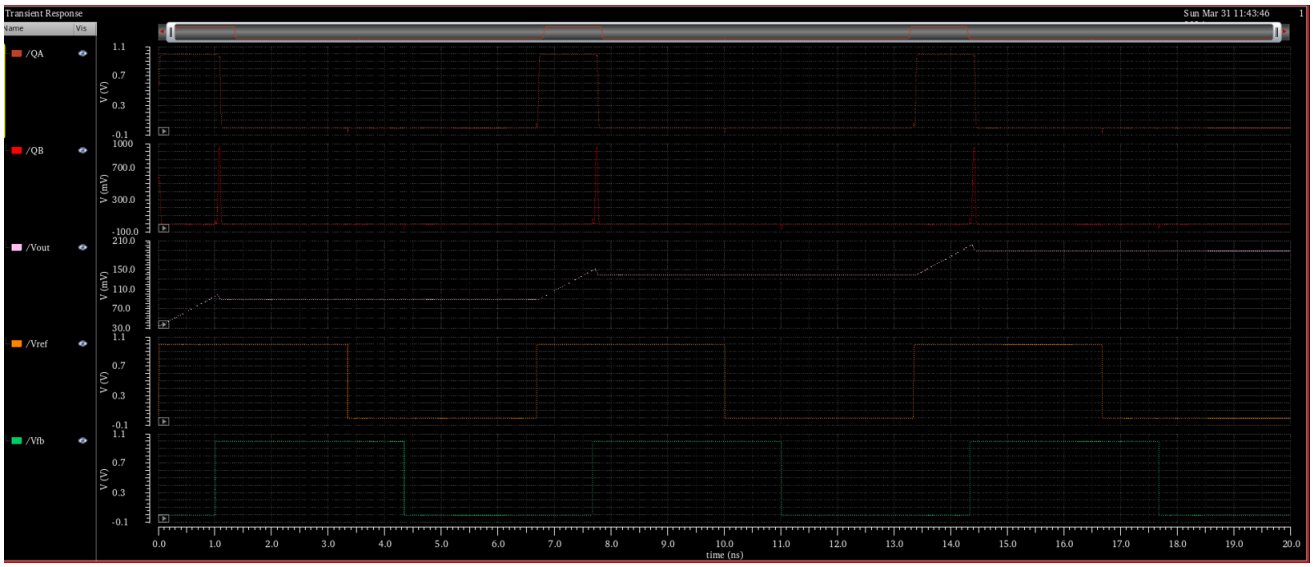

Figure 9: Simulated Plot of Charge pump Output

5.3 Schematic Circuit Diagram of Loop Filter

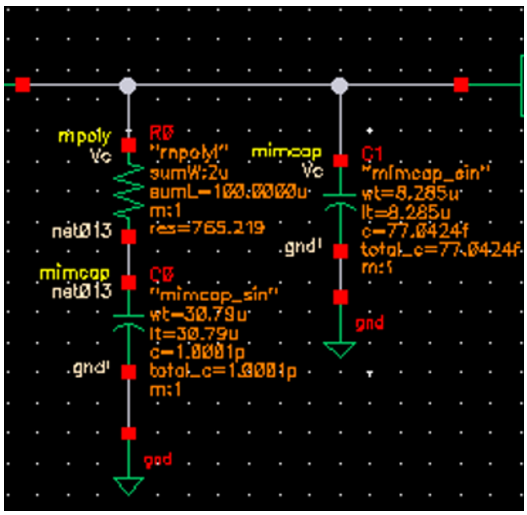

Figure 10: Schematic diagram of Loop Filter

6 Design of Voltage Controlled Oscillator (VCO)

VCOs plays an important role in the PLL circuit design. The fundamental principle underlying VCOs is to produce clock signals with required oscillations meeting the Barkhausen criteria. As per these criteria, the VCO's transfer function achieves unity magnitude at the oscillation frequency, with a phase of -180 degrees.Here a ring oscillator is used with 5 invertors connected together to acheive the required criteria. To get an pulse signal at output two invertors are connected in series and from there output is taken.

6.1 Schematic Circuit Diagram

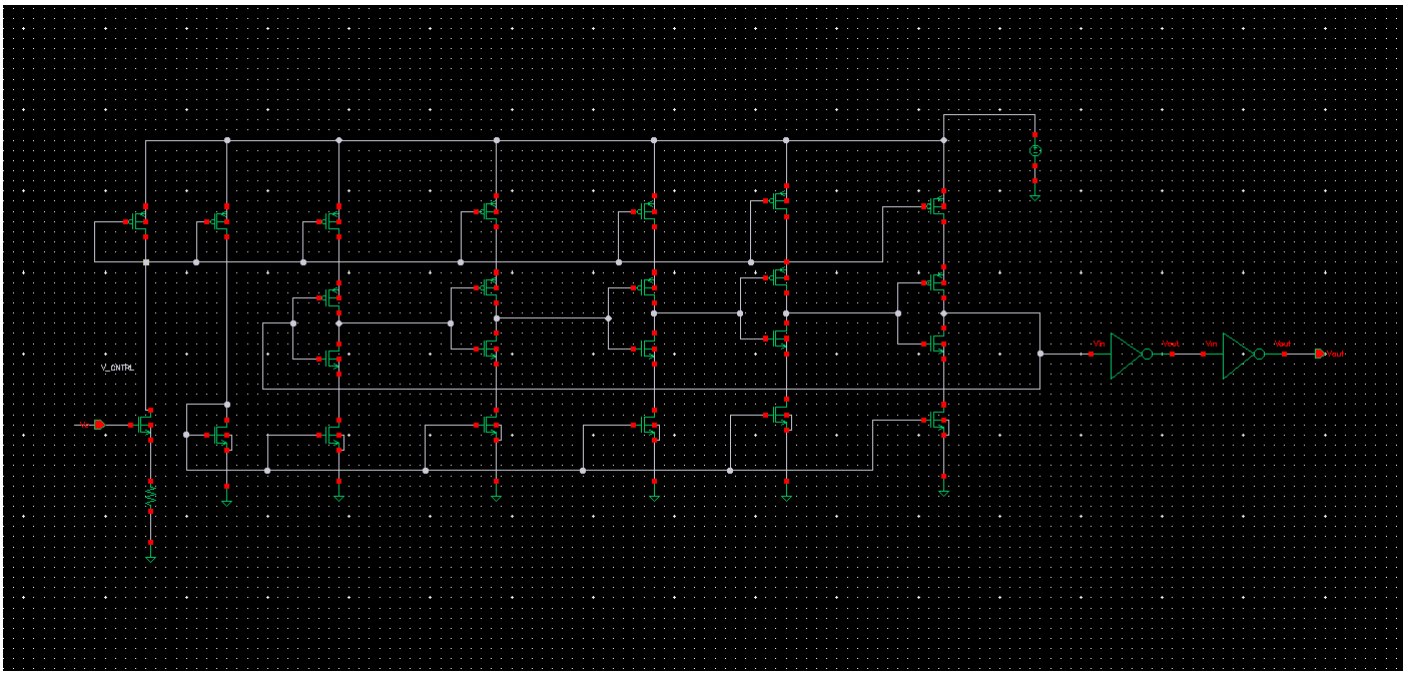

Figure 11: Schematic Circuit Diagram of VCO

6.2 Analysis

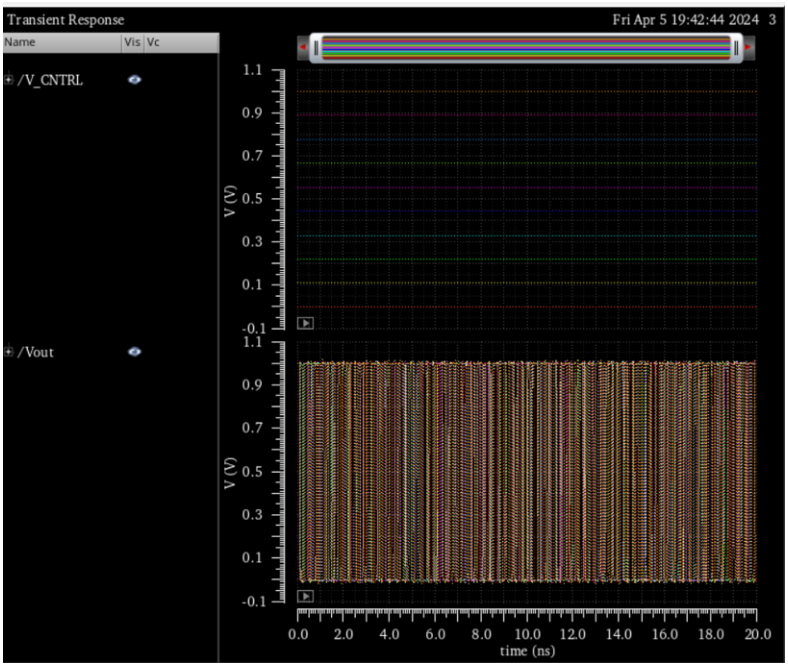

Figure 12: Plot of VCO output

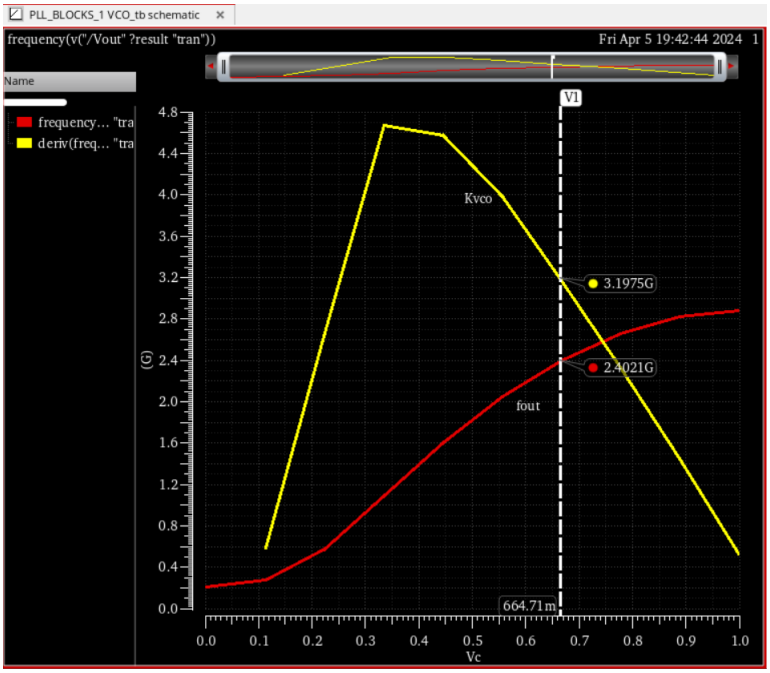

Figure 13: Plot of Output frequency and K_{VCO}

7 Design of Frequency Divider

Phase-locked loop circuit make use of frequency dividers to generate a feed back frequency that is a multiple of a reference frequency. Given target frequency division is N=16,this is acheived by connecting in series four frequency divider circuit with N=2(frequency division/2) .

7.1 Schematic Circuit Diagram

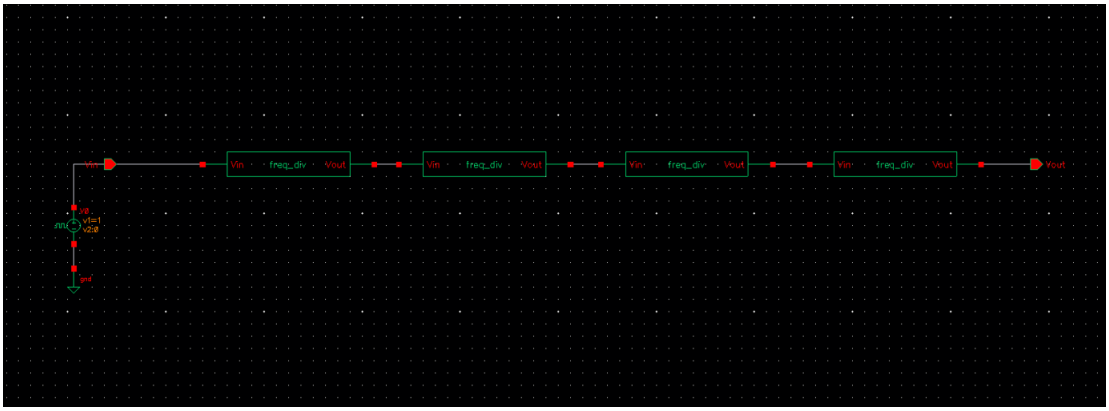

Figure 14: Schematic Circuit Diagram of frequency divider

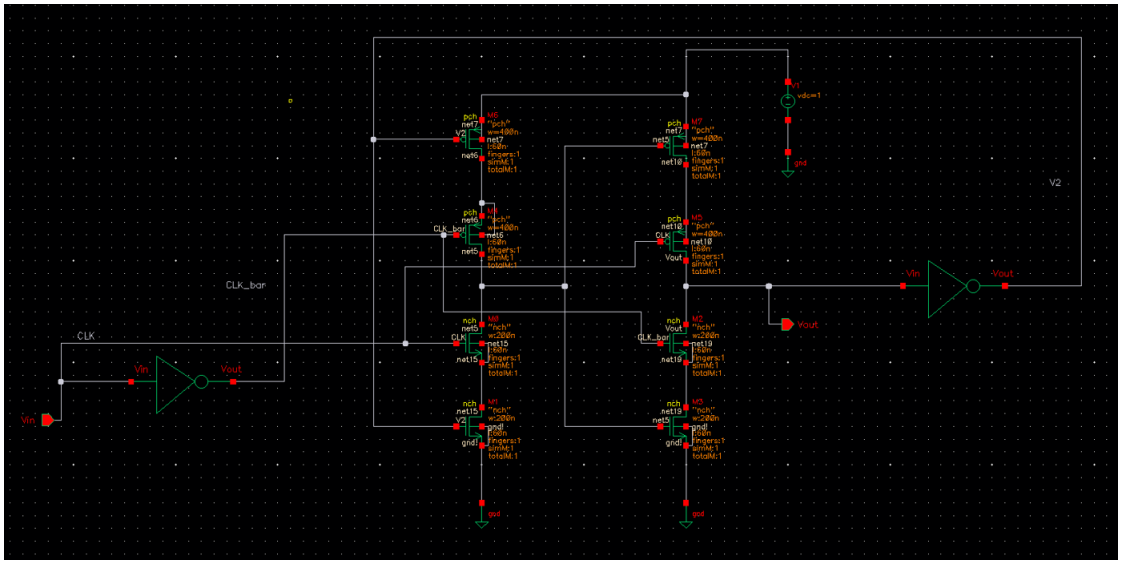

Figure 15: Schematic Circuit Diagram of each block of frequency divider

7.2 Analysis

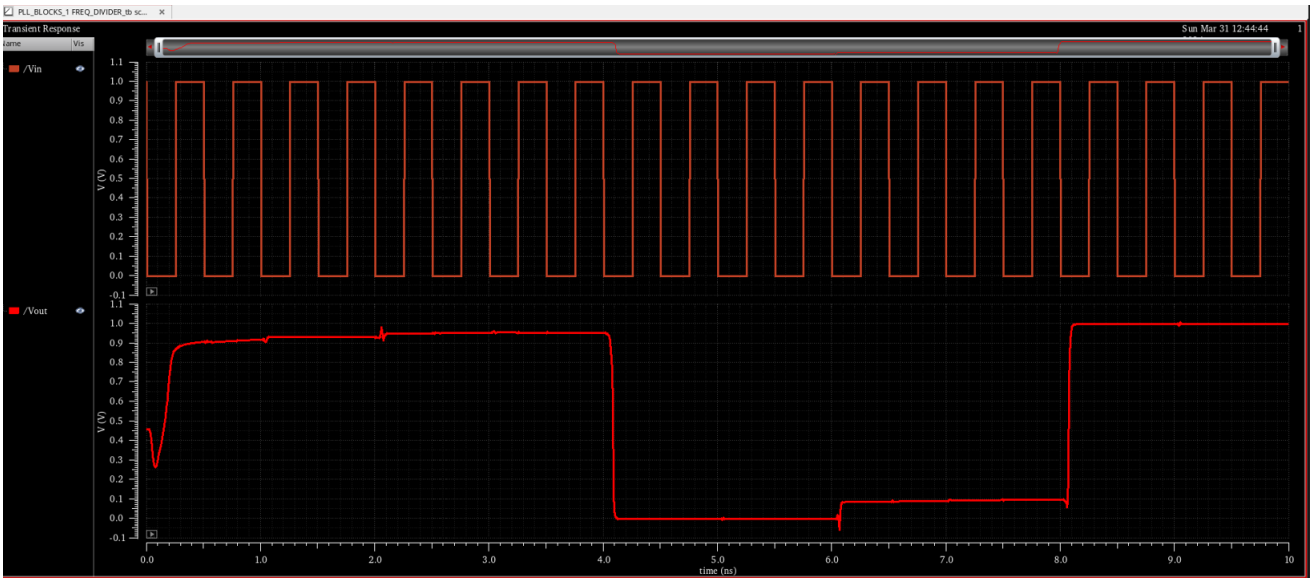

Figure 16: Simulated plot of frequency divider output (N=16)

8 Conclusion

In conclusion,A phase-locked loop (PLL) meeting the target frequency criteria of 2.4GHz is designed and implemented using TSMC 65nm tehnology node library in Cadence Design Suite . Each sub-block of PLL, including the Phase Frequency Detector(PFD), Voltage-Controlled Oscillator, Loop Filters,Charge Pump and Frequency divider, has been designed at transistor level and integrated together to form the PLL circuit.Through this project a better understanding of the PLL circuit and each of its components and its behaviour is achieved.

9 References

1. P. K. Hanumolu, M. Brownlee, K. Mayaram and Un-Ku Moon, "Analysis of charge-pump phase-locked loops," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 51, no. 9, pp. 1665-1674, Sept. 2004, doi: 10.1109/TCSI.2004.834516.

2 Behzad Razavi, "Design of CMOS Phase-Locked Loops: From Circuit Level to Architecture Level" , Cambridge University Press, 2020.