EE532: Device Simulation Lab
Project

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Entry No: 2023EEM1025 & 2023EEM1029 **April 24, 2024**

Experiment Name:High Performance UTBB FDSOI Devices Featuring 20nm Gate Length for 14nm Node and Beyond

1 Design parameters for PFET FDSOI:

Table 1: Design parameters PFET FDSOI

Parameters	Type
Channel	Silicon
Source & Drain (For PFET FDSOI)	SiGe
Gate Length (L_G)	20 nm
BOX thickness (T_{box})	25nm
Source & Drain doping	Boron
Source & Drain doping concentration	$1 \times 10^{21}/cm^3$
Channel thickness(T_{Si})	6nm
Gate material	Titanium Nitride
Back gate material	Silicon
Back gate doping	$1 \times 10^{18}/cm^3$
Spacer material	Si_3N_4
Metal workfunction of Titanium Nitride	4.5 eV
BOX material	SiO_2
Gate oxide material	SiO_2
High-K oxide	HfO_2

Table 2: Physics models for UTBB FDSOI

Parameters	Value
Mobility models	Mobility (Doping Dependence High field saturation)
Band gap and Band gap narrowing	Effective intrinsic density (no band gap narrowing)
Temperature(K)	300K
Recombination	SRH (DopingDep Temperature)
Fermi Level	Fermi
Area factor	1e3
Physics material	SiGe MoleFraction (xFraction=0.5)

2 Device structure

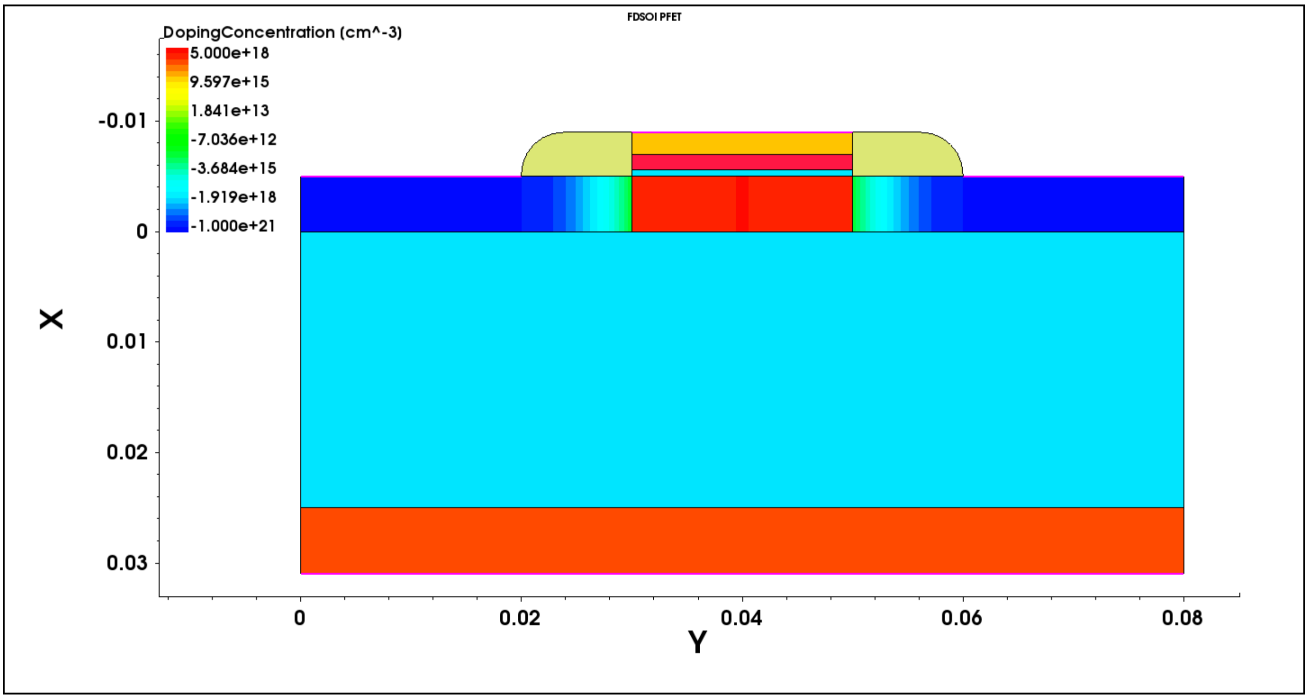

Figure 1: FDSOI PFET Device structure

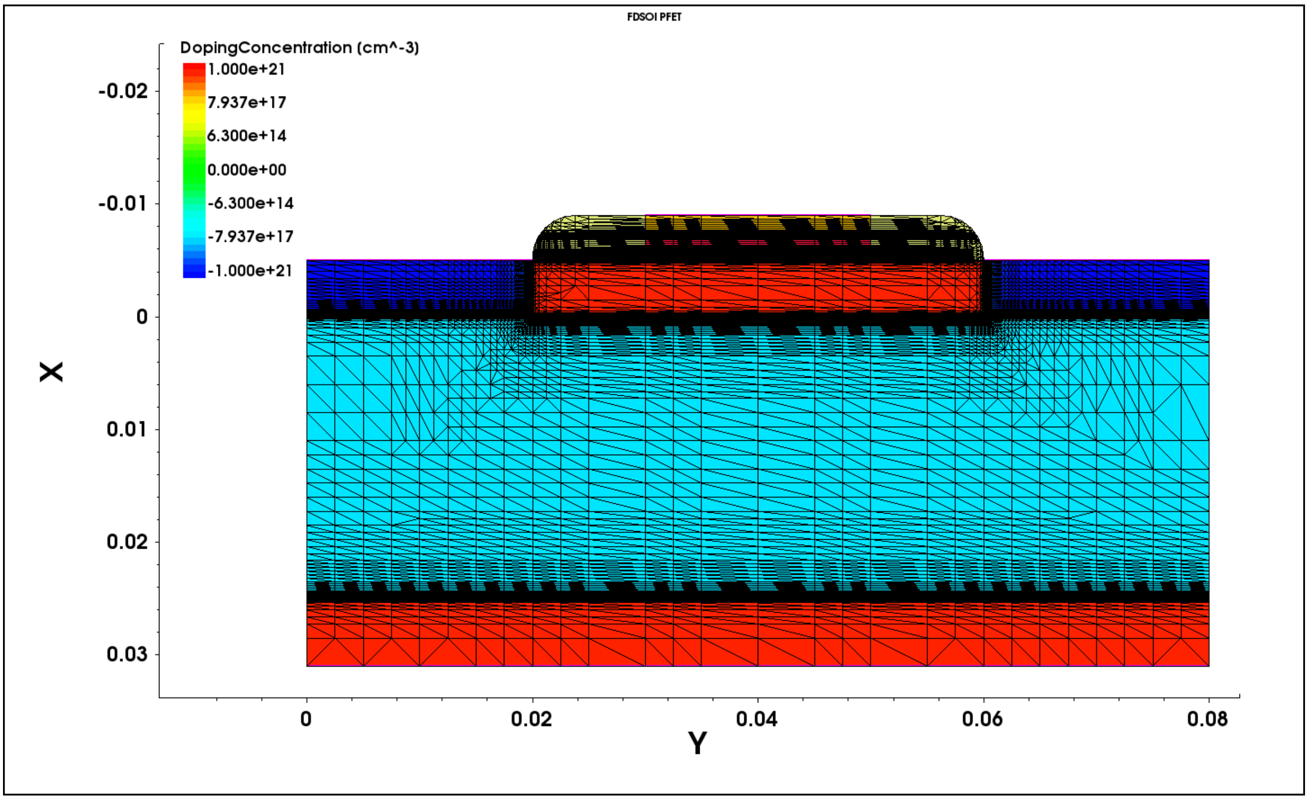

Figure 2: FDSOI PFET Device structure with meshing

3 Simulated Device physics models

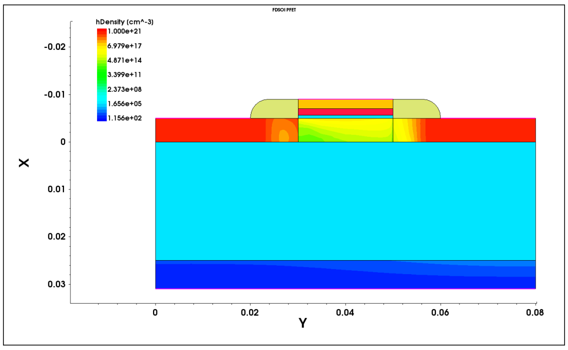

Figure 3: PFET FDSOI hole density

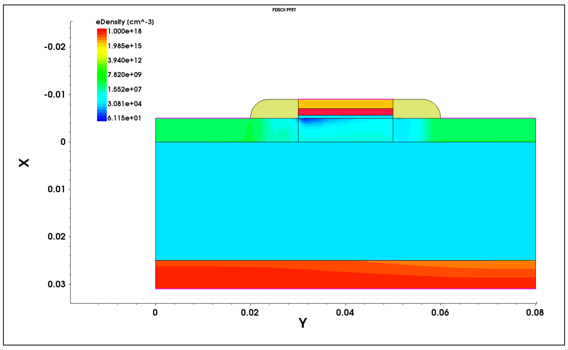

Figure 4: PFET FDSOI electron density

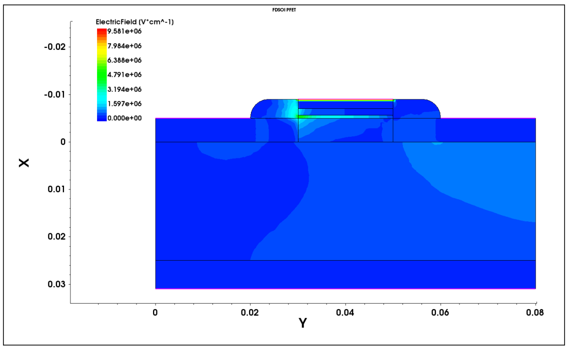

Figure 5: PFET FDSOI electric field

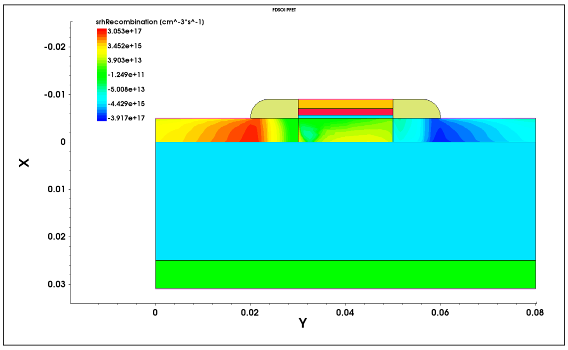

Figure 6: PFET FDSOI srh recombination

Above Simulated Device physics models shown basically shows the PFET FDSOI hole density plot.Here, the source and drain has doping of SiGe in P-type doping so the colour is red. The back gate Silicon Substrate is $N-type$ so the colour is blue. Also, The channel has colour of yellow because of fully depleted region due to inversion layer formation due to both front and back gate biasing in positive value.
Above Simulated Device physics models shown basically shows the PFET FDSOI electron density plot.Here, the colour is basically opposite of hole density as shown.Similarly, the device simulated physics model of electric field and SRH recombination is also shown up.

4 Design parameters for NFET FDSOI:

Table 3: Design parameters

Parameters	Type
Channel	Silicon
Source & Drain (For NFET FDSOI)	SiC
Gate Length (L_G)	20 nm
BOX thickness (T_{box})	25nm
Source & Drain doping	Boron
Source & Drain doping concentration	$1 \times 10^{21}/cm^3$
Channel thickness(T_{Si})	6nm
Gate material	Titanium Nitride
Back gate material	Silicon
Back gate doping	$1 \times 10^{18}/cm^3$
Spacer material	Si_3N_4
Metal workfunction of Titanium Nitride	4.5 eV
BOX material	SiO_2
Gate oxide material	SiO_2
High-K oxide	HfO_2

Table 4: Physics models

Parameters	Value
Mobility models	Mobility (Doping Dependence High field saturation)
Band gap and Band gap narrowing	Effective intrinsic density (no band gap narrowing)
Temperature(K)	300K
Recombination	SRH (DopingDep Temperature)
Fermi Level	Fermi
Area factor	1e3
Physics material	SiGe MoleFraction (xFraction=0.5)

5 Device structure NFET FDSOI

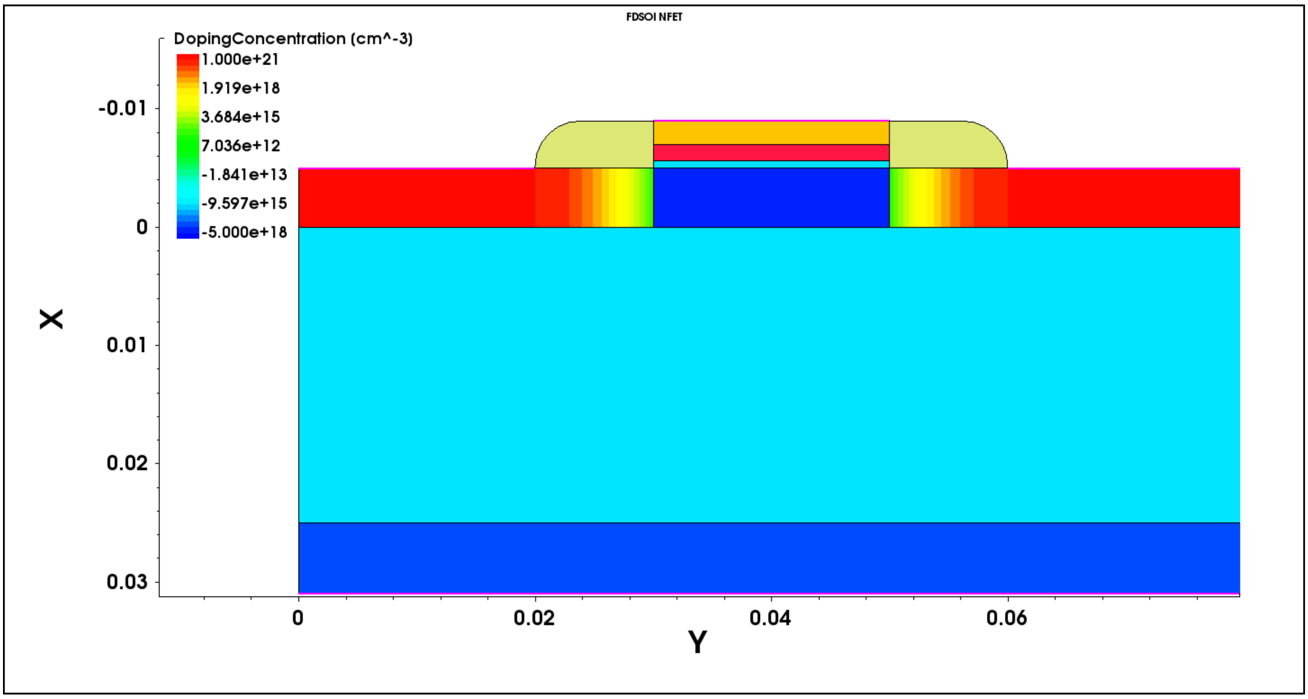

Figure 7: FDSOI NFET Device structure

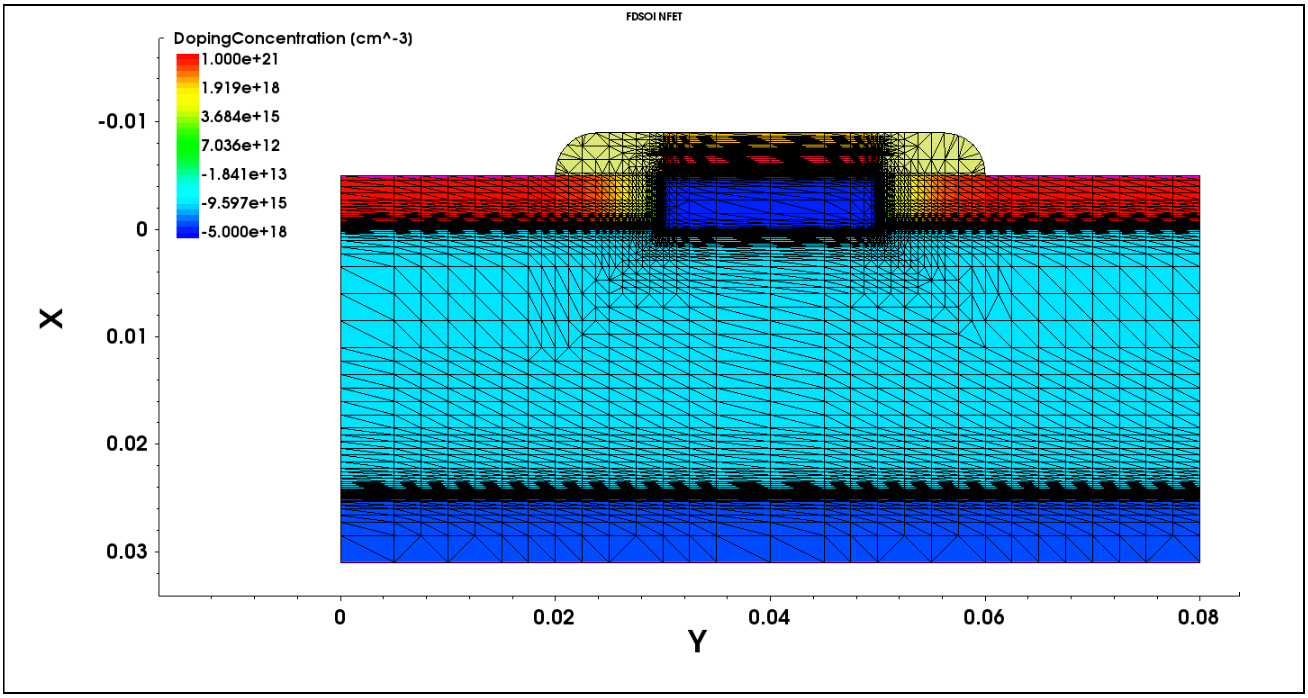

Figure 8: FDSOI NFET Device structure with meshing

6 Simulated Device physics models

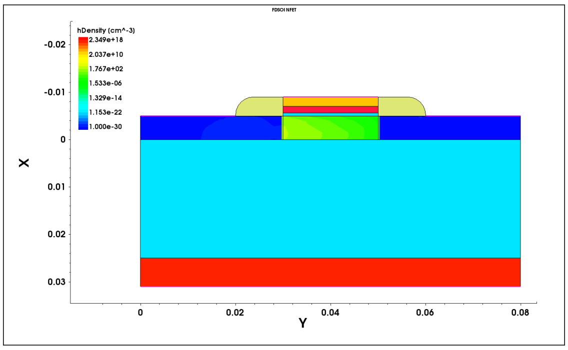

Figure 9: NFET FDSOI hole density

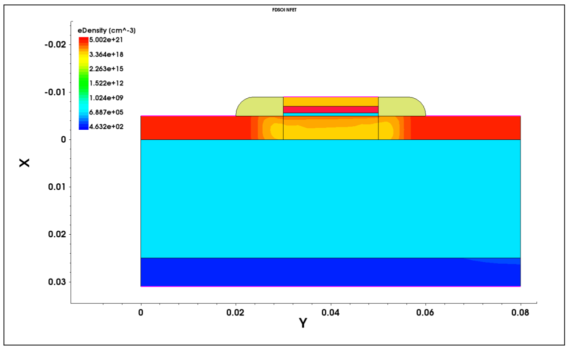

Figure 10: NFET FDSOI electron density

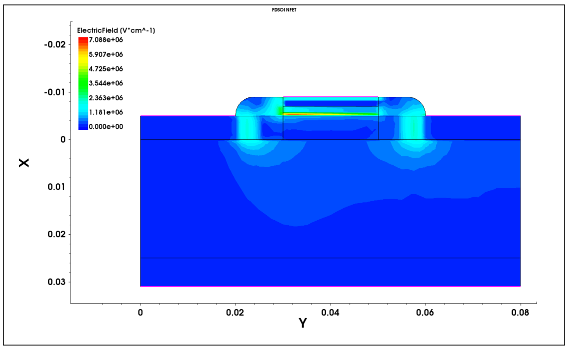

Figure 11: NFET FDSOI electric field

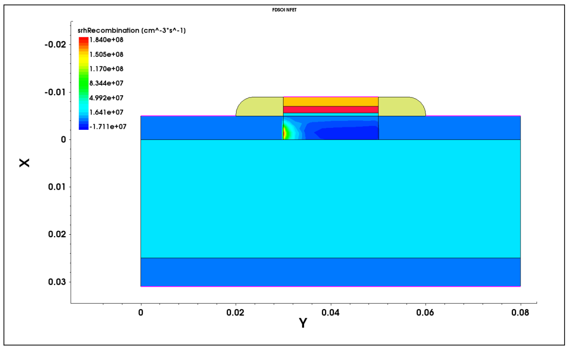

Figure 12: NFET FDSOI srh recombination

Above Simulated Device physics models shown basically shows the NFET FDSOI hole density plot.Here, the source and drain has doping of SiC in N-type doping so the colour is blue. The back gate Silicon Substrate is $P-type$ so the colour is red. Also, The channel has colour of yellow because of fully depleted region due to inversion layer formation due to both front and back gate biasing in positive value.
Above Simulated Device physics models shown basically shows the PFET FDSOI electron density plot.Here, the colour is basically opposite of hole density as shown.Similarly, the device simulated physics model of electric field and SRH recombination is also shown up.

7 Theoretical Calculation

7.1 Calculation of effective oxide thickness (EOT):

As we know, Effective oxide thickness (EOT) is the effective thickness of oxide for a combination of SiO_2 and HfO_2 which is present in both NFET and PFET FDSOI shown in this project.
The Formula for EOT can be written as :-

$$EOT = t_{SiO2} + (\frac{\varepsilon_{SiO2}}{\varepsilon_{Hfo2}}) \times t_{Hfo2} \tag{1}$$

Where:

Substituting values of table 5 ,we get:

$$t_{SiO2} = 1.4nm \tag{2}$$

Table 5: Known values for EOT equation

Parameters	Value
Silicon dioxide thickness (t_{SiO2})	0.6nm
Relative permittivity of Silicon dioxide (ε_{SiO2})	3.9
Relative permittivity of Hafnium dioxide(ε_{HfO2})	22
EOT	0.9nm

7.2 Calculation of Oxide capacitance, C_{ox}:

$$C_{ox} = \frac{\varepsilon_{ox}}{EOT} \tag{3}$$

On calculation , we get:

$$C_{ox} = 3.95\frac{\mu F}{cm^2} \tag{4}$$

7.3 Calculation of ϕ_f :

We know the formula for ϕ_f
where :
N_A =1 $\times$ $10^{21}/cm^3$
n_i = 1.5 $\times$ $10^{10}/cm^3$
After putting all values ,we get:

$$\frac{kT}{q} \times ln(\frac{Na}{ni}) \tag{5}$$

On calculation. we get:

$$\phi_f = 0.383V \tag{6}$$

7.4 Calculation of work function ϕ_s

$$\phi_s = \chi + \frac{E_G}{2} + \phi_f \tag{7}$$

where:
χ = 4.05eV (Electron affinity of silicon)
E_G = 1.12eV (Bandgap energy of silicon)
ϕ_f = 0.383V
After putting all values ,we get:

$$\phi_s = 4.83eV \tag{8}$$

8 Analysis

8.1 I_D/V_G curve of PFET FDSOI:

1. Vdd = 0.9 V & Vdd = 0.05V

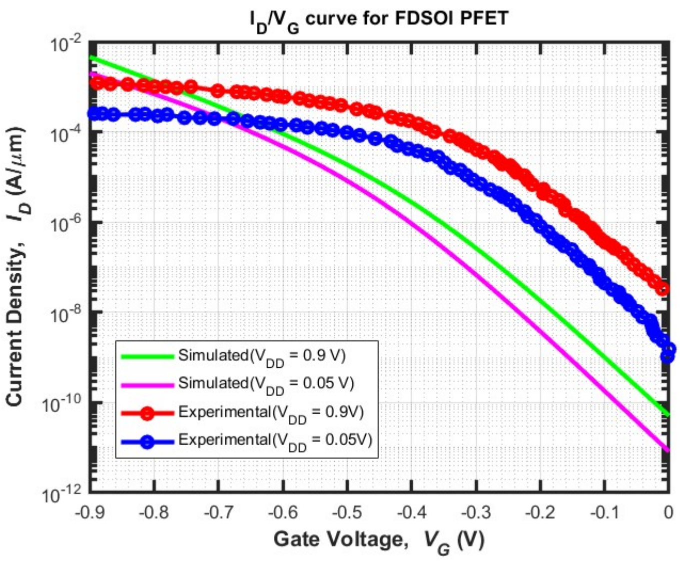

Figure 13: FDSOI PFET I_D/V_G curve

2. Vdd = 0.75 V & Vdd = 0.05V

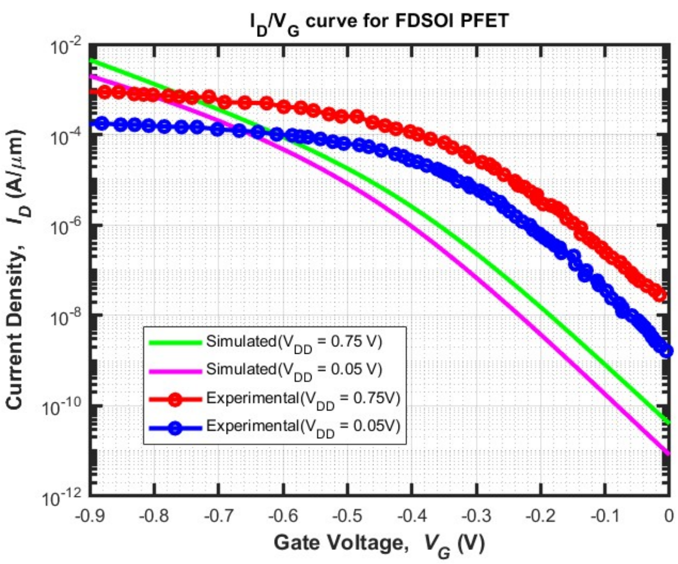

Figure 14: FDSOI PFET I_D/V_G curve

8.2 I_D/V_G curve of NFET FDSOI:

Vdd = 0.9 V

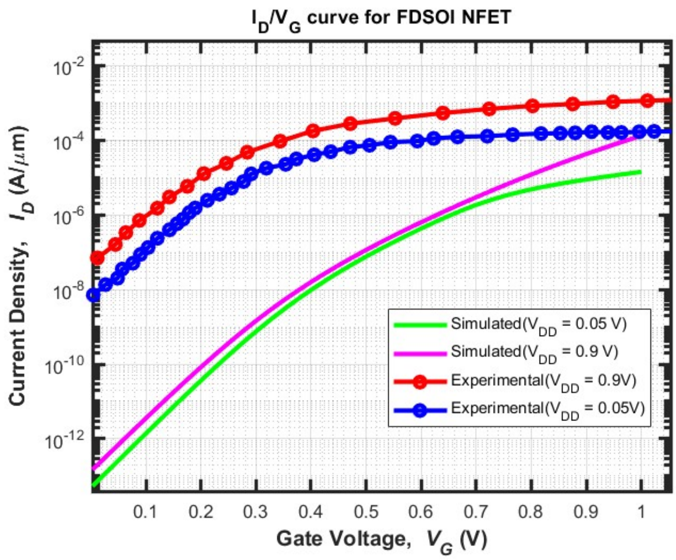

Figure 15: FDSOI NFET I_D/V_G curve

Vdd = 0.75 V

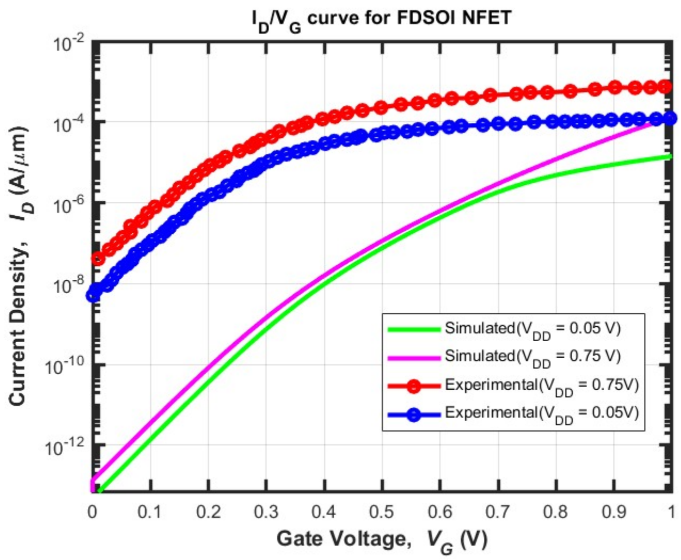

Figure 16: FDSOI NFET I_D/V_G curve at V_{DD} = 0.75V & $0.05V$

8.3 I_D/V_G curve of PFET/NFET FDSOI:

(a) Vdd = 0.9 V & $Vdd = 0.05V$

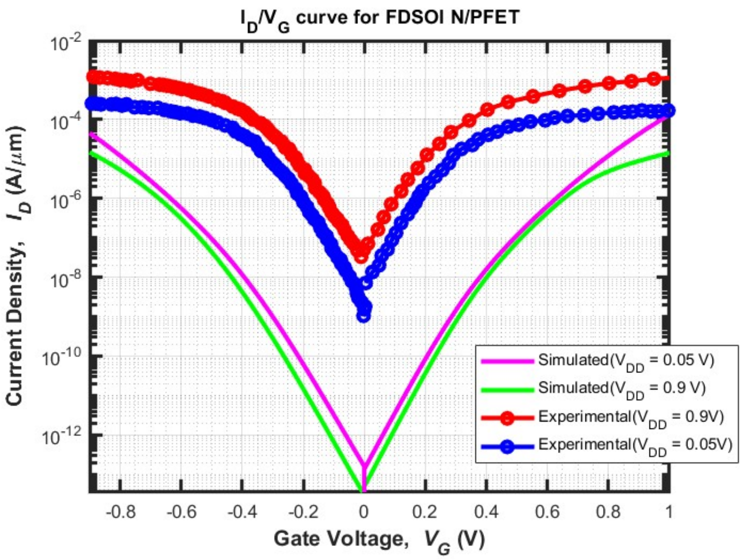

Figure 17: FDSOI N/PFET I_D/V_G curve

(b) Vdd = 0.75 V Vdd = 0.05 V

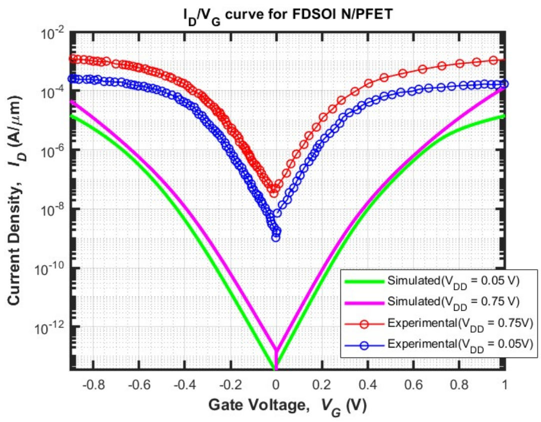

Figure 18: FDSOI N/PFET I_D/V_G curve

(a) DIBL of NFET $V_{dd}sat$ = 0.9 V and $V_{dd}lin$ = 0.05 V

$DIBL = \frac{Vth(linear) - Vth(sat)}{Vds(sat) - Vds(linear)}$

$DIBL = \frac{0.6-0.52}{0.9-0.05} = 0.094 = 94mV/V$

(b) DIBL of NFET $V_{dd}sat$ = 0.75 V and $V_{dd}lin$ = 0.05 V

$DIBL = \frac{Vth(linear) - Vth(sat)}{Vds(sat) - Vds(linear)}$

$DIBL = \frac{0.72-0.52}{0.75-0.05} = 0.285 = 285mV/V$

8.4 I_D/V_G of PFET with back bias from -2V to 2V at Vdd=0.75V

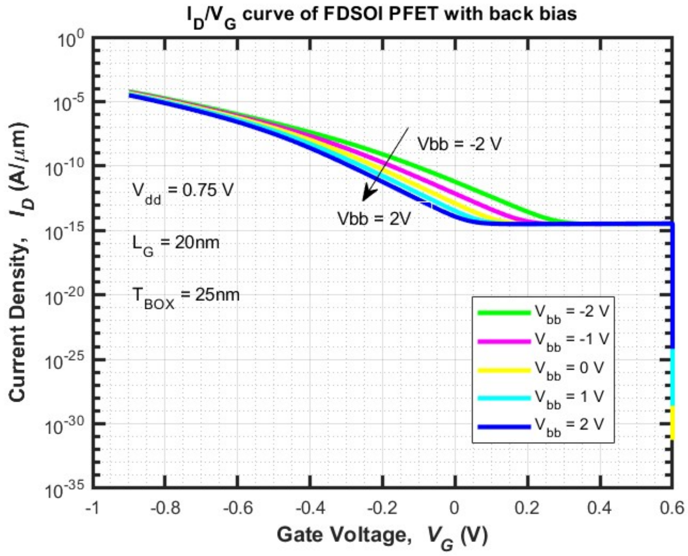

Figure 19: FDSOI PFET I_D/V_G curve with back biasing

Table 6: I_{on}/I_{off} of PFET with back bias from -2V to 2 V

I_{on} (μA)	I_{off} (f A)	I_{on} / I_{off} (10^{10})	Back Bias Voltage (V)
61.52	3.01	20.44	-2
52.32	3.19	16.40	-1
44.29	3.28	13.5	0
37.18	3.38	11	1
30.79	3.48	8.85	2

As back bias voltage increases from -2V to 2V I_{on}/I_{off} of PFET decreases.

8.5 I_D/V_G of NFET with back bias from -2V to 2V at Vdd=0.75V

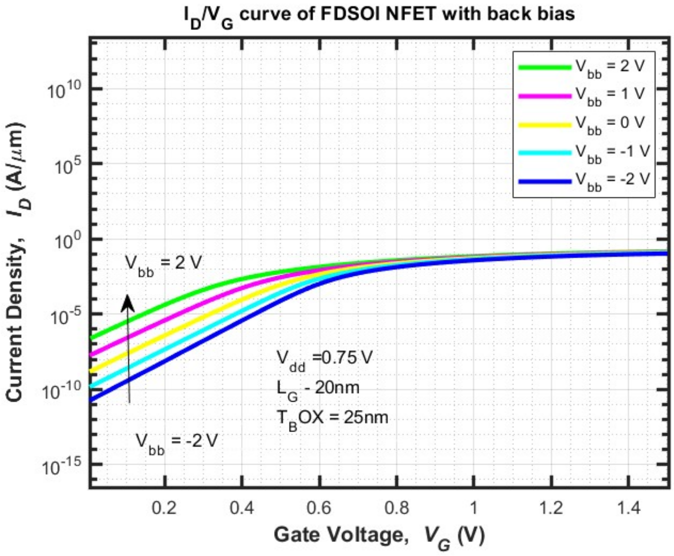

Figure 20: FDSOI NFET I_D/V_G curve with back biasing

As back bias voltage increases from -2V to 2V I_{on}/I_{off} of NFET decreases.

Table 7: I_{on}/I_{off} of NFET with back bias from -2V to 2 V

I_{on} (μA)	I_{off} (f A)	I_{on} / I_{off}	Back Bias Voltage (V)
0.1458	7.69e-11	1.89e13	-2
0.1356	5.655e-10	2.3e12	-1
0.126	5.743e-9	2.19e11	0
0.1164	6.599e-8	1.76e10	1
0.1069	9.159e-7	1.16e9	2

9 Conclusion

9.1 Comparison table

Table 8: Comparison table

Parameters	**Paper Work**	**Simulated Work**
V_{DD}	0.9V	0.9V
N/P DIBL (mV/V)	80/100	97/108
N/P Subthreshold swing(S.S) (mV/dec)	90/110	90/105
N/P Ion (mA/μm)	1.12/1.22	4.4e-5/126e-3
N/P Ioff (mA/μm)	0.63/0.67	3.28e-15/5.74e-9