Electrical and Electronics Engineering Lab Report

Exp No: *03*
Exp Name: ***Verification of Kirchhoff's Law***.
Equipmets: 1.Ammeter 2.Voltmenter 3.Bread borad 4.Three resistance 5.DC power supply 6.Connecting wires

Theory:

Kirchhoff's current law(KCL) states that the algebraic sum of current entering a node (or a closed boundary) is zero.

$$\sum_{n=1}^{N} i_n = 0$$

Kirchhoff's voltage law(KVL) states that the algebraic sum of all voltages around a close palth (or looop) is zero.

$$\sum_{m=1}^{M} V_m = 0$$

Circuit diagram of KCL: The circuit diagram is look like the following figure below.

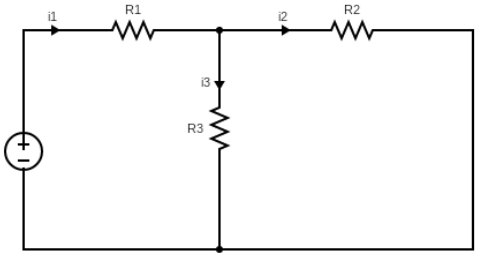

Fig 3.1: KCL Circuit diagram

Calculation:

black

Data table:

$s.n$	$voltage(V)$	I_1	I_2	I_3	$Error = \lvert\frac{V_s-(I_1+I_2+I_3)}{V_s}\rvert \times 100\%$
1	3	$black$	$black$	$black$	$black\%$
2	4	$black$	$black$	$black$	$black\%$
3	6	$black$	$black$	$black$	$black\%$

Circuit diagram of KVL: The circuit diagram is look like the following figure below.

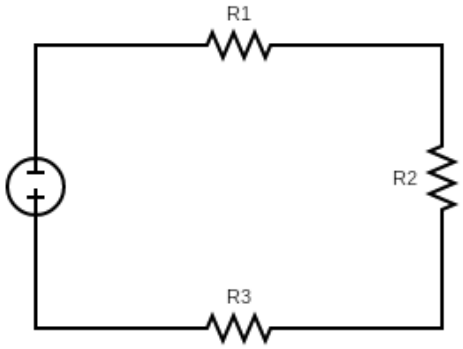

Fig 3.2: KVL Circuit diagram

Calculation:

$$black$$

Data table:

$s.n$	$Voltage(V_s)$	V_1	V_2	V_3	$Error = \lvert\frac{V_s-(V_1+V_2+V_3)}{V_s}\rvert \times 100\%$
1	3	$black$	$black$	$black$	$black\%$
2	4	$black$	$black$	$black$	$black\%$
3	6	$black$	$black$	$black$	$black\%$

Result: blank

Discussion: blank