Architecture I

ECE 3710

One time a cop pulled me over for running a stop sign. He said, "Didn't you see the stop sign?" I said, "Yeah, but I don't believe everything I read."

- Steven Wright

why you should read:

Trivia: Reading Test — *Udder Buffoonery™ Productions LLC*

Reading Test

I cdnuolt blveiee taht I cluod aulaclty uesdnatnrd waht I was rdgnieg.

THE PAOMNNEHAL PWEOR OF THE HMUAN MNID

Aoccdrnig to a rscheearch at Cmabrigde Uinervtisy, it deosn't mttaer in waht oredr the ltteers in a wrod are, the olny iprmoatnt tihng is taht the frist and lsat ltteer be in the rghit pclae. The rset can be a taotl mses and you can sitll raed it wouthit porbelm. Tihs is bcuseae the huamn mnid deos not raed ervey lteter by istlef, but the wrod as a wlohe.

Amzanighuh ?

UdderButtoonery.com

don’t make millions of years of evolution a waste of time, eh?

lecture notes != abridged version of text

next week: assembly and I/O

terminology for *memory* only

Bit : a binary digit that can have the value 0 or 1

Byte : 8 bits

Nibble : half of a bye, or 4 bits

Word : two bytes, or 16 bits

no

Kilobyte (K): 2^{10} bytes

Megabyte (M) : 2^{20} bytes, over 1 million

Gigabyte (G) : 2^{30} bytes, over 1 billion

Terabyte (T) : 2^{40} bytes, over 1 trillion

JEDEC

assumed whenever discussing memory

Kibibyte (KiB)

Mebibyte (MiB)

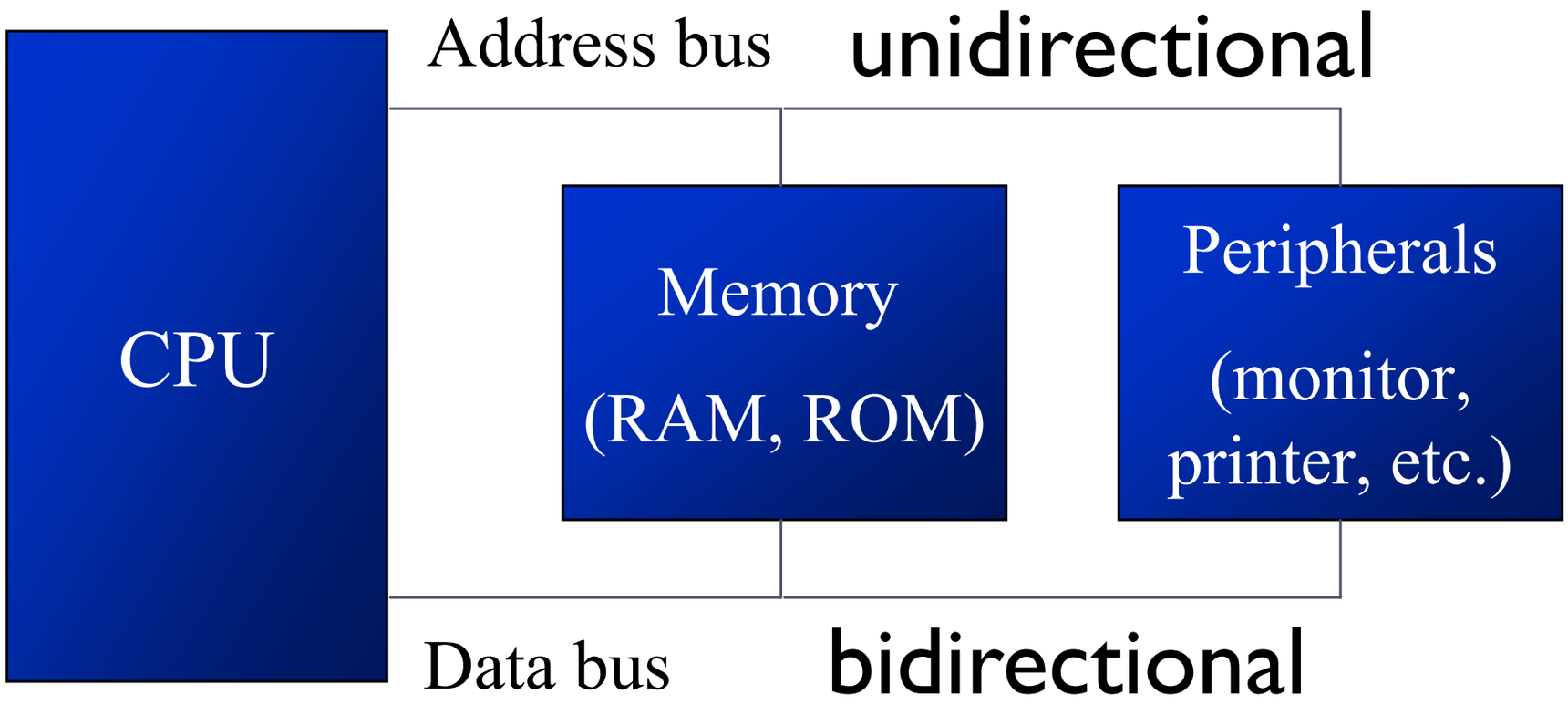
Gibibyte (GiB)

Tebibyte (TiB)

IEC

buses: how information is moved

(#wires != #bits)



address: how computers know where to get/store information

- The more data buses available, the better the CPU
  - Think of data buses as highway lanes
- More data buses mean a more expensive CPU and computer
  - The average size of data buses in CPUs varies between 8 and 64
- Data buses are bidirectional
  - To receive or send data
- The processing power of a computer is related to the size of its buses


KaaZ

The first PC motherboards with support for RDRAM debuted in 1999. They supported PC800 RDRAM, which operated at 400 MHz but presented data on both rise and fall of clock cycle resulting in effectively 800 MHz, and delivered 1600 MB/s of bandwidth over a 16-bit bus using a 184-pin RIMM form factor. This was significantly faster than the previous standard, PC133 SDRAM, which operated at 133 MHz and delivered 1066 MB/s of bandwidth over a 64-bit bus using a 168-pin DIMM form factor.

cost: $RDRAM > $SDRAM &
bus: #RDRAM < #SDRAM &
throughput: #RDRAM > #SDRAM

simple performance comparisons...

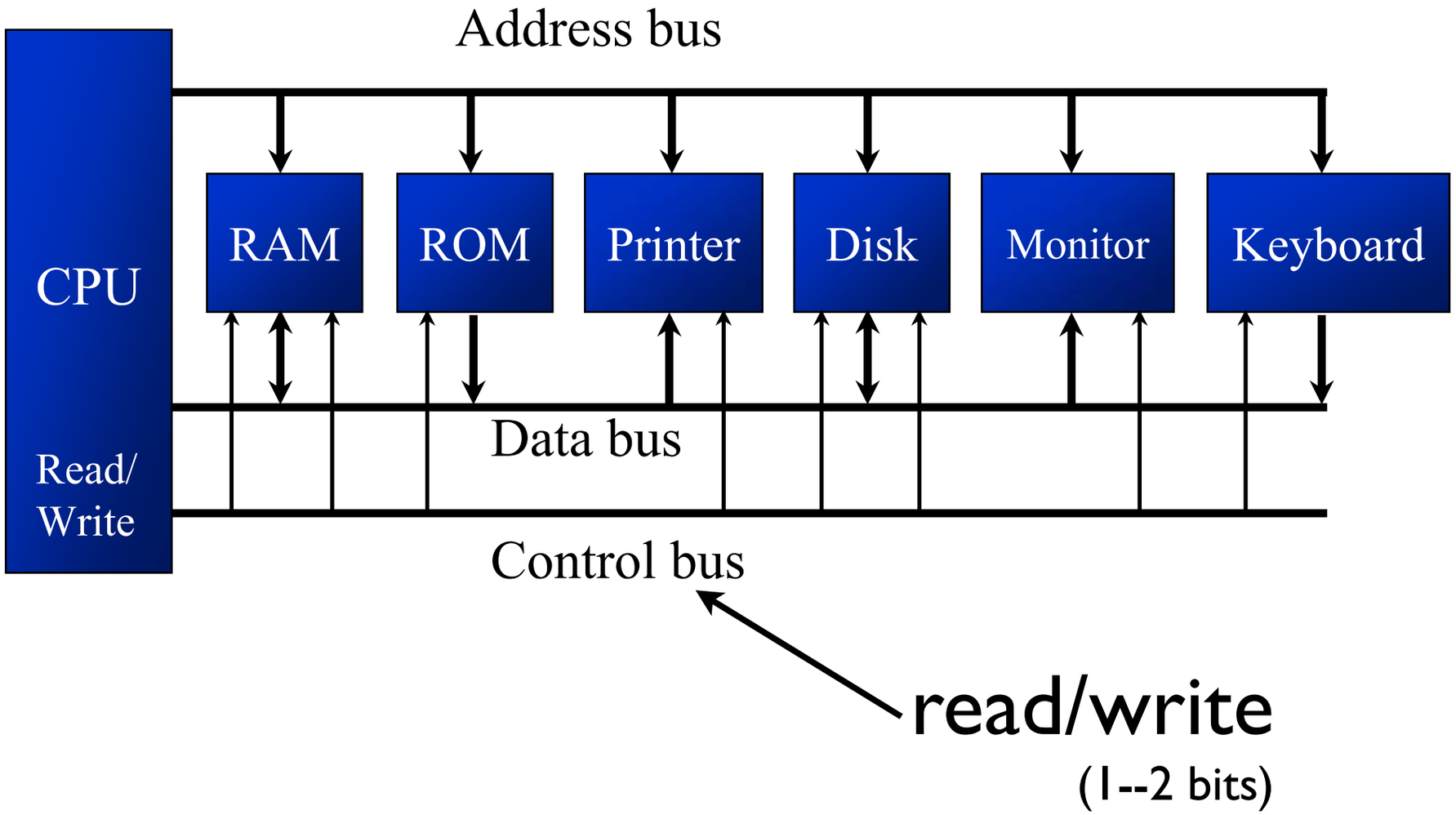
e.g. Pentium IV @ 3.5 GHz vs Intel i7 @ 2.5 GHz

a great space heater; see last generation of Power Mac G5s, too

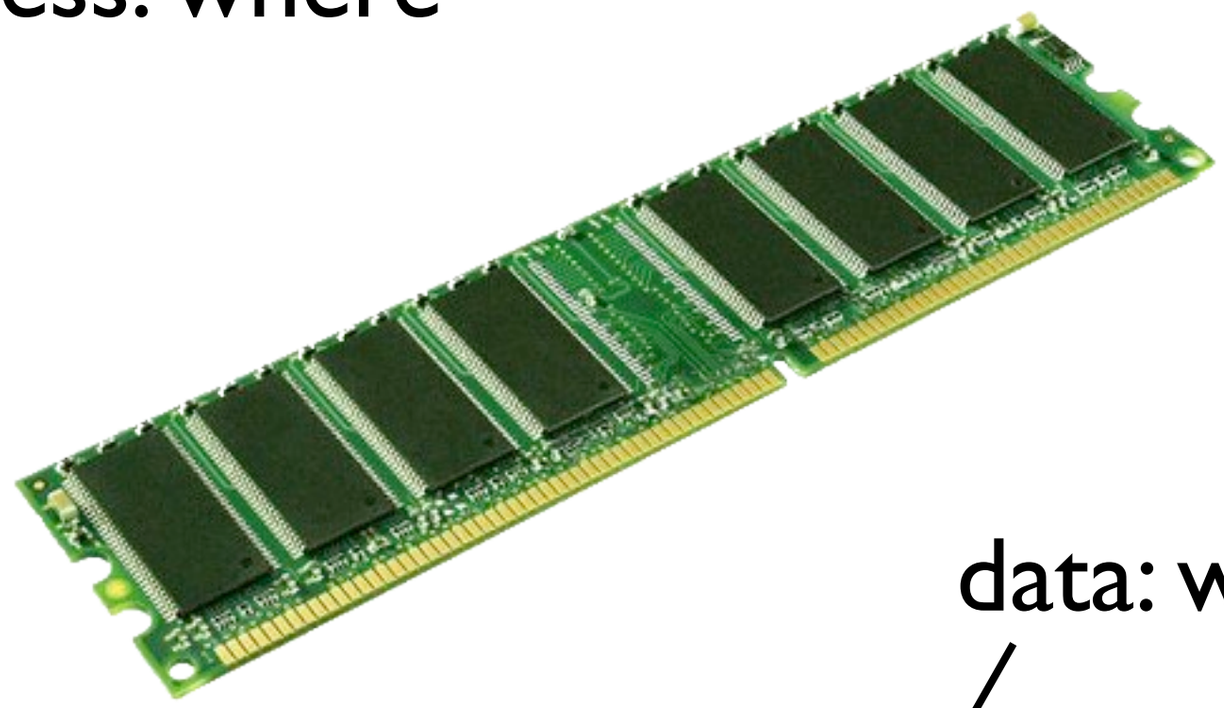
how do devices know address is for them?

does it refer to read or write?

(i.e. should they expect to send or receive data?)



address: where



data: what

order: endianness

(gah!)

endianness: byte

req. ten bits

dec2hex(1000):

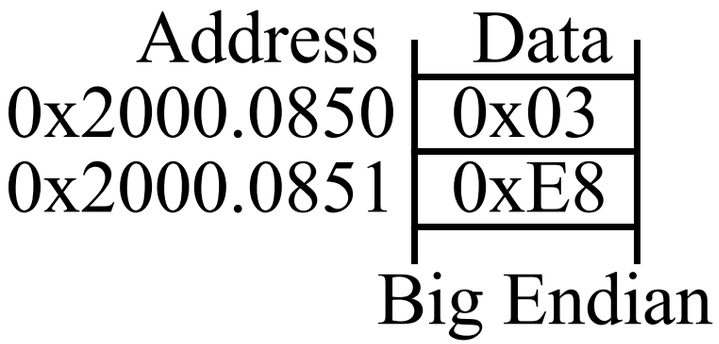
$2^9_{(512)}+2^8_{(256;768)}+2^7_{(128;896)}+2^6_{(64;960)}+2^5_{(32;992)}+2^3_{(8;1000)}$

= 1111101000

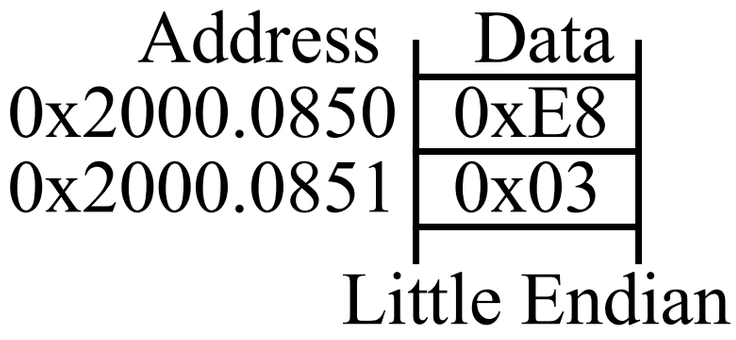
= 0000001111101000

= 0x03E8

use closest multiple of 8-bits



MSByte stored at lowest addr.



LSByte stored at lowest addr.

note: Cortex-M3 is little by default

endianness: bit

order follows byte

e.g.: 0x0A0B0C0D

big endian:

byte addr	0	1	2	3
bit offset	01234567	01234567	01234567	01234567
binary	00001010	00001011	00001100	00001101
hex	0a	0b	0c	0d

little endian:

byte addr	3	2	1	0
bit offset	76543210	76543210	76543210	76543210
binary	00001010	00001011	00001100	00001101
hex	0a	0b	0c	0d

always put MSB first when writing

smallest
(in general)

address bus:

1. what: byte
2. how many (e.g. 16-bit bus: 2^16 = 64 KiB)

2^16 = 2^6*2^10= 64 KiB

data bus:

1. can be more or less than address
2. how much

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I have dropped the 'i' as when we're speaking about memory IEC units are implicit

Q: 32-bit address bus, how much memory (MB)?

byte-addressable, direct

1MB := 2^20 B

Q: 32-bit address bus, how much RAM (MB)?

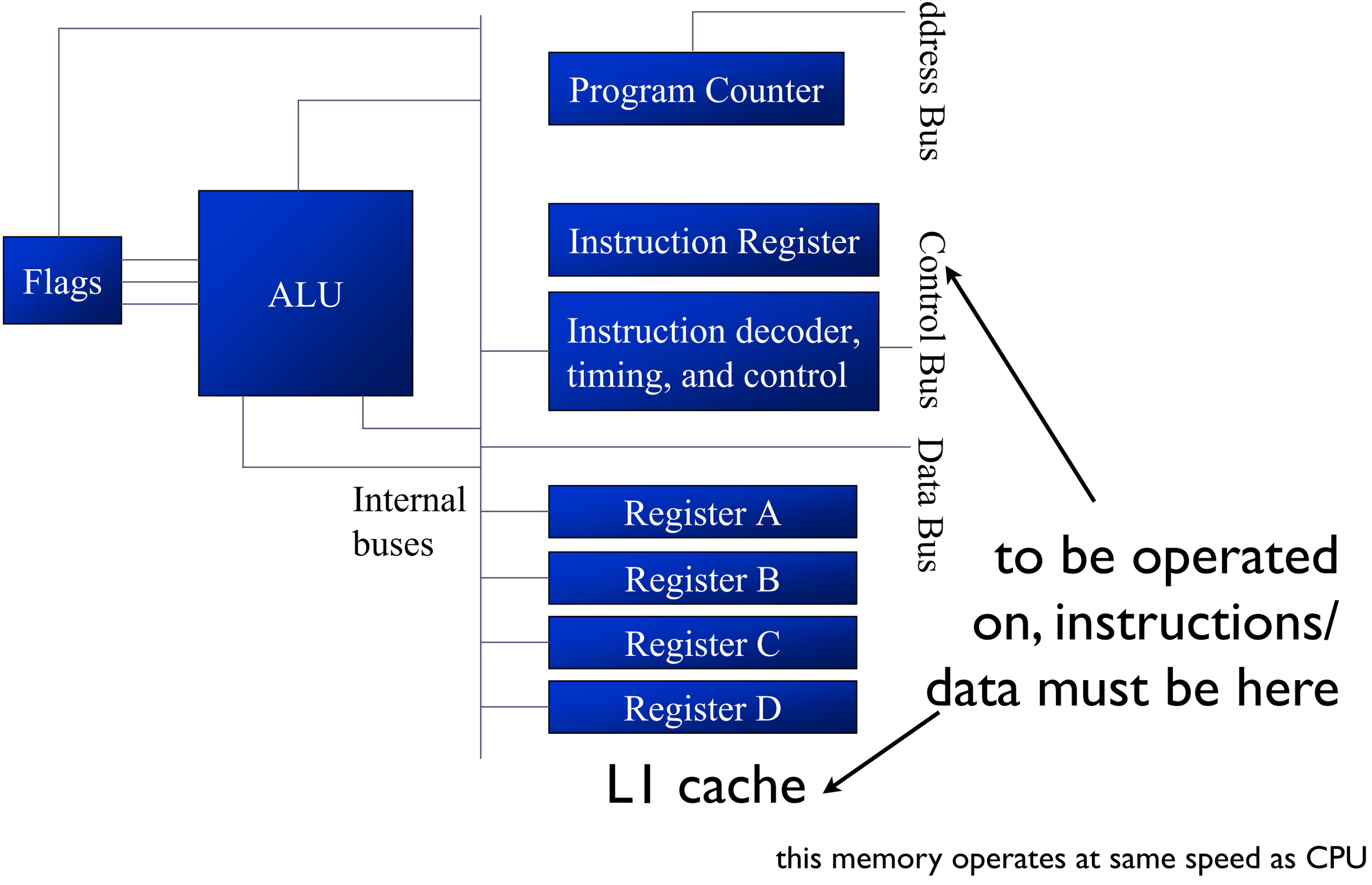
A: $2^{32} = 2^{20} \times 2^{12} = 4096 \text{ MB}$

Q: if we address byte, why is data bus > 8 bits?

Q: if we address byte, why is data bus > 8 bits?

A:

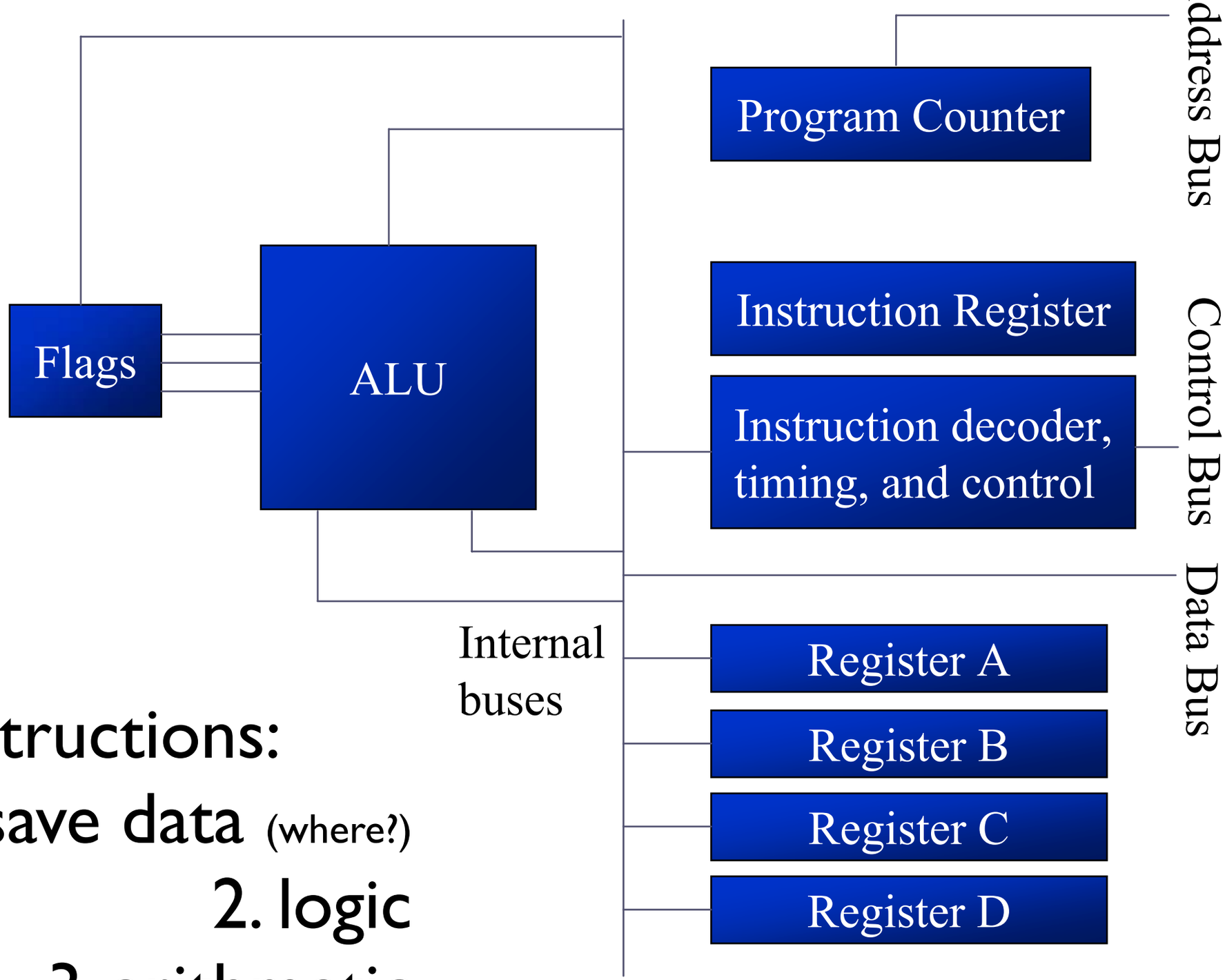
1. can address more
2. memory is slow, get data moving


Program Counter
Address Bus
Instruction Register
Instruction decoder, timing, and control
Control Bus
Flags
ALU
Internal buses
Register A
Register B
Register C
Register D
Data Bus
to be operated on, instructions/ data must be here
L1 cache
this memory operates at same speed as CPU

n-bit computing:

1. # addressable bytes
2. size of registers
3. size of instructions
4. size of data natively handled (numbers, e.g.)

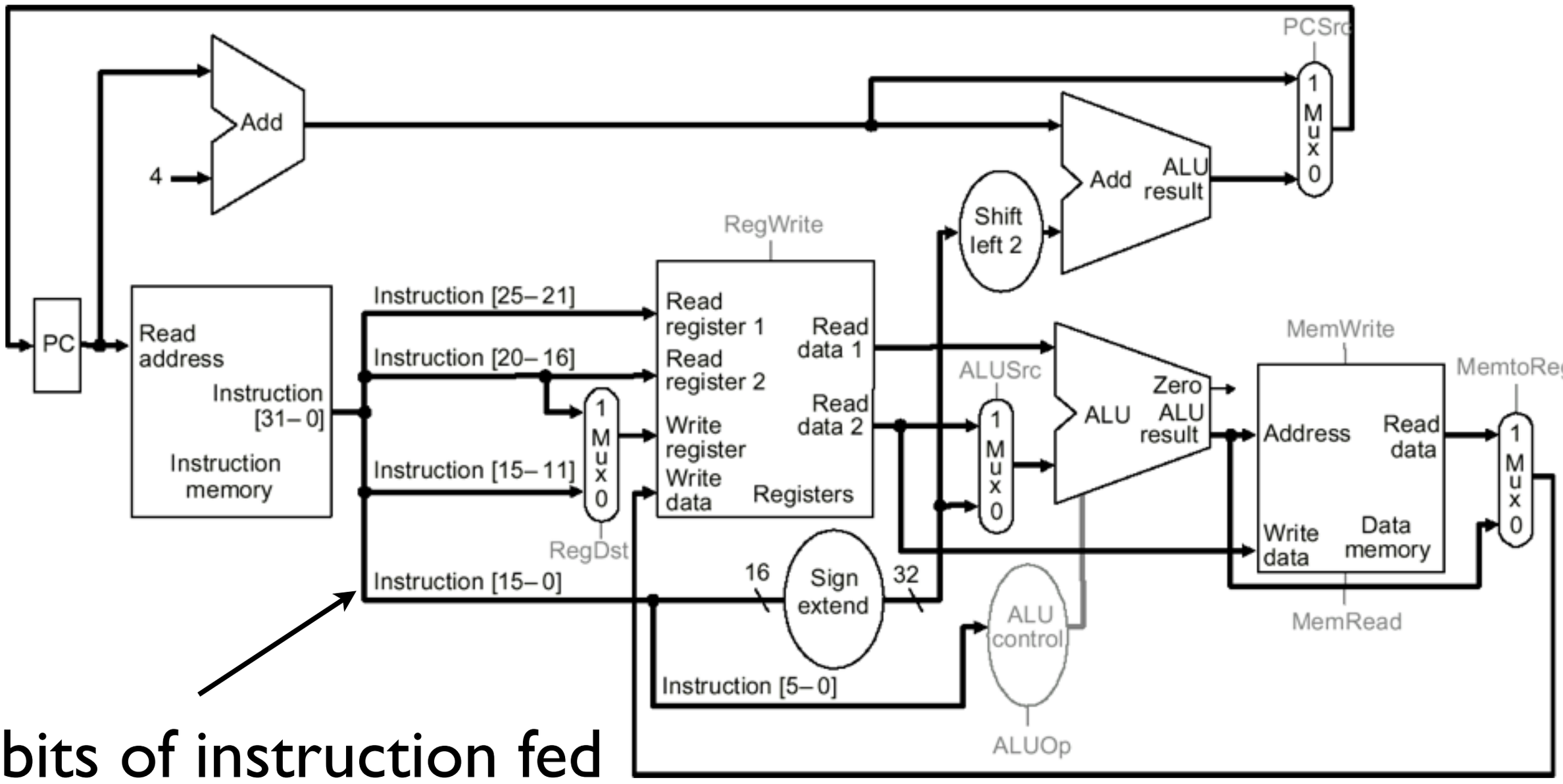
how do we use this?



computer instructions:

1. load/save data (where?)
2. logic
3. arithmetic

32-bit single cycle MIPS



bits of instruction fed to various components