Lab 1

6.1 Excercise 1

6.1.1 Calculation

According to the KVL

We have the first equation: - 12 - 4i + 2v_0 – 4 – 6i = 0 (1)

According to the Ohm's law

We have the second quation: v_0 = 6i (2)

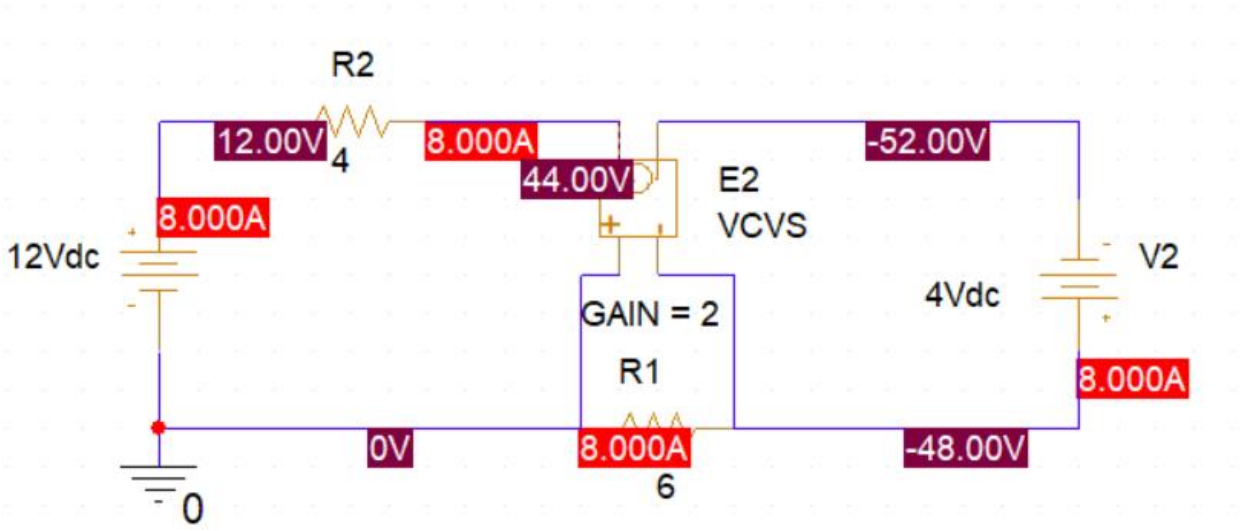
From (1) and (2) we have:

v_0 = 48V

i = 8A

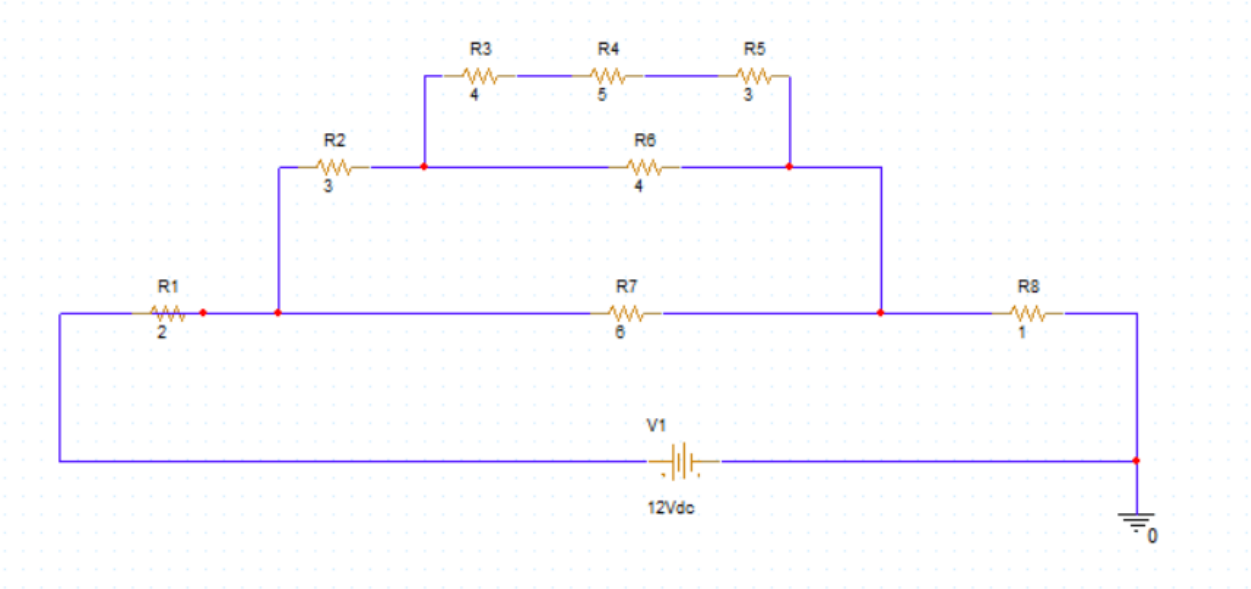
6.1.2 Simulation

Simulation result (image)



6.2 Exercise 2

6.2.1 Rearrange the circuit



6.2.2 Calculation

R3, R4, R5 in series and parallel with R6 so:

$R_{CD\_3456} = \frac{(R3+R4+R5)*R6}{R3+R4+R5+R6} = \frac{(4+5+3)*4}{4+5+3+4} = 3\Omega$

R2 and R_{CD_3456} in series and parallel with R7 so:

$R_{BE} = \frac{(R_{CD_{3456}}+R2)*R7}{R_{CD\_3456}+R2+R7} = \frac{(3+3)*6}{3+3+6} = 3\Omega$

R1, R_{BE} and R8 in series so:

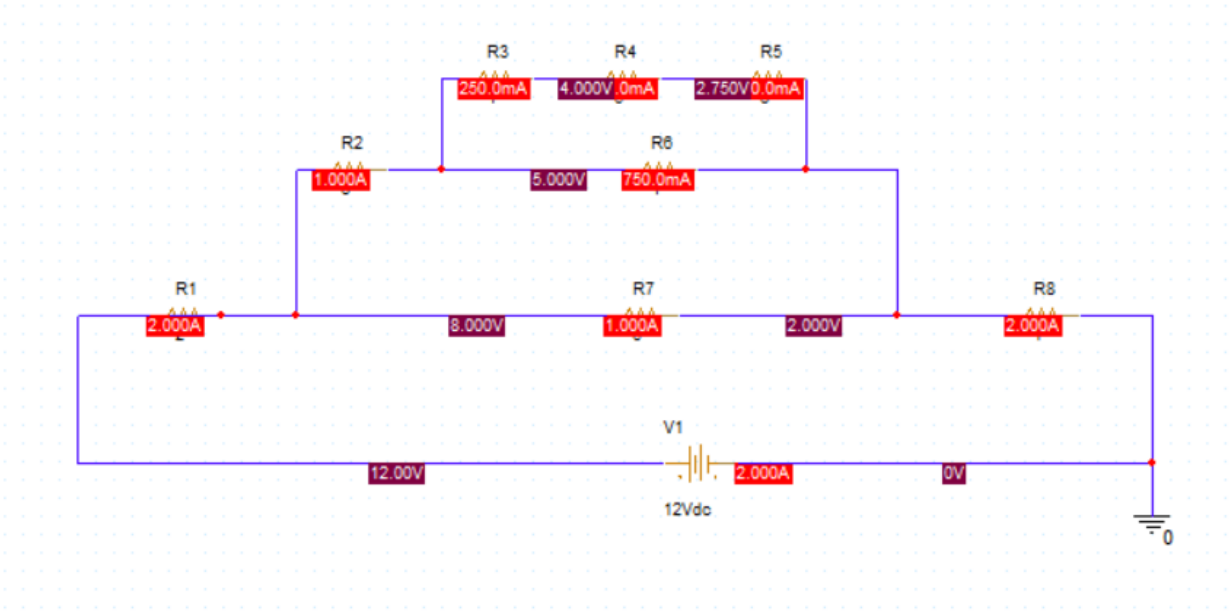
R_{AF} = R1 + R_{BE} + R8 = 2 + 3 + 1 = 6 Ω

According to the Ohm's law

We have:

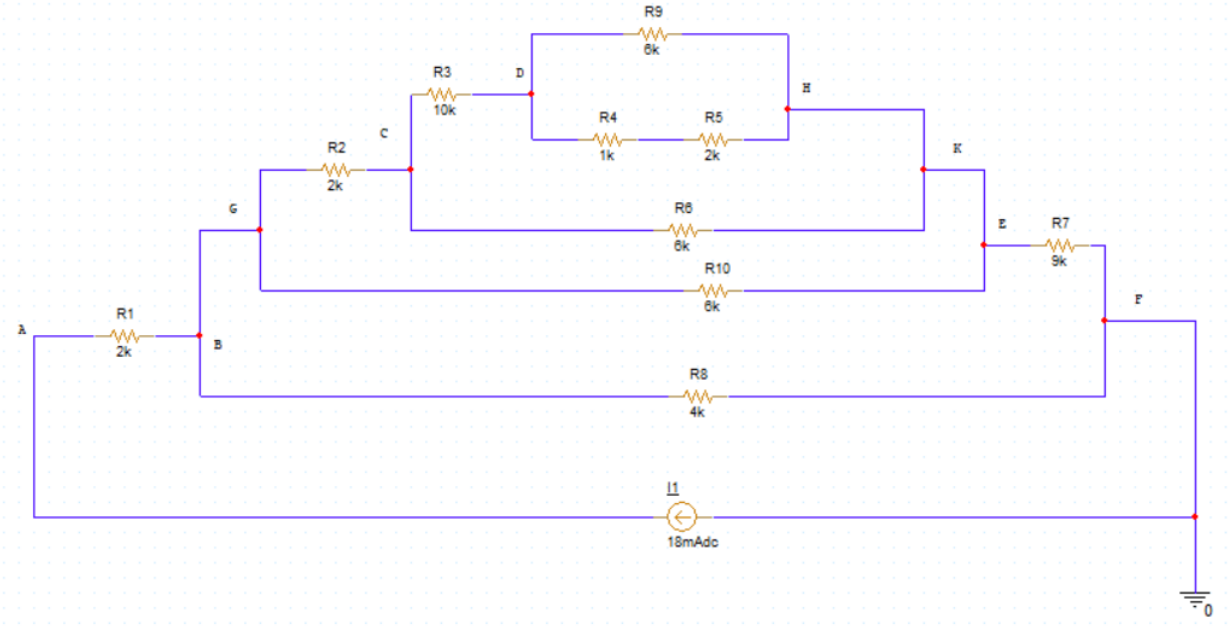
$I_{AB} = \frac{V1}{R_{AF}} = \frac{12}{6} = 2A$

6.2.3 Simulation



6.3 Exercise 3

6.3.1 Rearrange the circuit



6.3.2 Calculation

Due (((((((R4, R5 in series and parallel with R9) in series with R3) parallel with R6) in series with R2) parallel R10) in series with R7) parallel R8) in series with R1) so:

R_{AF} = 5 Ω

According to the Ohm's law

We have:

V_A = I.R_{AF} = $18.10^{-3}.5.10^{3}$ = 90V

According to voltage division we have:

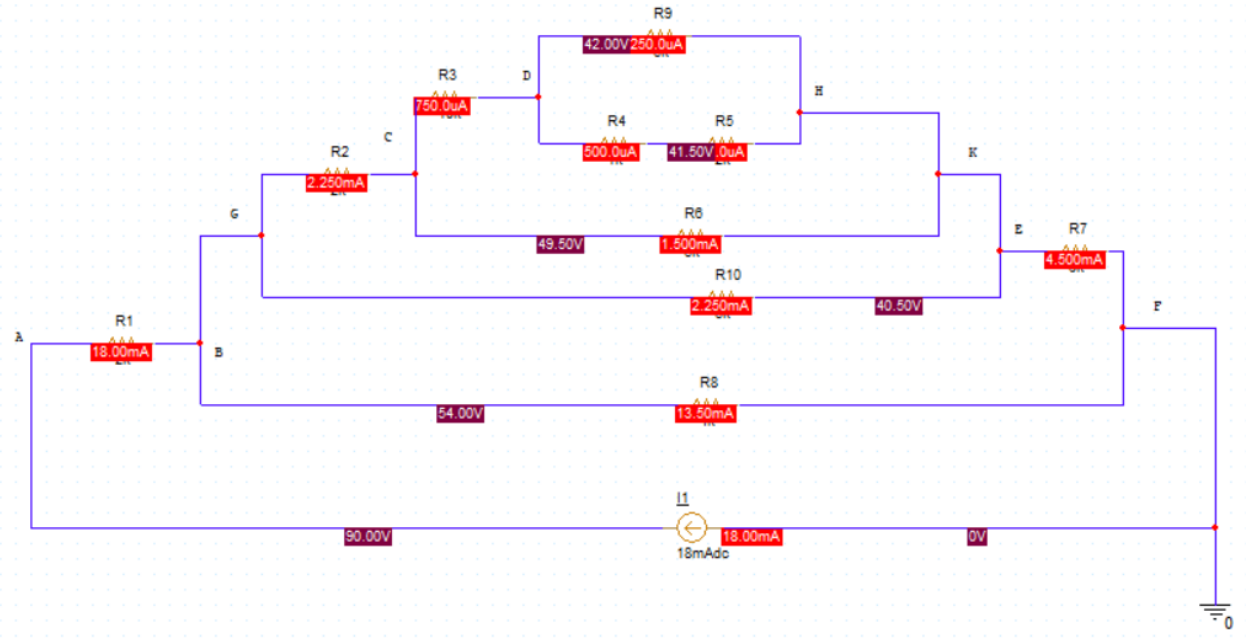
$V_B = V_A - I_1 * R_1 = 90 - 18.10^{-3}.2.10^3 = 54V$

$V_C = V_B - I_2 * R_2 = 54 - 2{,}25.10^{-3}.\ 2.10^3 = 49{,}5V$

$V_D = V_C - I_3 * R_3 = 49{,}5 - 0{,}75.\ 10^{-3}.10.\ 10^3 = 42V$

$V_E = V_B - I_G * R_{GE} = 54 - 4{,}5.\ 10^{-3}.3.\ 10^3 = 40{,}5V$

6.3.3 Simulation



6.4 Exercise 4

6.4.1 Calculation

$R_{tong} = \frac{(3k+3k)*6k}{3k+3k+6k} + 9k = 12k\Omega$

According to Ohm's law, we have:

$I_1 = \frac{12}{R_{tong}} = \frac{12}{12k} = 1mA$

$V_a = I_1.3k = 3V$

$I_2 = \frac{V_a}{6k} = \frac{3}{6k} = 0{,}5mA$

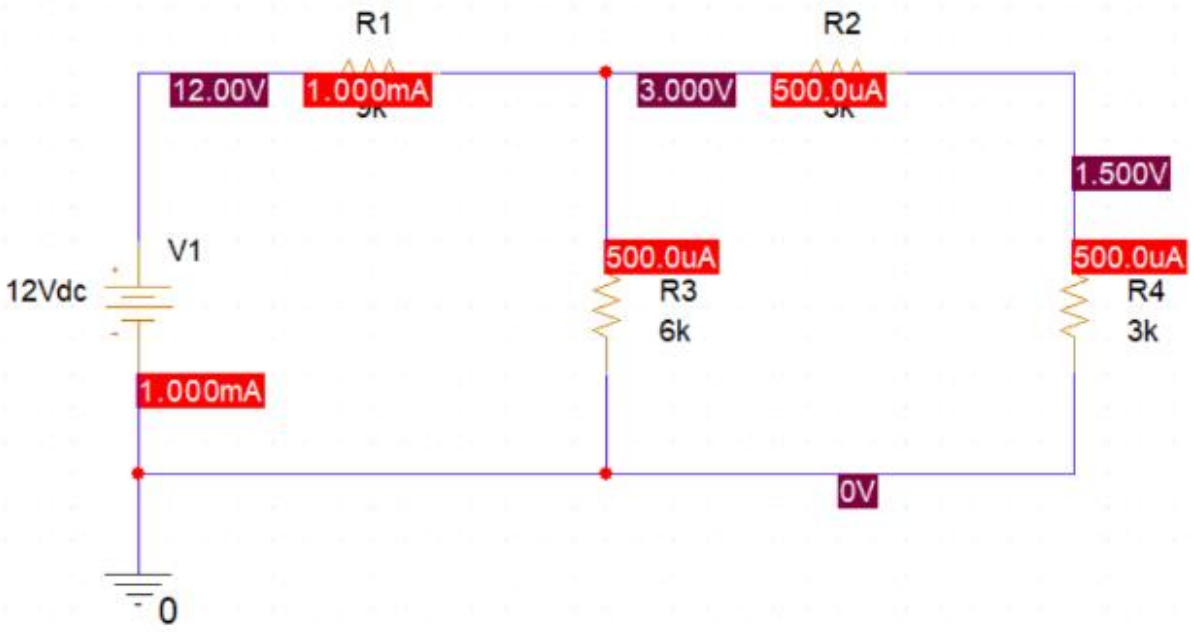
According to KCL, we have

$I_1 = I_2 + I_3$

$\rightarrow I_3 = I_1 - I_2 = 1mA - 0{,}5mA = 0{,}5mA$

$V_b = 3k.\ I_3 = 1{,}5V$

6.4.2 Simulation



6.5 Exercise 5

According to KVL, we have

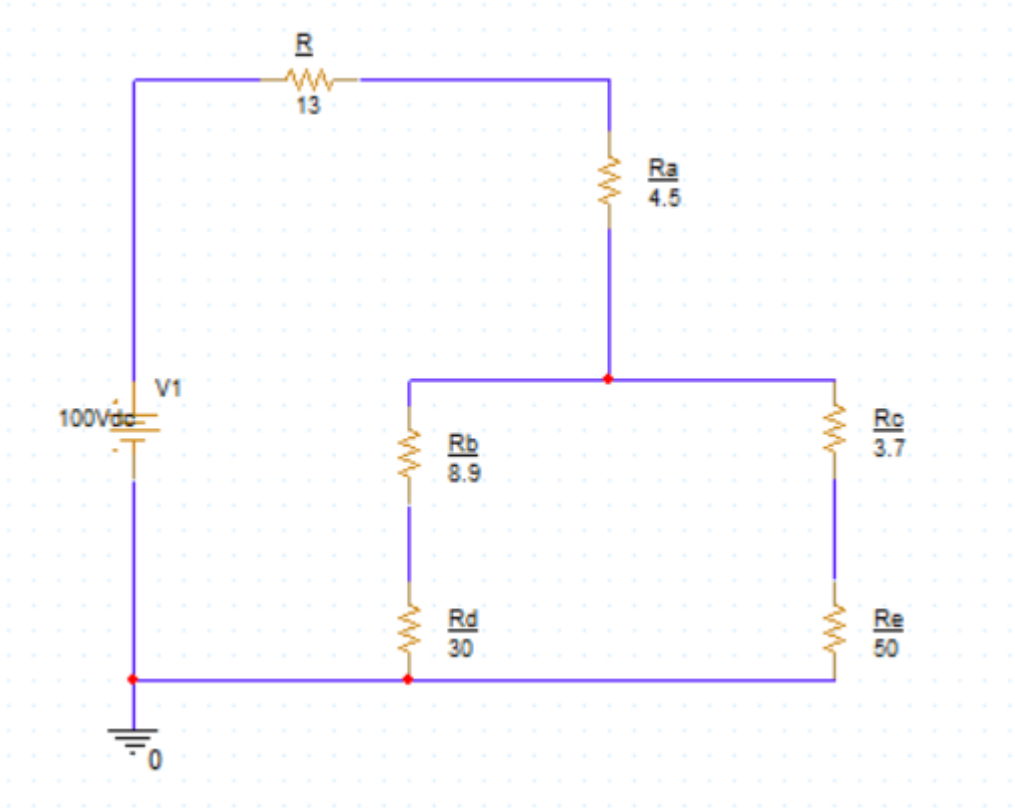
V_R = 24 – 5 = 19V

I = $\frac{5}{3{,}9k}$ = 1,282 mA

a. R = $\frac{V_R}{I}$ = 14,82kΩ
b. 10% tolerance resistor is 15 kΩ
c. I = $\frac{24}{(15k+3{,}9k)}$ = 1,27 mA → V_1 = I.R = 4,953V
d. % Error = $\frac{(4{,}953-5)}{5}$.100 = -0.94%
e. P = I^2.R = $(1{,}27.10^{-3})^2$.15k = 24,2 mW

6.6 Exercise 6

6.6.1 Circuit transformation



$R_a = \frac{24.10}{24+10+20} = 4{,}44\Omega$

$R_b = \frac{24.20}{24+10+20} = 8{,}9\Omega$

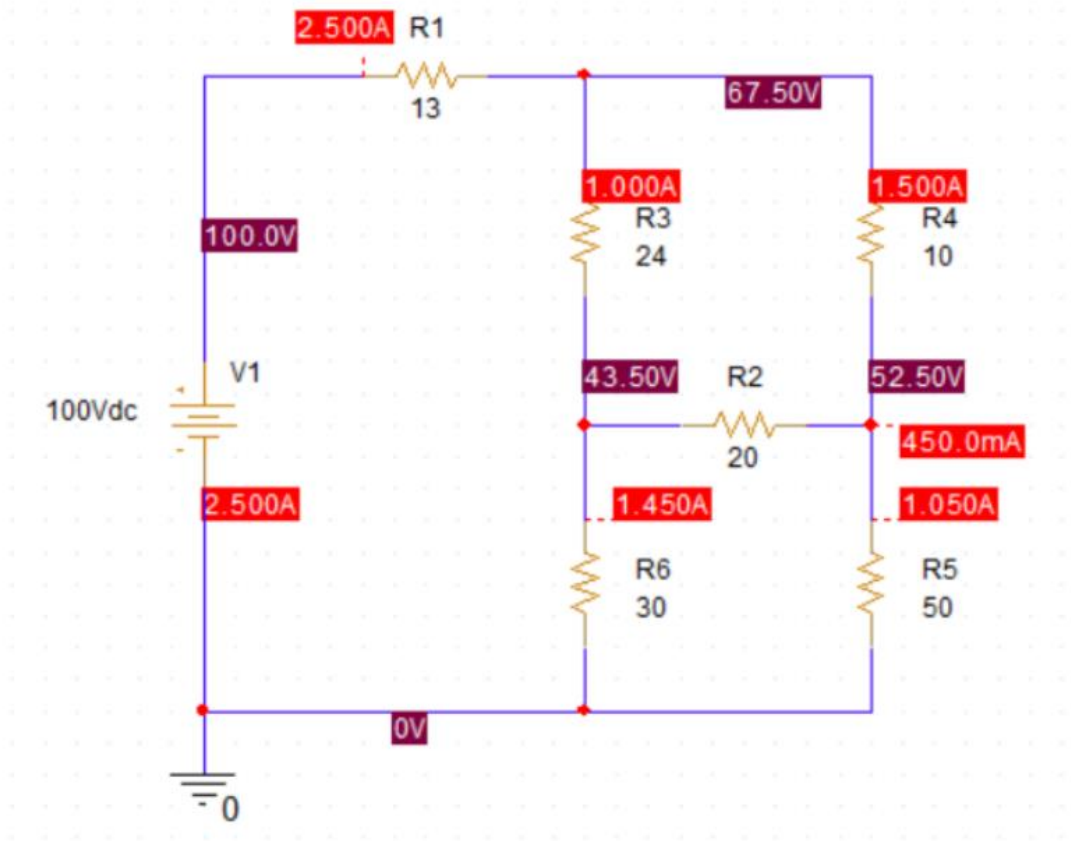
$R_c = \frac{10.20}{24+10+20} = 3{,}7\Omega$

6.6.2 Calculation

$R_{ab} = \frac{(3{,}7+50).(8{,}9+30)}{(3{,}7+50)+(8{,}9+30)} + 4{,}5 + 13 = 40\Omega$

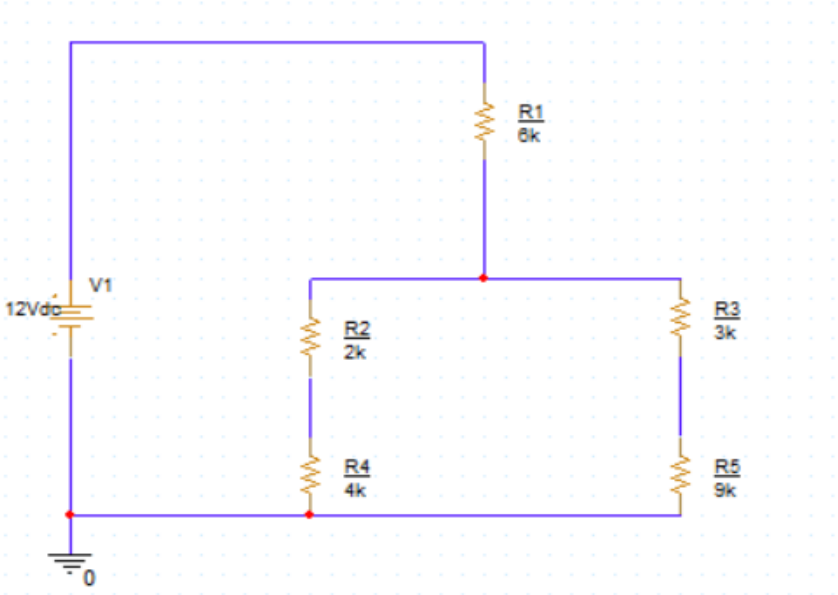
$i = \frac{100}{40} = 2{,}5A$

6.6.3 Simulation



6.7 Exercise 7

6.7.1 Circuit transformation



R1 = $\frac{12k.18k}{12k+18k+6k}$ = 6k Ω

R2 = $\frac{6k.12k}{12k+18k+6k}$ = 2k Ω

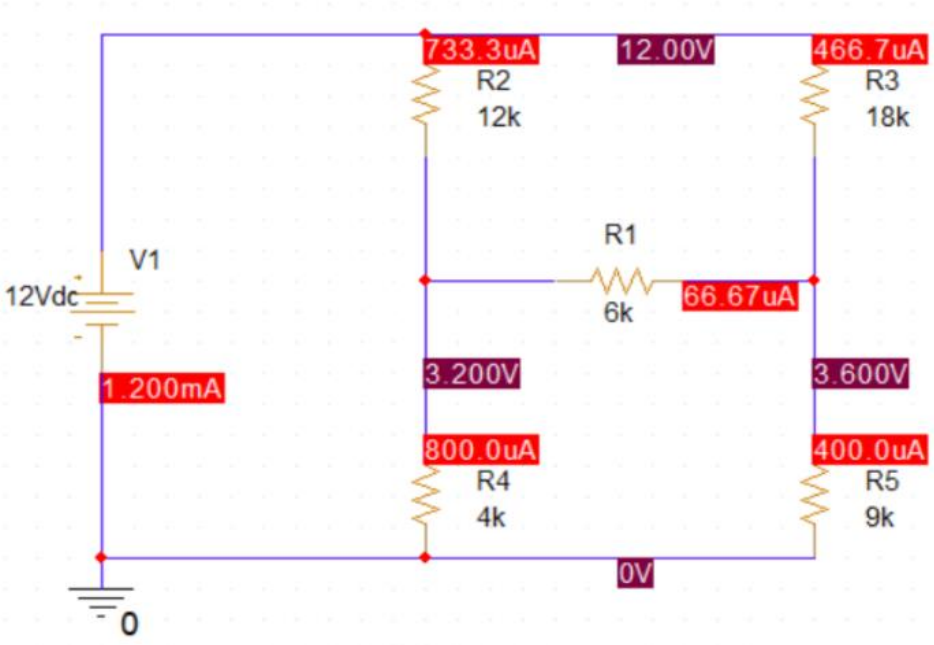
R3 = $\frac{6k.18k}{12k+18k+6k}$ = 3k Ω

6.7.2 Calculation

$R_{equipvalent} = \frac{(3k+9k).(2k+4k)}{(3k+9k)+(2k+4k)}$ = 10k Ω

$I_s = \frac{12}{10k}$ = 1,2 mA

6.7.3 Simulation



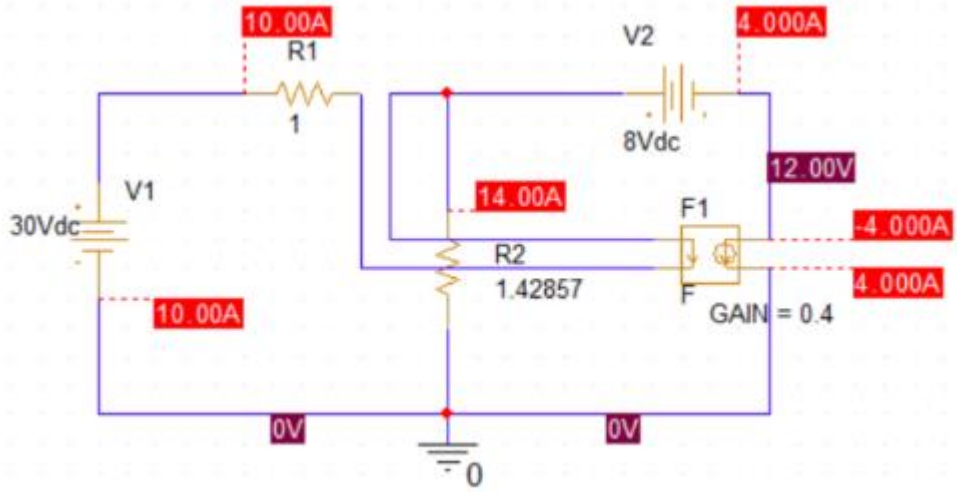
6.8 Exercise 8

p_2 =10.10 = 100W → Passive element

p_3 = 20.14 = 100W → Passive element

p_4 = - 8.4 = -32W → Active element

6.8.2 Redraw the circuit for simulation



6.9 Exercise 9

6.9.1 Calculation

According to the KVL

We have:

v = 10 – 4 = 6V

$i_x = \frac{4-16}{3}$ = -4A

So, we have:

p_1 = -4.4 = -16 → Active element

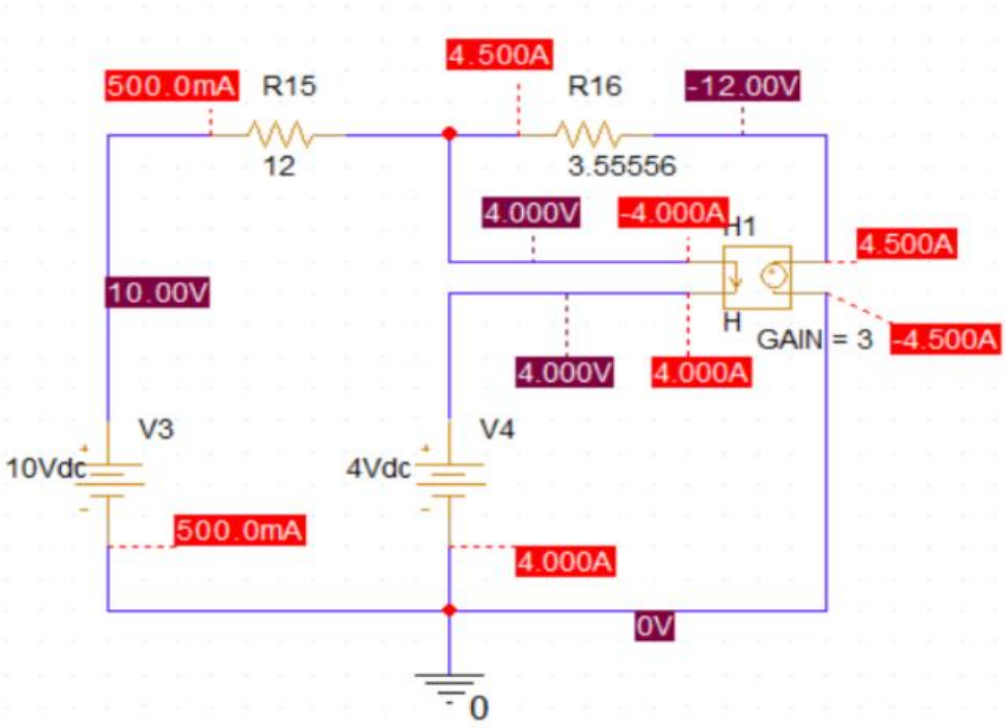
$I_{AB} = \frac{6}{12}$ = 0,5A

I_{BC} = 0,5 – (-4) = 4,5A

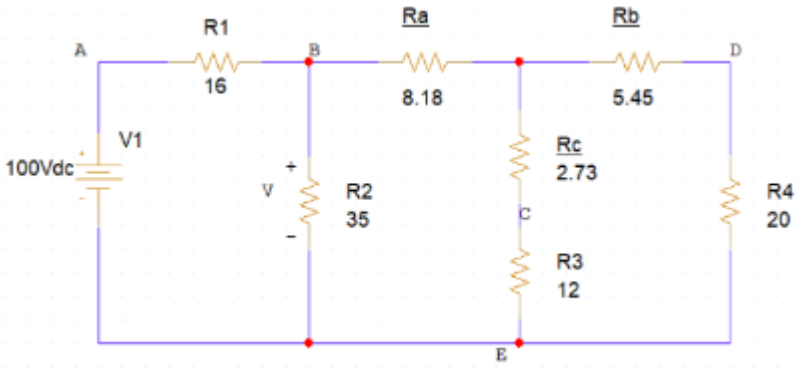
p_2 = 16.4,5 = 72W → Passive element

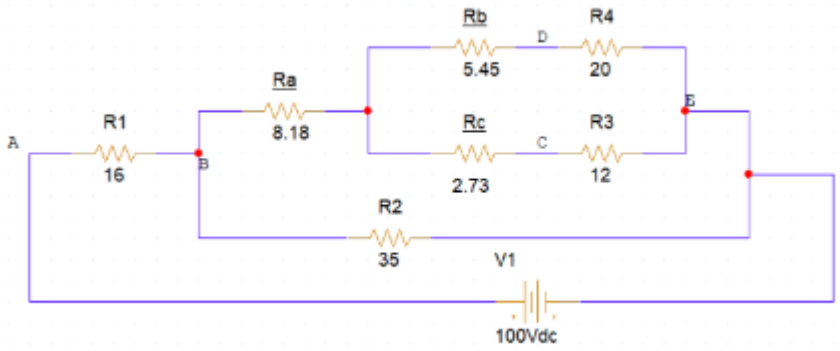
U_{CD} = 3. i_x = -12V

6.9.2 Simulation



6.10 Exercise 10





According to Delta-wye

$R_a = \frac{15.30}{10+15+30}$ = 8,18 Ω

$R_b = \frac{10.30}{10+15+30}$ = 5,45 Ω

$R_c = \frac{10.15}{10+15+30}$ = 2,73 Ω

So we have:

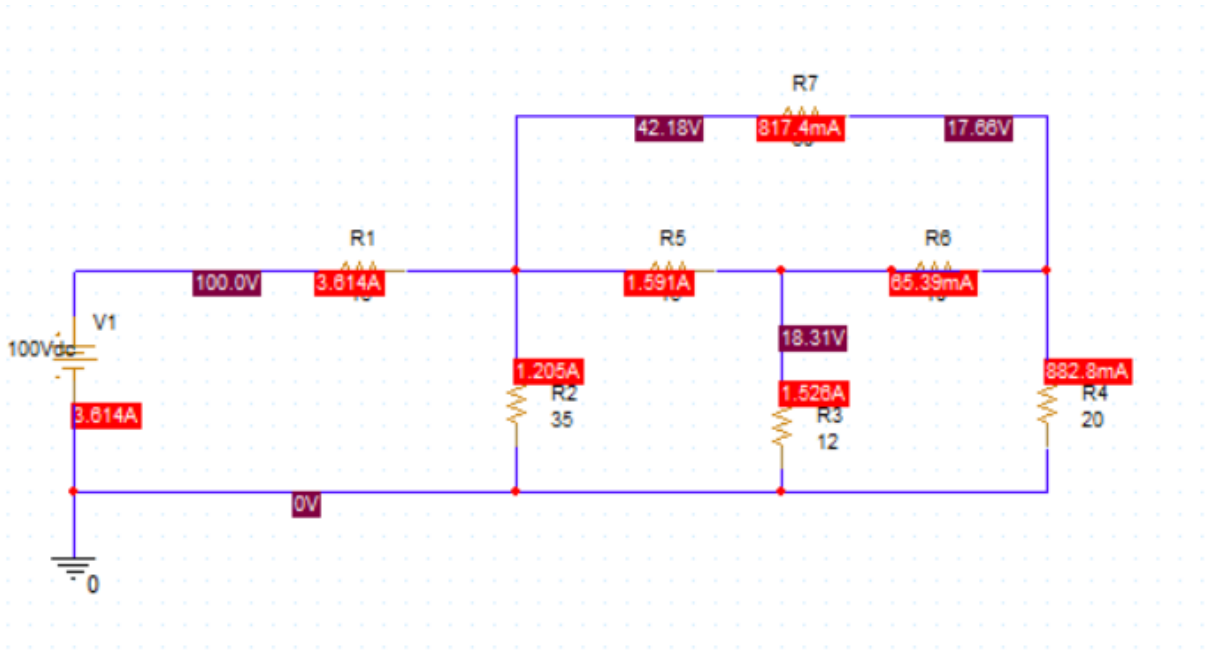
R_{tong} = 27,67 Ω

I = $\frac{100}{R_{tong}}$ = 3,61A

According to KVL

100 - I_1R_1 – V = 0 → V = 100 - I_1R_1 = 100 – 16.3,61 = 42,24V

Simulation



LAB 2

1. Complete diode model

   1.1 Theory calculation

   According to the: Complete diode model

   Formula to calculate VD: VF = 0.7V

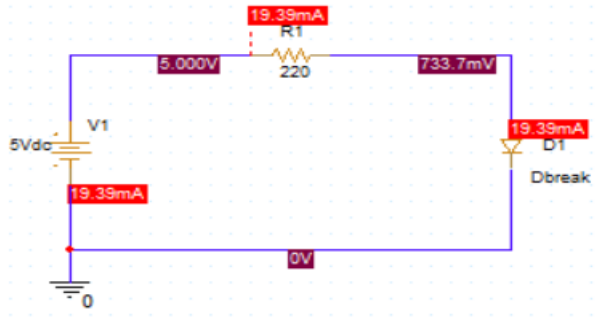
   Formula to calculate VR: I*R

   Formula to calculate I: (V-0.7)/(R + RD)

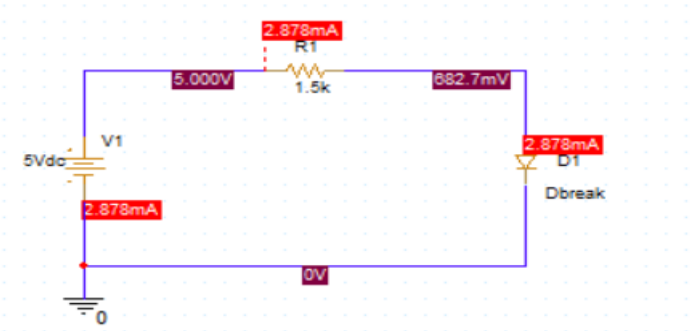
   Finally, when R = 220 Ohm, VR = IR = ((5-0,7)/(220 + 50))*220 = 3.503 V

   And when R = 1.5k Ohm, VR = IR = = ((5-0,7)/(1500 + 50))*1500 = 4.161 V

   1.2 PSpice Simulation



Hình 1: R= 220 Ohm



Hình 2: R = 1500 Ohm

1.3 Comparison

	Theory			PSpice		
	VR	VD	I	VR	VD	I
R = 220 Ohm	3.503	1.497	15.925	4.226	0.734	19.39
R = 1500 Ohm	4.161	0.839	2.774	4.317	0.683	2.878

2. Diode in a series

2.1 Theory calculation

According to the: Practical diode model

We have VD1 = 0.7223V

VD2 = 0.7223V

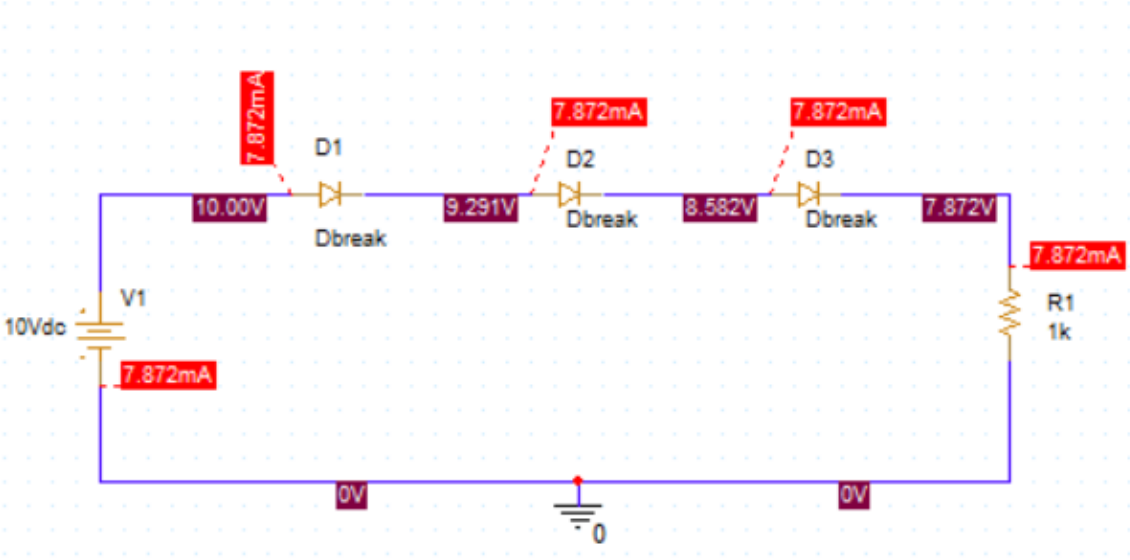
VD3 = 0.7223V

VR1 = 10 -0.7223*3 = 7.8331V

Formula to calculate I: (10 – 0.7223)/1000

I = 7.8331 mA

2.2 PSpice Simulation



2.3 Comparison

	VD1	VD2	VD3	VR1	I
Theory calculation	0.7223	0.7223	0.7223	7.8331	7.8331
PSpice Simulation	0.709	0.709	0.71	7.872	7.872

3. Circuit Analysis with Diode

3.1 Theory calculation

According to the practical diode mode: V1 -V2 = 0.7V

Students are proposed to construct the equations to determine the current across all the resistors.

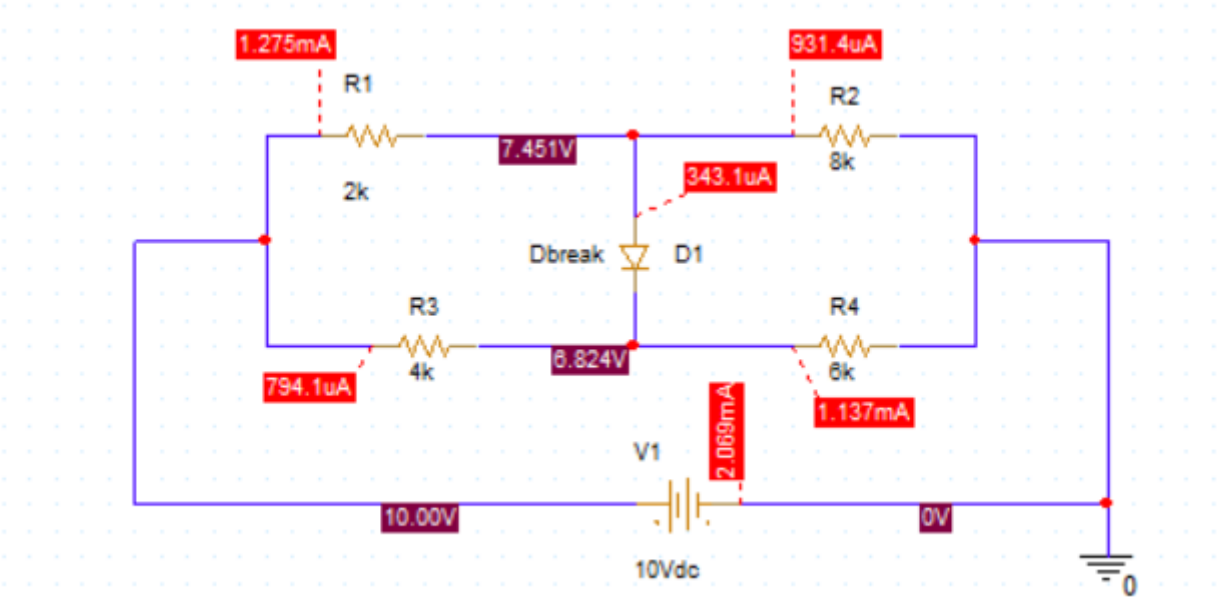
According to the kirchhoff's laws:

I1 + I3 = I2 + I4 <=> (10 – V1)/2k + (10 – V2)/4k = V1/8k + V2/6k

=> V1 = 7.48V, V2 = 6.78V

=> I1 = 1.26 mA ; I2 = 0.935 mA;I3 = 0.805m A;I4 = 1.13m A

3.2 PSpice Simulation



3.3 Comparison

	Theory Calculation						PSpice Simulation					
	IR1	IR2	IR3	IR4	V1	V2	IR1	IR2	IR3	IR4	V1	V2
V = 8V	0.98	0.755	0.665	0.89	6.04	5.34	0.996	0.75	0.653	0.898	6.008	5.398
V = 12V	1.54	1.115	0.945	1.37	8.92	8.22	1.553	1.112	0.935	1.377	8.894	8.26

4. Clamper Diode Circuit

4.1 Theory calculation

In this part, it is assumed that the practical diode model is used. Present your equations to calculate three different currents, including IR1, IR2, ID2 and the voltage VR2.

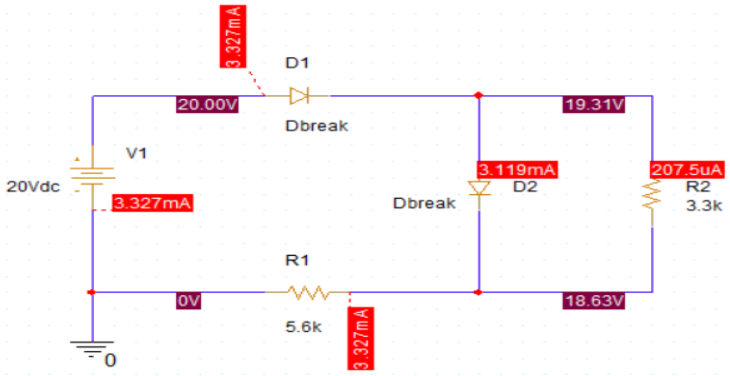
VR2 = VD2 = 0.7V

IR1 = (20 – 0.7*2)/5.6k = 3.32 mA

IR2 = 0.7/3.3k = 0.21m A

ID2 = IR1 − IR2 = 3.32−0.21 = 3.11m A

4.2 PSpice Simulation



4.3 Comparison

	Theory Simulation				PSpice Simulation			
	IR1	IR2	ID2	VR2	IR1	IR2	ID2	VR2
V = 12V	1,89mA	0,21mA	1,68mA	0.7V	1.903mA	0.202mA	1.701mA	0.67V
V = 20 V	3.32mA	0.21mA	3.11mA	0.7V	3.327mA	0.207mA	3.119mA	0.68V

5. Power switching circuit

5.1 Theory calculation

ID4 = 0A

VRL = 5−VD3 = 5−0.7 = 4.3V

ID3 = IRL = VRL/RL = 4.3/1k = 4.3 mA

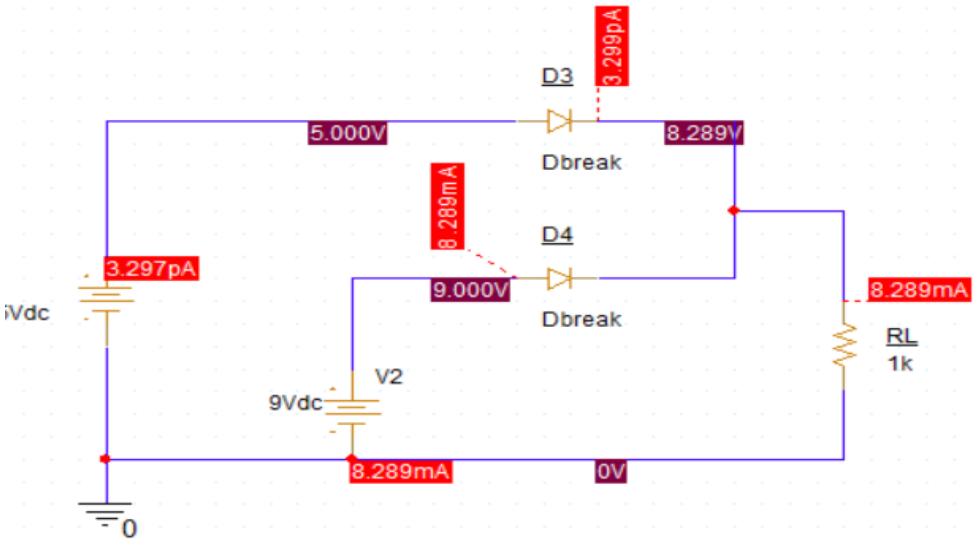
If only 9V:

ID3 = 0A

VRL = 9−VD4 = 9−0.7 = 8.3V

ID4 = IRL = VRL/RL = 8.3/1k = 8.3 mA

5.2 PSpice simulation



5.3 Comparison

Theory calculation				PSpice Simulation			
ID1	ID2	IRL	VRL	ID1	ID2	IRL	VRL
0A	8.3mA	8.3mA	8.3V	3.299pA	8.298mA	8.298mA	8.289V

6. Half-wave Rectifier

6.1 Theory calculation

Approximation: Diodes have Vf = 0.78V
Minimum Value of VR1 = 0V
Maximum Value of VR1 = V AMPL −VD1 = 22−0, 78 = 21.22V
Duration (millisecond) for a cycle of VR1 = 1/FREG = 1/50 = 20ms

6.2 PSpice simulation
Minimum Value of VR1 = 0V
Maximum Value of VR1 = 21.263V
Duration (millisecond) for a cycle of VR1 = 20ms
The tracking point can also be used directly on the simulation output windows, by the Toggle Cursor option on the toolbar. A Probe Cursor window is opened to update a tracking point.

7. Full-wave Rectifier
7.1 Theory calculation
Approximation: Diodes have Vf = 0.7V
VAB = Vin/10 = 22V
VCD = VAB −2∗0.7 = 20.6V
7.2 Simulation

8. Zener Diode as a Regulator
For theory calculation, students are supposed to provide equations for these values
IL = VZ/RL = 5/1.5k = 3.33mA
IS = (Vcc – VL)/Rs = (8-5)/200 = 15mA
IZ = IS − IL = 15−3.33 = 11.67m A
PRS =URS ∗ IRS = 3∗0.015 = 45mW
PZ =UZ ∗ IZ = 5∗0.01167 = 58.35mW
The results are summarized in the table bellow. (V in Volt; I in mA; P in mW)

	Theory Calculation						PSpice Simulation					
	IS	IL	VZ	VL	PRS	PZ	IS	IL	VZ	VL	PRS	PZ
Vcc = 8V	15	3.33	11.67	5	45	58.35	15.04	3.329	11.71	4.993	45.21	58.45
Vcc = 12V	35	3.33	31.67	5	245	158.35	34.96	3.339	31.62	5.009	244.4	158.4

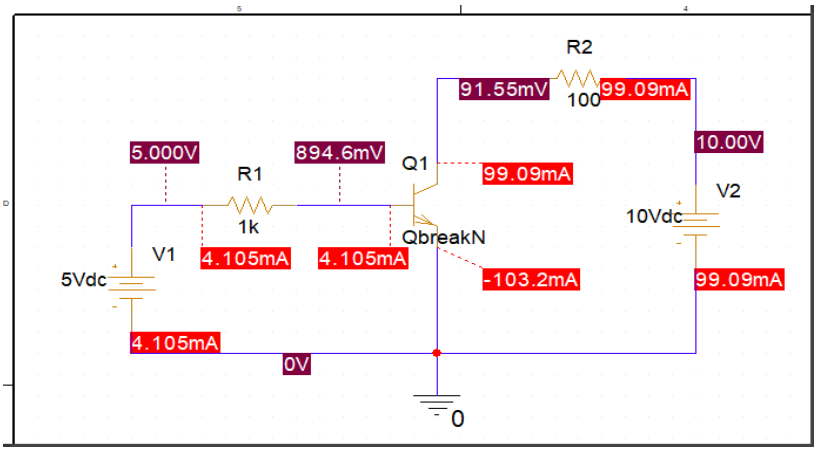
9. AC/DC Power Circuit Application
10. Exercise 8: AC/DC Power Circuit Application With LM2596_5P0_TRANS

LAB 3

3. Exercise and Report

3.1 BJT in Saturation Mode

Change the value of R1 to 1k and run the simulation again. Capture the simulation results explain the values of IB, IC, VCE. The default transistor gain is β = 100, and the saturated voltage VCE(Sat) = 0.65V and VBE = 0.7V.



The results in PSpice are explained as follows:

According to the Ohm law, IB = (VBB -VBE)/R1 = (5 – 0.7)/10^3 = 4.3 mA

It is assumed that the transistor is in linear (or active) mode, IC = β*IB = 100*4.3*10^(-3) = 0.43 A

Finally, in order to confirm the assumption above, VCE = VCC – IC*R2 = 10 – 0.43*100 = -33V

Since VCE < 0, our assumption is not correct. The transistor stays in saturation mode.

Therefore, IC is determined as follows:

IC = (VCC – VCE(Sat))/R2 = (10 – 0.65)/100 = 93.5 mA

3.2 DC sweep Simulation

The schematic in the first exersice with **R1 = 1k** is re-used in this exercise. However, a DC- Sweep simulation mode is performed with V1 is varied from 0V to 5V (0.1V for the step), as follows:

When the transistor becomes saturation, the value of V1 is: 1.9V

At this value, the value of IB is 1mA

And the value of IC(Sat) is 100mA

3.3 BJT used as Switch

For a given BJT circuit, determine R1 and R2 to have IC saturated at 50 mA. In this saturation mode, VCE(Sat) is 30mV.

The transistor stays in saturation mode:

R2 = (VCC – VCE(Sat))/IC(Sat) = (10 – 30*10^(-3))/(50*10^(-3)) = 199.4 Ohms

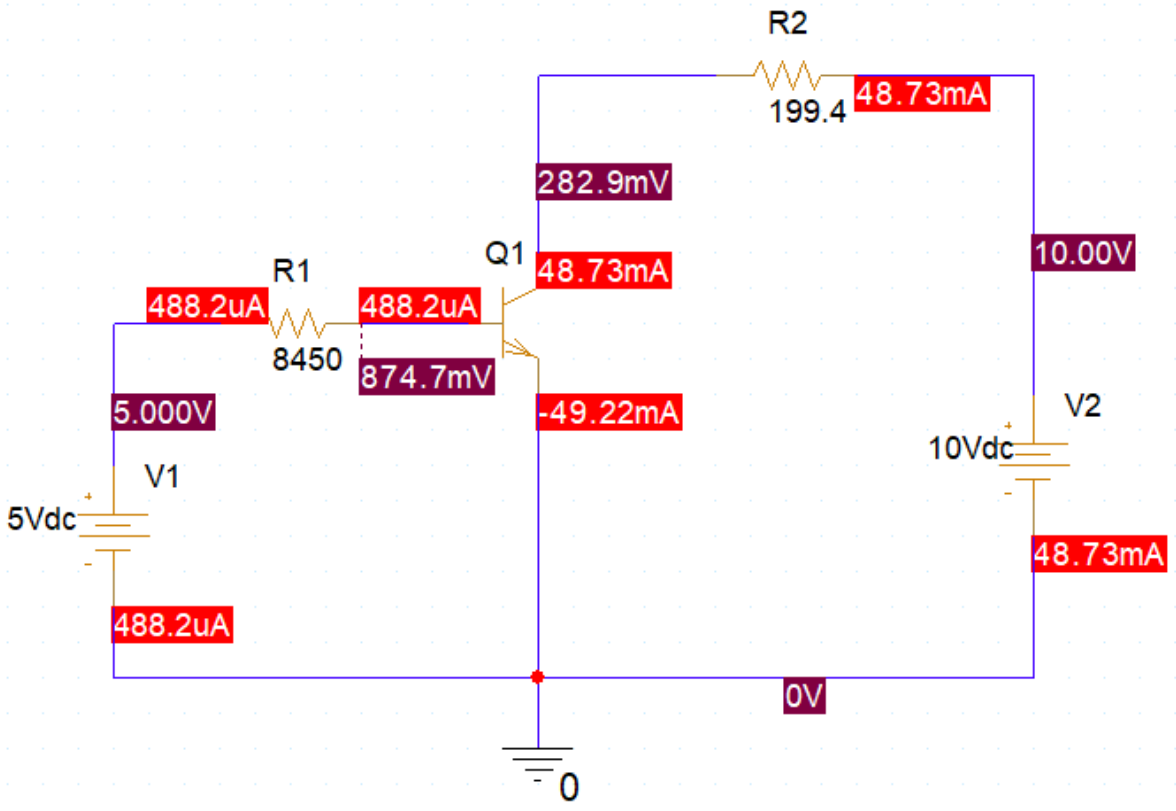
Therefore IB >= IC(Sat)/β

=> (VBB – VBE)/R1 > IC(Sat)/ β

=> (5 – 0.7)/R1 >= 50*10^(-3)/100

=> R1 <= 8600 Ohms

Selected resistor: 8450 Ohms



3.4 Drive a device with an NPN BJT

This exercise has a $5V$ logic output (the V_{ter} in Figure 1.6) that can source up to $10m\,A$ of current without a severe voltage drop and stand a maximum current of $20m\,A$. If the logic terminal sources a current larger than $20m\,A$, it would be damaged. Or, if it sources a current larger than $10m\,A$, the V_{ter} voltage will drop to less than $4V$. We should avoid this drop in many cases. However, this logic terminal has to be used to drive an electrical component with an equivalent internal resistance of 5 ohms (the LOAD in Figure 1.6) and requires a current of at least $300m\,A$ and not exceeding $500m\,A$ to function normally. Given that we have an NPN transistor with the current gain β equals 100, the maximum I_C

current is 400mA, and the barrier potential at the BE junction is $V_{BE} = 0.7V$, select a resistor available in the market to replace the resistor R_B revealed in Figure 1.6. to make the circuit function well. After that, perform a simulation to double-check your selection.

3.4.1 Theory calculations

According to the limits of the LOAD and the transistor, we have:

300 mA(min) < IC < 400 mA(max)

3 mA (min) < IB < 4 mA(max)

With IB(min) = 3 mA we have:

RB(max) = (V2 – VBE)/IB – R1 = (5 – 0.7)/0.003 – 100 = 1333.333 (Ohm)

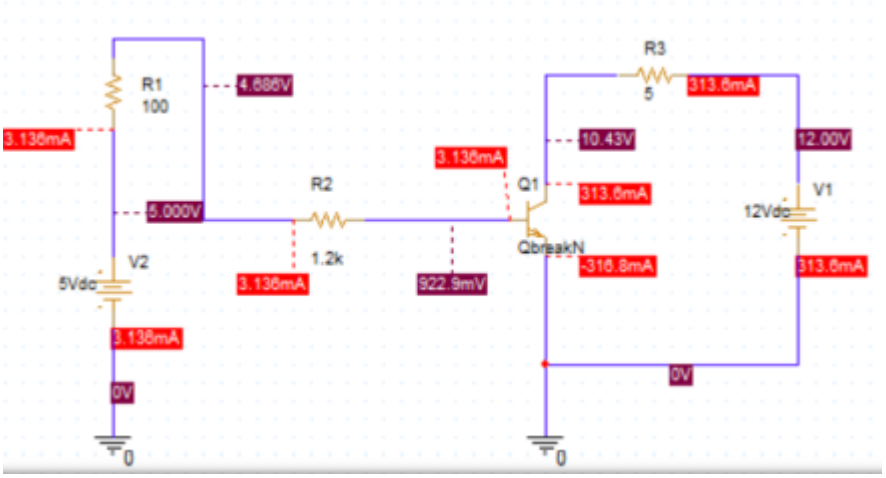
With IB (max) =4mA

RB (min) = (V2 – VBE)/IB – R1 = (5 – 0.7)/0.004 – 100 = 975 (Ohm)

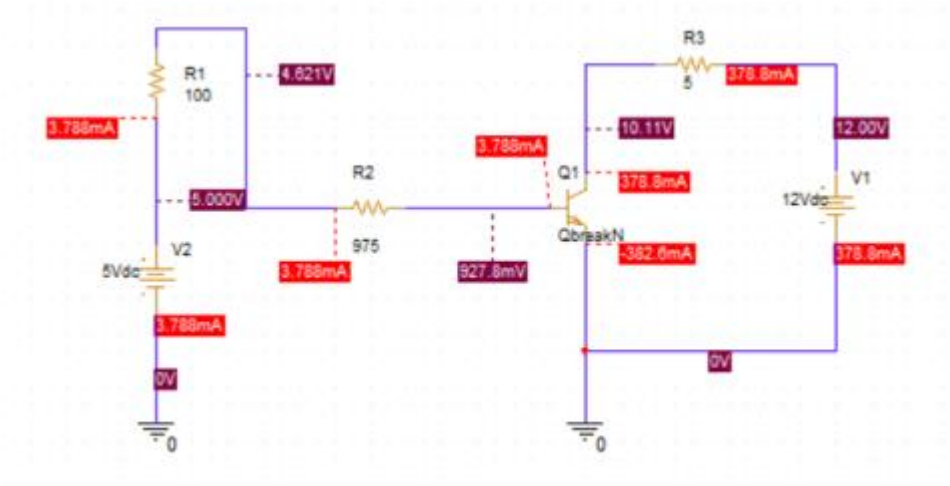
So: 975 Ohm (min) < RB < 1333.33 Ohm (max)

Selected RB: 1200 Ohm

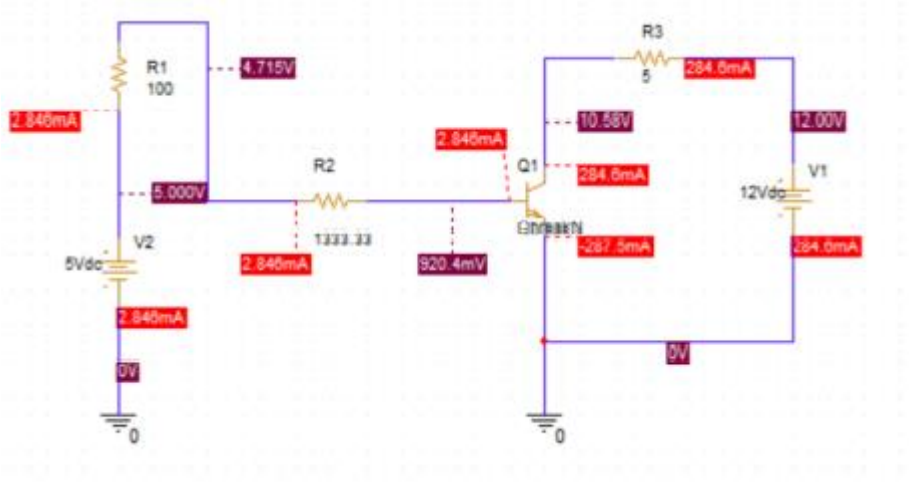
3.4.2 Simulation



RB = 1.2k Ohm



RB = 975 Ohm



RB = 1333.33

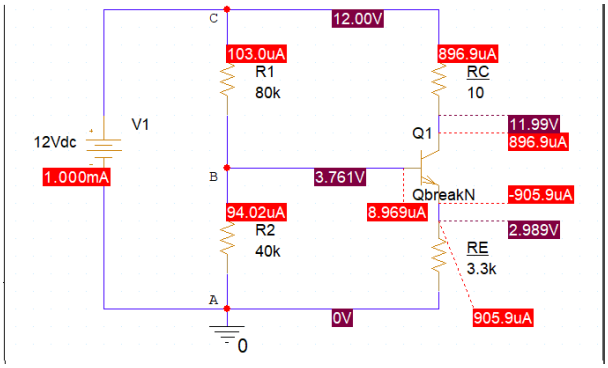
3.4.3 Compare

		Theory			PSpice		
	R_B	V_{BE}	I_B	I_C	V_{BE}	I_B	I_C
R_B (*min*)	975 Ohm	0.7V	4mA	400mA	0.927V	3.788mA	378.8mA
R_B (*max*)	1333.33 Ohm	0.7V	3mA	300mA	0.920V	2.846mA	284.6mA
R_B (*selected*)	1200 Ohm	0.7V	3.307mA	330.7mA	0.923V	3.136mA	313.6mA

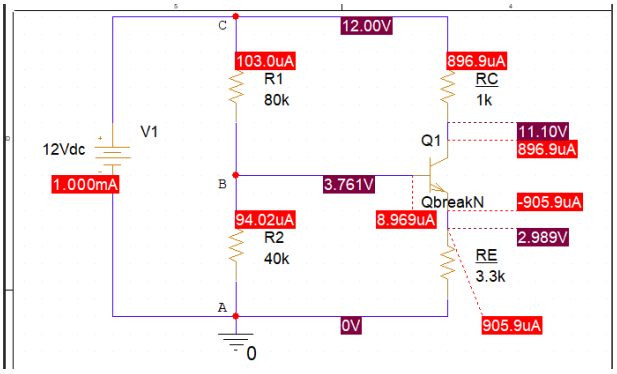
3.5 Simple bias configuration

The circuit given in Figure 1.10 is known as a simple kind of NPN bias configuration. First, students simulate the circuit with two values of RC, respectively 10 Ohms and 1k Ohms. Then, give your statement on the change of the current I_E and explain the phenomena.

Step 1: Simulate the circuit with R_C = 10 Ohms.



Step 2: Simulate the circuit with R_C = 1k Ohms.



3.5.1 Ciruit analysis

Conduct some theoretical calculation to explain for the phenomena you have observed from the simulation.

We can conduct some equations from the circuit as follow (assume the BJT is in active mode):

1. $I_C = \beta * I_B$
2. $I_E = I_C + I_B$
3. $I_1 = I_B + I_2$
4. $I_1 * R_1 + I_2 * R_2 = 12$
5. $I_2 * R_2 = V_{BE} + I_E * R_E$

Substitute equation (1) into equation (2) and we have a simul equation with 4 variables (I_1, I_2, I_B, I_E) which can be solved independently of R_C's value. Hence, the I_E's value doesn't change in both cases.

Check assumption: $V_{CE} = V_C - I_C * R_C$

- $R_C = 10Ohms : V_{CE} = 12 - 1.08 * 10^{-3} * 10 = 11.99V > V_{BE} = 0.7V$
- $R_C = 1kOhms : V_{CE} = 12 - 1.08 * 10^{-3} * 10^3 = 10.92V V_{BE} = 0.7V$

Thus, our assumption was correct.

3.6 PNP Circuit

Figure 1.11 shows a very typical PNP transistor circuit. Calculate I_B , I_E , and I_C then simulate the circuit to double-check your calculation. Assume the current gain β = 100.

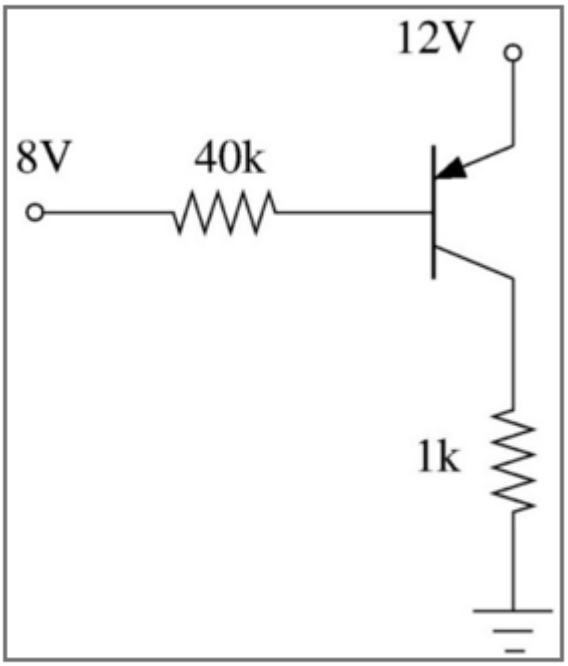


Figure 1.11: A PNP Circuit

3.6.1 Theoretical calculation

Assume the BJT is in active mode:

$V_{EB} = 0.7V$

The emitter-base KVL: $12 = V_{BE} + I_B * R_B + 8$

$\Longrightarrow I_B = 82.5\mu A$

$I_C = \beta * I_B = 100 * 82.5 * 10^{-6} = 8.25mA$

$= I_B + I_C = 8.33mA$

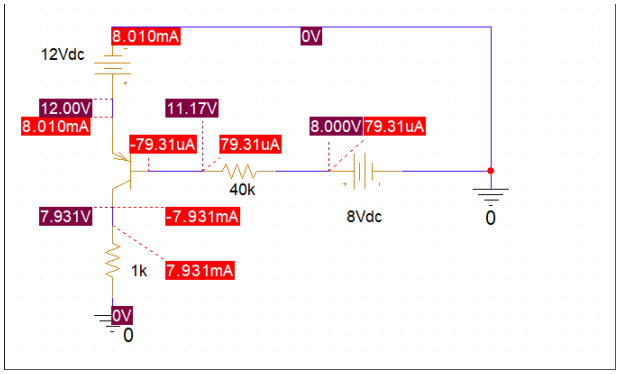
assumption:

The emitter-collector KVL: $12 = V_{EC} + I_C * R_C$

$\Longrightarrow V_{EC} = 3.75 > 0.7V$

Thus, our assumption was correct.

3.6.2 Simulation



3.6.3 Comparison

I_B (In theory) = 82.5 μA..... I_B (simulation) = 79.31 μA

I_C (In theory) = 8.25 mA..... I_C (simulation) = 7.931 mA

I_E (In theory) = 8.33 mA ..... I_E (simulation) = 8.01 mA

3.7 Circuit with NPN and PNP bipolar junction transistors

Give the circuit in Figure 1.12. Calculate the Voltage at all nodes and the current in all branches. Assume the current gain of both transistors is the same at β = 100. Then perform a simulation and compare the result with the theoretical calculation.

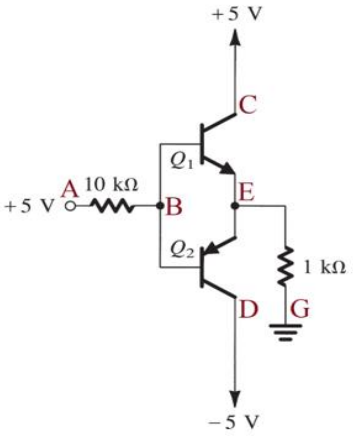


Figure 1.12: Circuit with NPN and PNP bipolar junction transistors

3.7.1 Theoretical calculation

We have $V_E < V_B$, therefore the transistor Q_2 is cut off

According to the KVL and Q_1's active mode, we have the following equation:

IBE (hereinafter called ID) = (5 – VBE)/(RAB + 101*REG) (1)

Solve (1) we have I_B = 38.74 μA

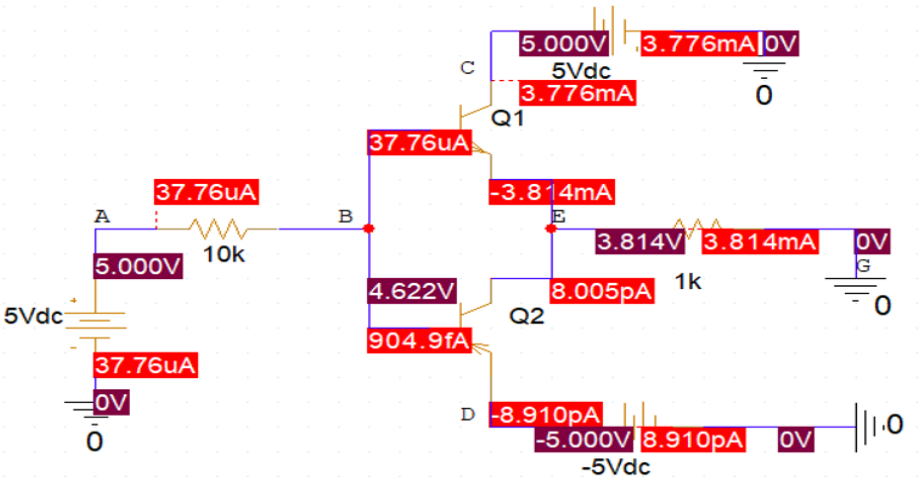
$I_C = \beta * I_B$ = 3.87 mA

$I_{EG} = I_B + I_C$ = 3.91 mA

$V_E = I_{EG} * R_E$ = 3.91 V

$V_B = 5 - I_B * R_{AB}$ = 4.61 V

3.7.2 Simulation



3.7.3 Comparison

I_B (In theory) = 38.74 µA ..... I_B (simulation) = 37.76 µA .....

I_C (In theory) = 3.87 mA. ..... I_C (simulation) = 3.776 mA .....

I_{EG} (In theory) = 3.91 mA ..... I_{EG} (simulation) = 3.814 mA .....

V_E (In theory) = 3.91 V ..... V_E (simulation) = 3.814 V .....

V_B (In theory) = 4.61 V ..... V_B (simulation) = 4.622 V .....

3.8 NPN Circuit with E resistance

3.8.1 Theoretical calculation

I_B = 23.4 µA

I_C = 2.34 mA

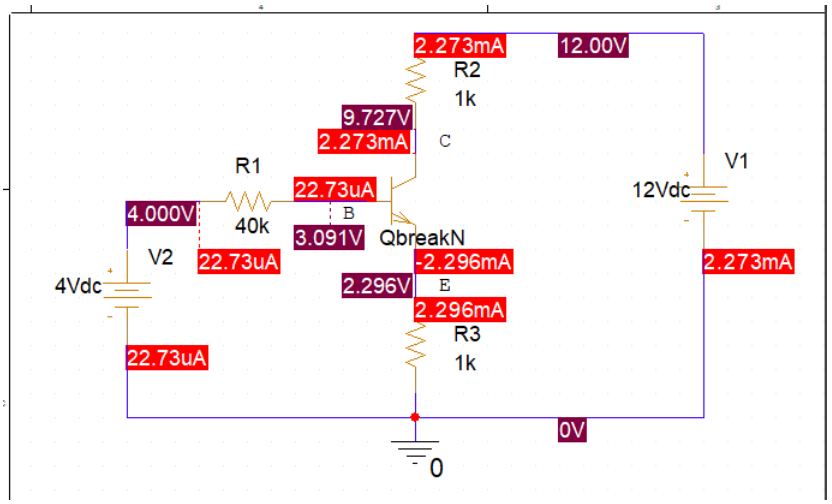
I_E = 2.36 mA

Check assumption: $V_{CE} = 12 - I_C * R_2 - I_E * R_3 = 7.29 > 0.7 \Rightarrow$ Assumption is correct.

$V_E = I_E * R_3$ = 2.36 V

$V_C = 12 - I_C * R_2 = 9.66\ \text{V}$.

3.8.2 Simulation



3.9 Darlington circuit

3.9.1 Theoretical calculation

Explanations, formulas, and equations are expected rather than only results.

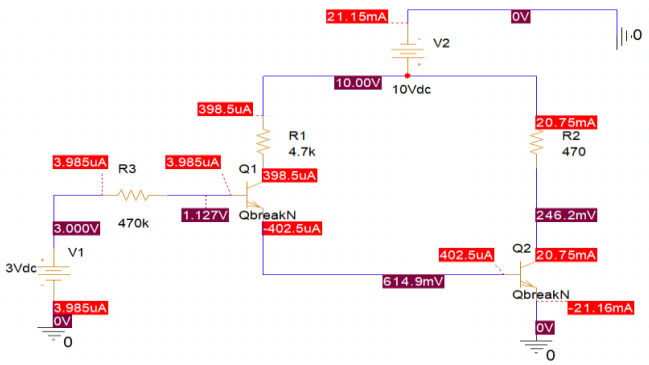
$I_{BE} = (\beta + 1) * I_{X\ B} = 101 * ((3–0.7–0.7)/470k) = 0{,}343\ (\text{mA})$

$I_{AC} = \beta * I_{X\,B} = 100 * (3–0.7 - 0.7)/470k = 0.34\ (\text{mA}) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots$

$I_{AL} = \beta * I_{BE} = 100 * 0.343 = 34.3\ (\text{mA}) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots$

$I_{AL} / I_{BE} = 100$

3.9.2 Simulation



LAB 4