Shane O'Donnell Lab F

Introduction

This Lab focuses on the simulation and implementation of sequential logic circuits using structural Verilog on the basys 3 board. Similarly to the other labs, smaller modules were assembled in Vivado to fulfil a greater logical truth table. In this instance the modules used included D Flip-Flops (DFFs), a seven segment display controller, a clock divider for managing the clock signal and a top module to implement it all as a Linear Feedback Shift Register (LFSR). Using vivado these modules were bench tested and then programmed on to the basys 3 board.

Part A

The aim of this section was to create a test bench that uses the clock and reset signals to observe how DFFs respond under different conditions. The following conditions were explored:

Positive Edge Triggered with Asynchronous reset

In this setup the output 'g' updates to match the input 'd' on every rising edge of the clock while the reset signal was inactive. If the reset signal becomes active (logic high), the output q is immediately set to 0 regardless of clock signal.

Negative Edge Triggered with Asynchronous reset

The configuration here mirrors the behaviour of the first except transitions occur on the falling edge of the clock. During regular operation the q follows d at each high to low clock transition. When reset is high, q is instantly cleared to 0 independent of the clock.

Negative Edge Triggered (Synchronous Only)

In the third case the output responds to the falling edge of the clock without any asynchronous reset mechanism. The output q simply adopts the value of d at each falling edge and retains that value until the next falling edge occurs.

Part B: Practical use of DFF

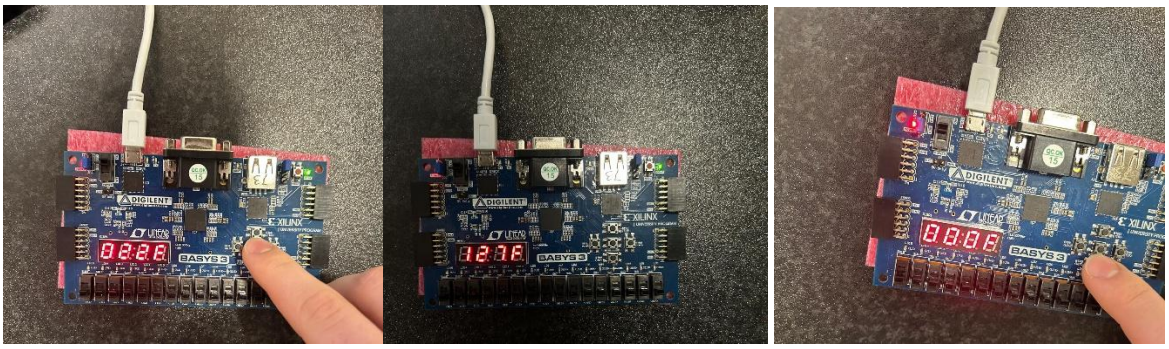
The goal of this section was to construct an 8-bit counter using DFFs that could be controlled using push buttons on the basys 3 board. The counter value was displayed using the on board seven segment display, along with the Letter 'F' to imply the value was representing degrees Fahrenheit. The 5 buttons on the board were used to change the value displayed, with the directional inputs incrementing and decrementing the value, and the centre button setting it to 22.

To achieve this, eight individual DFF modules were instantiated with each storing one bit of the 8 bit value which represented a temperature value ranging from 0 to 127. A debouncer module was used to clean up the mechanical noise from button presses. Without this module the button presses would be detected more than once per press, causing the

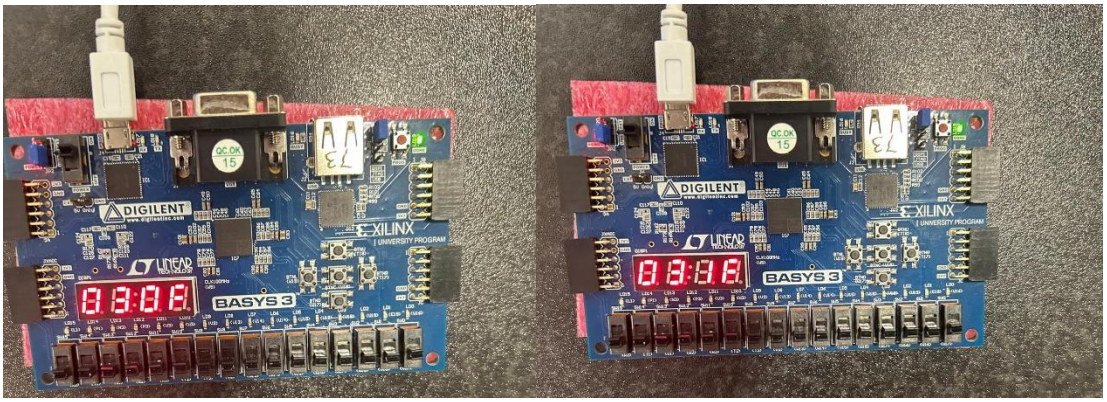
incrementation features to never only incrementing the value by one as intended. The sevenseg module was in charge of converting the binary value into a form that made it compatible with the seven segment display.

The buttons which controlled the counter had 3 functions. As said before the middle of the 5 would set the value displayed on the display to 22. The bottom and left buttons would decrease the current value by one, and the remaining buttons did the opposite. This approach demonstrated how a set of DFFs can be effectively used for state recognition in a sequential circuit.

The following images show the board displaying the default, maximum and minimum value of the programme. 22 F, 127 F and 0F repsectively.

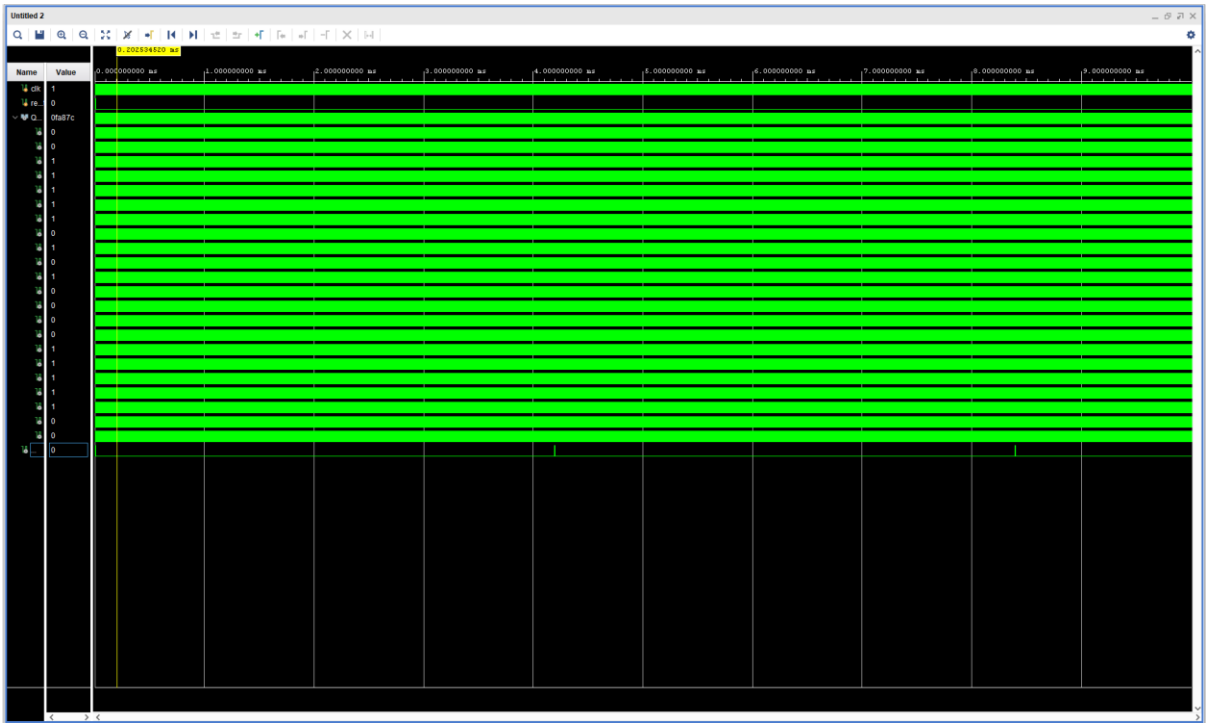


seen below is the board diplaying 30F and then 31F, as further example of the programm's increment and decrement features.

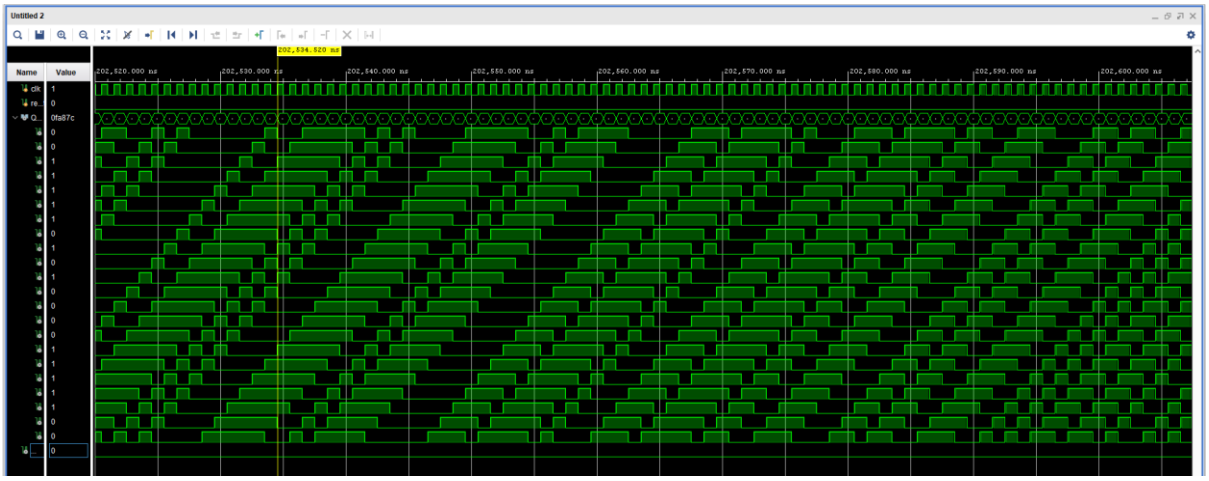


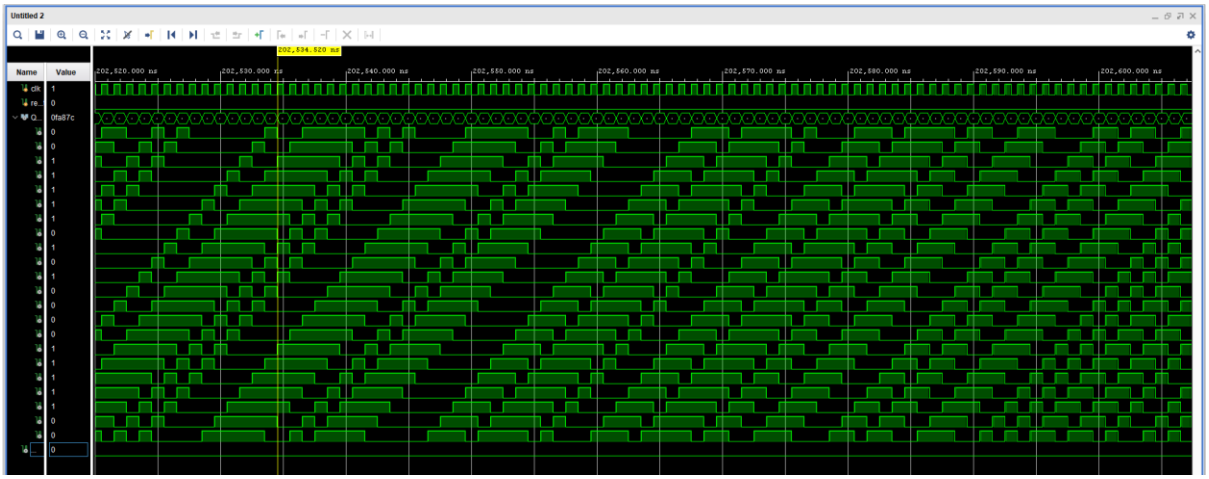
Part C: LFSR Implementation

The goal for part C was to implement a 22 bit Linear Feedback Shift register (LSFR) in Verilog. Including a testbench to validate the functionality and track the completion of a full sequence using a max_tick signal. The seed value was created using a bitwise XOR operation between the lab board number (73) and the last 3 digits of my student number (731). The LFSR was designed with feedback taps at bit positions 20 and 21based on the max length configuration from the lectures. The feedback loop used XNOR logic with each bit shifting once per clock cycle. The testbench simulated a clock signal with a 1ns period and held the reset signal for the first 10 cycles.



This image shows the max tick transmissions when Q reaches the seed again. The following two are cropped and zoomed images of the same waveform to clarify wha is actually happening.

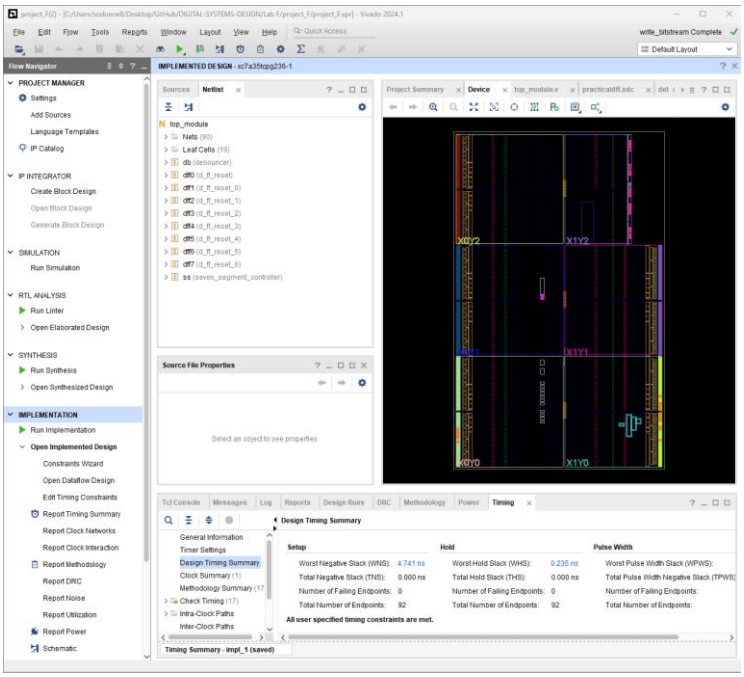


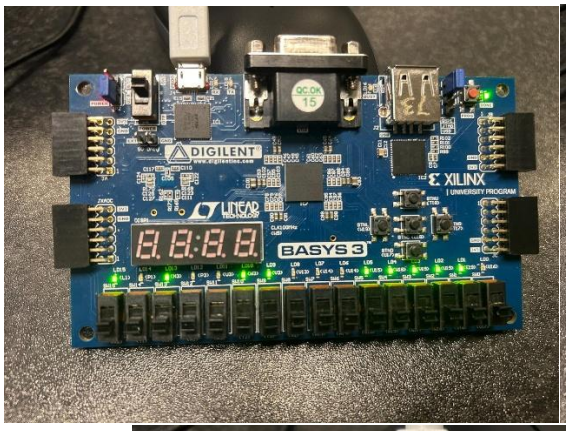


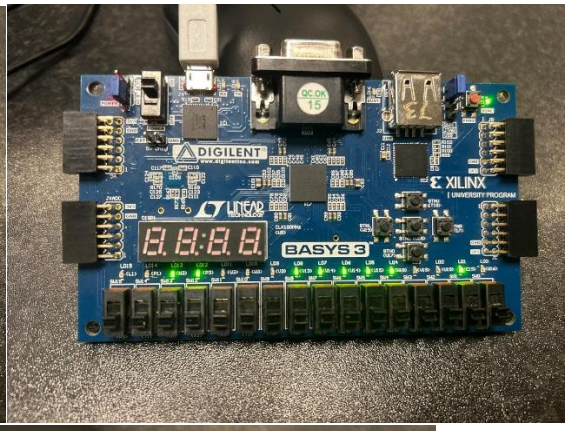
Part D: LFSR - Target to Board

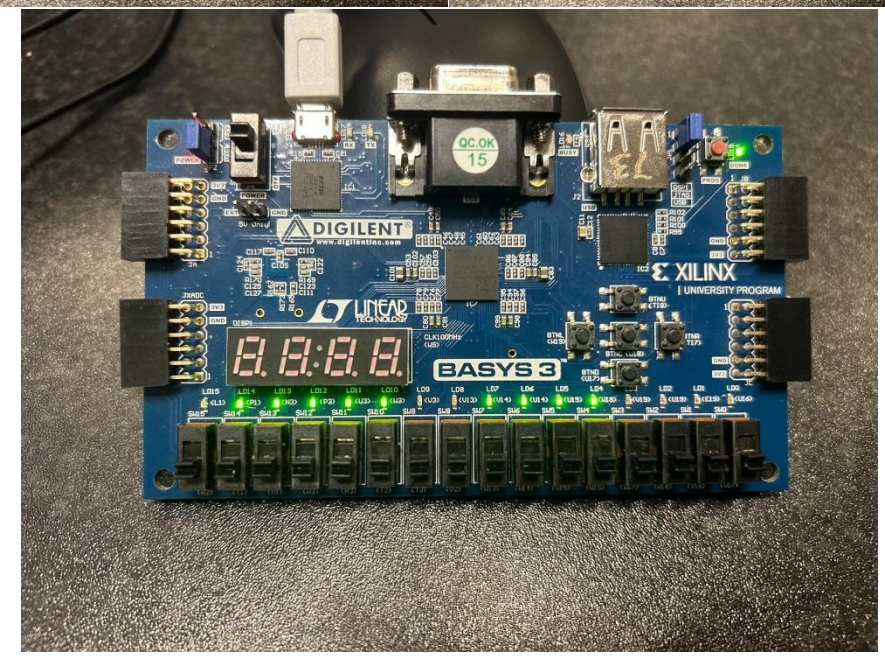
The goal for part D was to implent the LFSR from part C on the basys 3 board to visualize the operation in a form that is easy to understand than the waveform generator. To this the registers were mapped to the LED array on the board and a clock divider was used to reduce the system clock to a 1HZ signal. This slowd-down clock was then used to drive the LFSR. The top module made use of the aformentionmed clcok divider and the LFSR module from part C. A constraints file (.xdc) had to be created to map the verilog code to the LEDs on the board and the reset switch.

The following is the implemented design for part D. Followed by a demo of the progressing LEDs.









Conclusions

This Lab demonstrates how sequential logic circuits can be designed, simulated and implemented in hardware using structual Verilog. Through the various parts, key concepts such as D Flip-Flops, clock & reset behaviour, state storage and feedback logic were explored both in simulation and on the basys 3 board.

In Part A the behaviour of the DFFS under different clock edge and reset conditions was analyzed to highlight the differences between synchronous and asychronous resets. Part B extended this by using DFFs to create a functional counter that responds to physical button preses. Part C introduced the linear feedback shift registers or LFSRs and highlighted their psuedo random behaviour and the importance of proper seeding. Lastly part D saw the implementation of the LSFR on the physical board with a clock divider module to slow down the operations from part C, so it could be clearly displayed on the LED array.

As a whole the lab demonstrated how the modular systems are built. The design process of structural verilog from simulated test benches to practical implementation of physical FPGA boards.