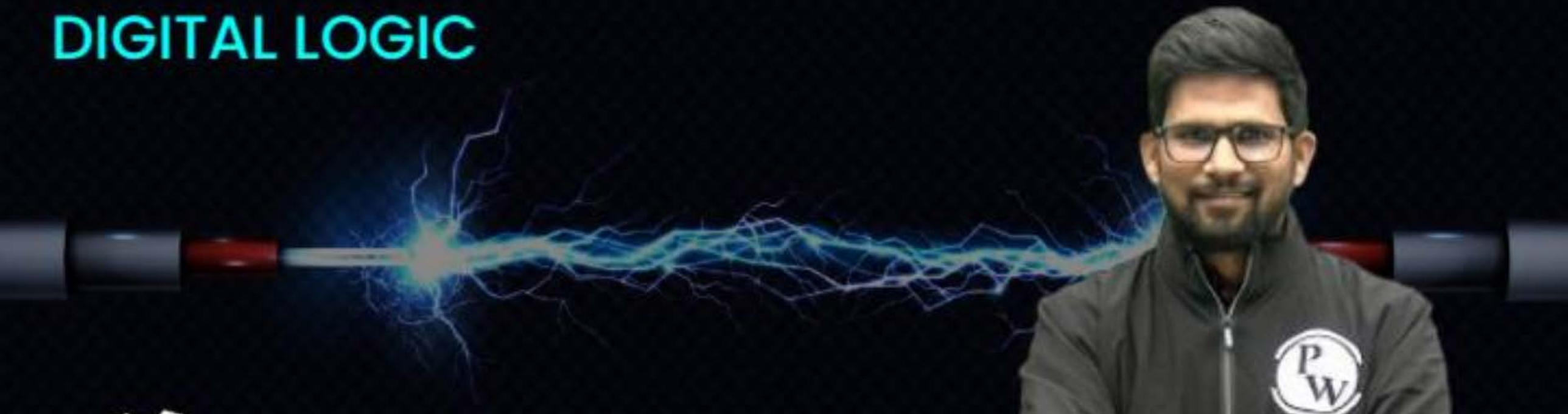
COMPUTER SCIENCE & IT

DIGITAL LOGIC



Lecture No: 10

Sequential Circuit

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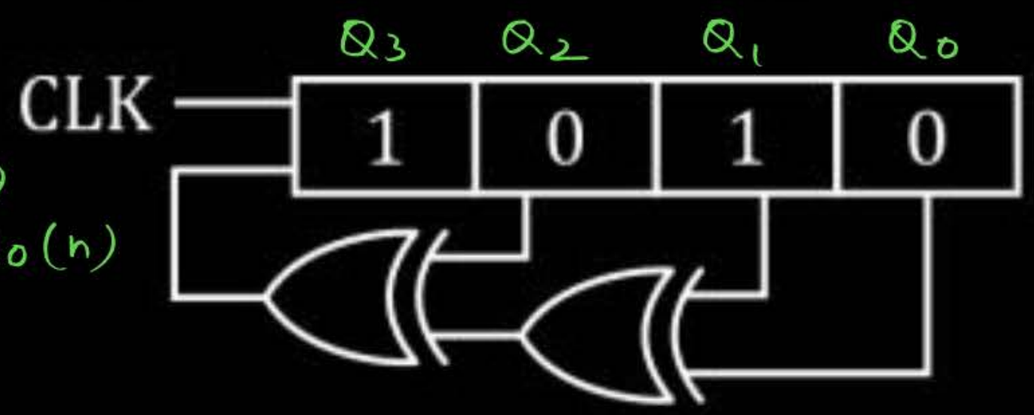
Recap of Previous Lecture

- Ring Counter
- Johnson Counter
- Shift Register

Question Discussion

Question

A four bit SIPO register is shown in fig. with starting state $(1010)_2$.



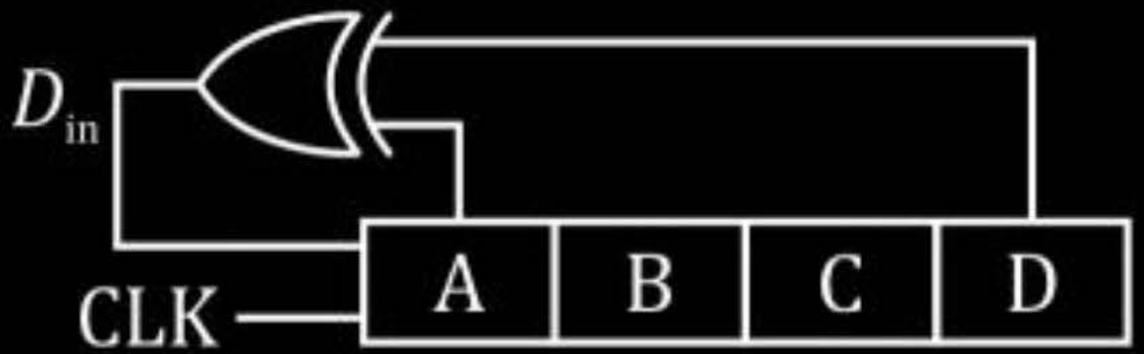
$Q_3(n+1) = Q_2(n) \oplus Q_1(n) \oplus Q_0(n)$

	Q_3	Q_2	Q_1	Q_0
	1	0	1	0
1	1	1	0	1
2	0	1	1	0
3	0	0	1	1
4	0	0	0	1
5th	1	0	0	0
6th	0	1	0	0
7th	1	0	1	0

After application of how many clock pulses content of SIPO will again will be $(1010)_2$ 7

Question

A 4-bit shift register circuit configured the right shift operation i.e. D_{in} – A, A – B, B – C, C – D is shown. If the present state of shift register is ABCD = $(1101)_2$, then the no. of clock cycle required to reach the state ABCD = $(1111)_2$ 10.



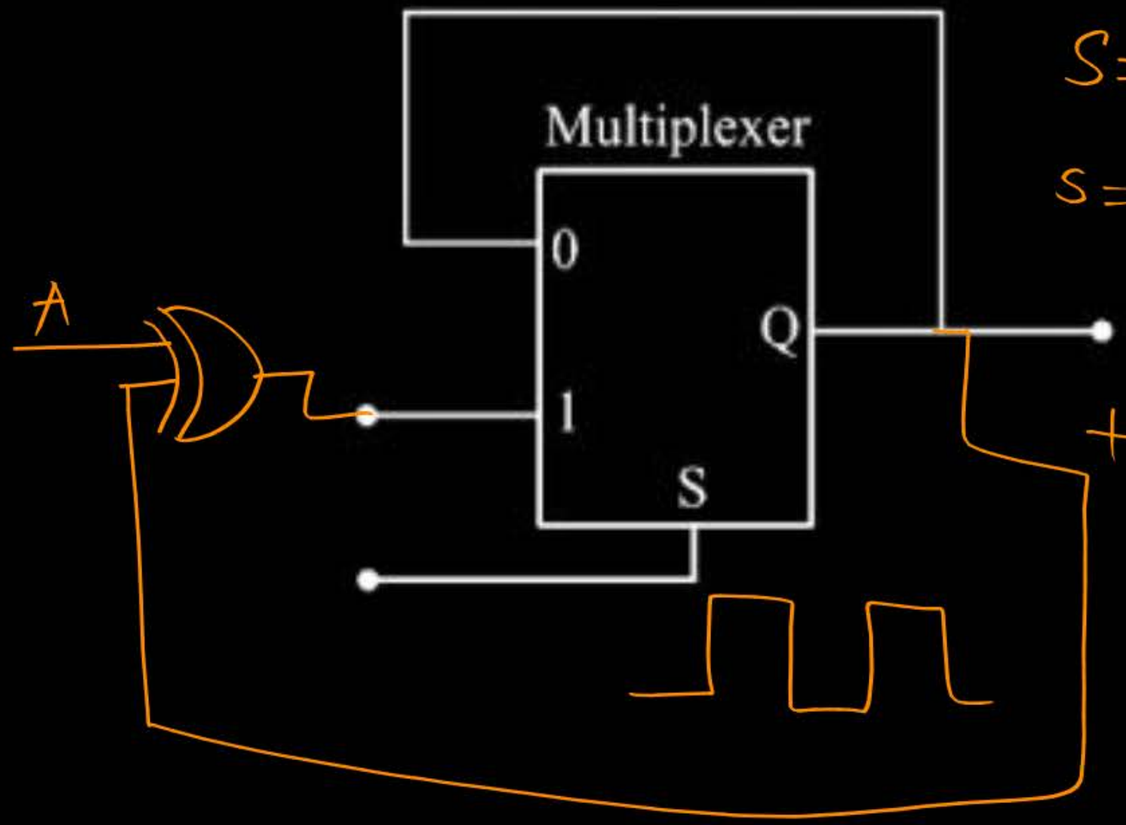
	1101	0111
1st	0110	1011
2nd	0011	0101
3rd	1001	1010
4th	0100	1101
5th	0010	
6th	0001	
7th	1000	
8th	1100	
9th	1110	
10th	1111	

[MCQ]

The output of a 2-input multiplexer is connected back to one of its inputs as shown in the figure.

Match the function equivalence of this circuit to one of the following options.

[GATE-2023-CS: 1M]



$S=0 \quad Q(n+1)=Q(n)$

$S=1 \quad Q(n+1)=A$

D-ff → level triggered

+ve level triggered D-ff

(A) D Flip-flop

(B) D Latch

(C) Half-adder

(D) Demultiplexer

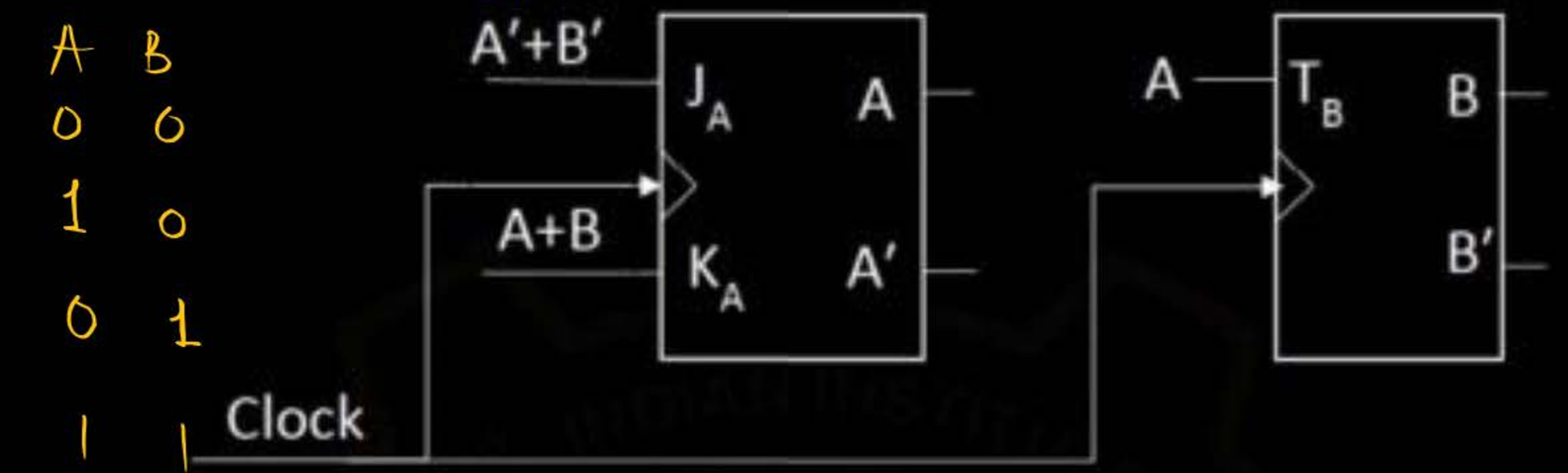
#Q. Given below is the diagram of a synchronous sequential circuit with one J-K flip-flop and one T flip-flop with their outputs denoted as A and B respectively, with $J_A = (A' + B')$, $K_A = (A + B)$, and $T_B = A$. Starting from the initial state (AB = 00), the sequence of states (AB) visited by the circuit is

$$A(n+1) = \left[\bar{A}(n) + \bar{B}(n)\right]\bar{A}(n) + \bar{A}(n)\cdot\bar{B}(n)\cdot A(n)$$

$$A(n+1) = \bar{A}(n)$$

$$B(n+1) = A(n) \oplus B(n)$$

A	B
0	0
1	0
0	1
1	1
0	0



A. ~~00 – 01 – 10 – 11 – 00~~

B. 00 – 10 – 01 – 11 – 00

C. ~~00 – 10 – 11 – 01 – 00~~

D. ~~00 – 01 – 11 – 00~~

[MCQ]

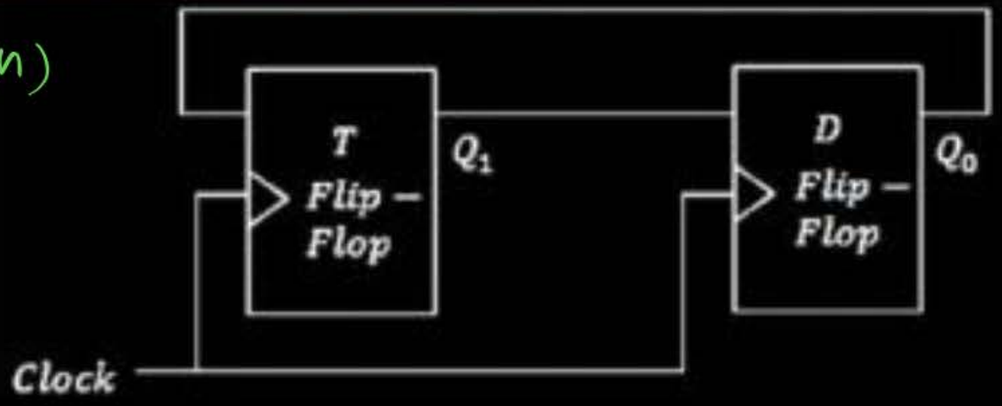
Consider a combination of T and D flip-flops connected as shown below. The output of the D flip-flop is connected to the input of the T flip-flop and the output of the T flip-flop is connected to the input of the D flip-flop.

Initially, both Q_0 and Q_1 are set to 1 (before the 1st clock cycle). The outputs

[GATE-2017-CS: 1M]

$Q_1(n+1) = Q_0(n) \oplus Q_1(n)$

$Q_0(n+1) = D_0 = Q_1(n)$



$Q_1 Q_0$

1 1

0 1

1 0

1 1

0 1

(A) Q_1Q_0 after the 3rd cycle are 11 and after the 4th cycle are 00 respectively

(B) Q_1Q_0 after the 3rd cycle are 11 and after the 4th cycle are 01 respectively

(C) Q_1Q_0 after the 3rd cycle are 00 and after the 4th cycle are 11 respectively

(D) Q_1Q_0 after the 3rd cycle are 01 and after the 4th cycle are 01 respectively.

[MCQ]

A positive edge-triggered D flip-flop is connected to a positive edge-triggered JK flip-flop as follows. The Q output of the D flip-flop is connected to both the J and K inputs of the JK flip-flop, while the Q output of the JK flip-flop is connected to the input of the D flip-flop. Initially, the output of the D flip-flop is set to logic one and the output of the JK flip-flop is cleared. Which one of the following is the bit sequence (including the initial state) generated at the Q output of the JK flip-flop when the flip-flops are connected to a free-running common clock? Assume that J = K = 1 is the toggle mode and J = K = 0 is the state-holding mode of the JK flip-flop. Both the flip-flops have non-zero propagation delays. [GATE-2015-CS: 1M]

$D - Q_0(n+1) = D_0 = Q_1(n)$

$JK - Q_1(n+1) = Q_0(n) \oplus Q_1(n)$

Q_1	Q_0	J
0	1	1
1	0	1
1	1	1
0	1	1

(A) 0110110...

(B) 0100100...

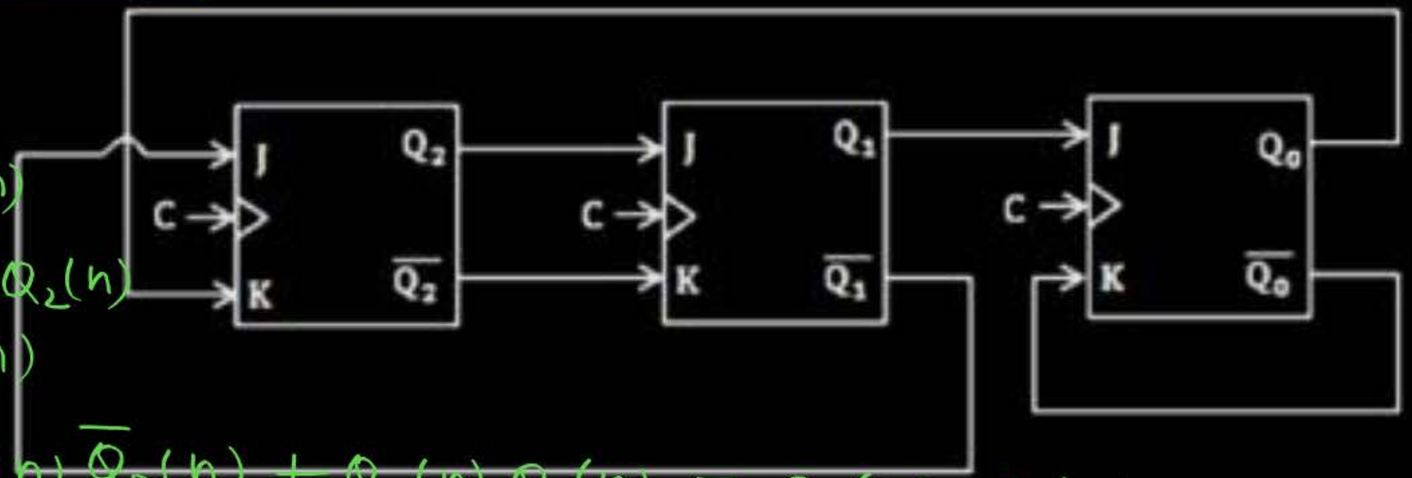
(C) 011101110...

(D) 011001100...

[MCQ]

The above synchronous sequential circuit built using JK flip-flops is initialized with $Q_2Q_1Q_0 = 000$. The state sequence for this circuit for the next 3 clock cycles is :

[GATE-2014-CS: 1M]



$Q_2(n+1)$
$= \overline{Q_1}(n)\,\overline{Q_2}(n) + \overline{Q_0}(n)\cdot Q_2(n)$

$Q_1(n+1) = Q_2(n)$

$Q_0(n+1) = Q_1(n)\,\overline{Q_0}(n) + Q_0(n)\cdot Q_0(n) = Q_0(n) + Q_1(n)$

Q_2	Q_1	Q_0
0	0	0
1	0	0
1	1	0
1	1	1

A. 001, 010, 011

B. 111, 110, 101

C. 100, 110, 111

D. 100, 011, 001

[MCQ]

The minimum number of D flip-flops needed to design a mod-258 counter is :

[GATE-2011-CS: 1M]

A 9

B 8

C 512

D 258

[MCQ]

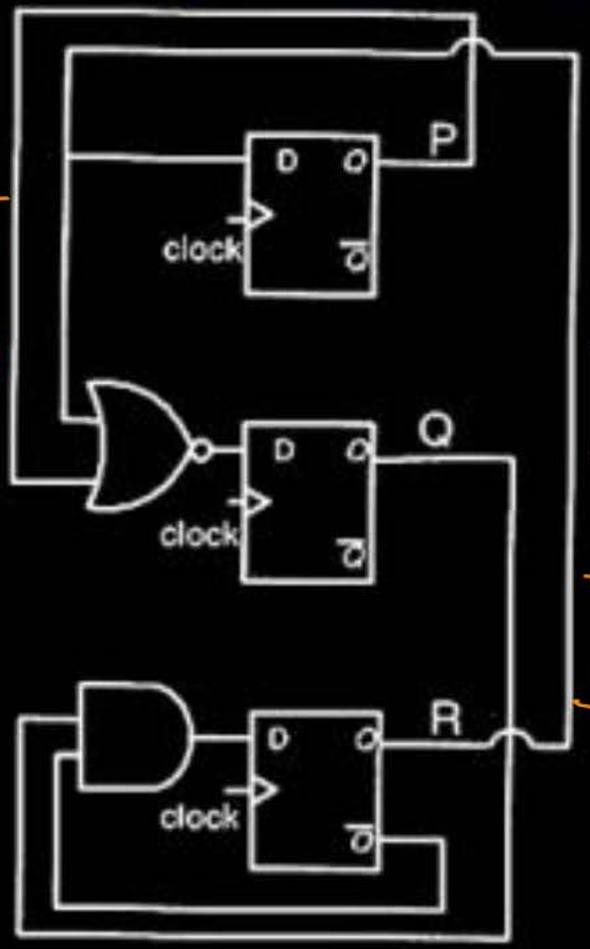
Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration. If all the flip-flops were reset to 0 at power on, what is the total number of distinct outputs (states) represented by PQR generated by the counter ?

[GATE-2011-CS: 1M]

$P(n+1) = D_P = R(n)$

$Q(n+1) = D_Q = \overline{P(n)+R(n)}$

$R(n+1) = D_R = Q(n) \cdot \overline{R}(n)$



PQR

0 0 0

0 1 0

0 1 1

1 0 0

0 0 0

MOD-4

A 3

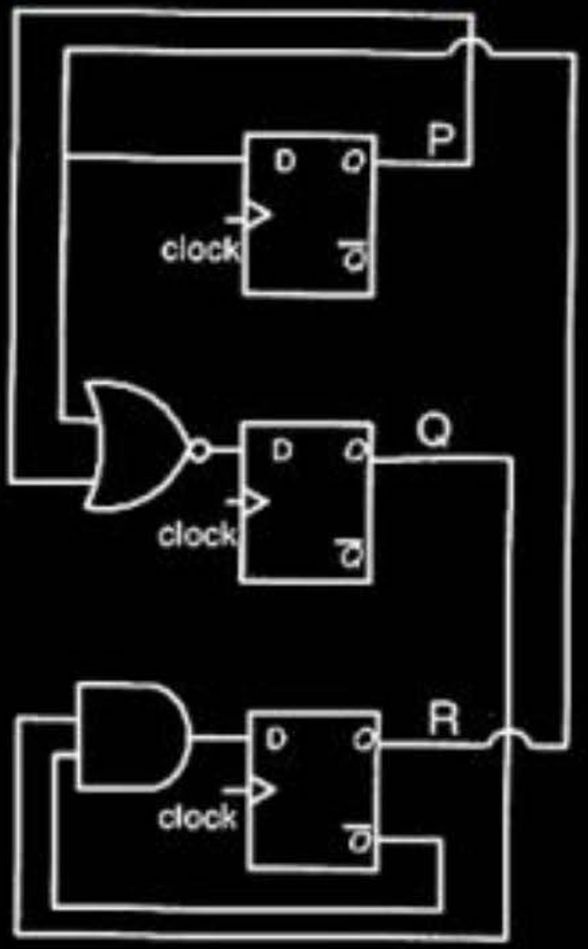
B 4

C 5

D 6

[MCQ]

Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration. If at some instance prior to the occurrence of the clock edge, P, Q and R have a value 0, 1 and 0 respectively, what shall be the value of PQR after the clock edge? [GATE-2011-CS: 1M]



P Q R
0 1 0
0 1 1

A 000

B 001

C 010

D 011

[MCQ]

Consider a sequential digital circuit consisting of T flip-flops and D flip-flops as shown in the figure. CLKIN is the clock input to the circuit. At the beginning, Q1, Q2 and Q3 have values 0, 1 and 1, respectively.

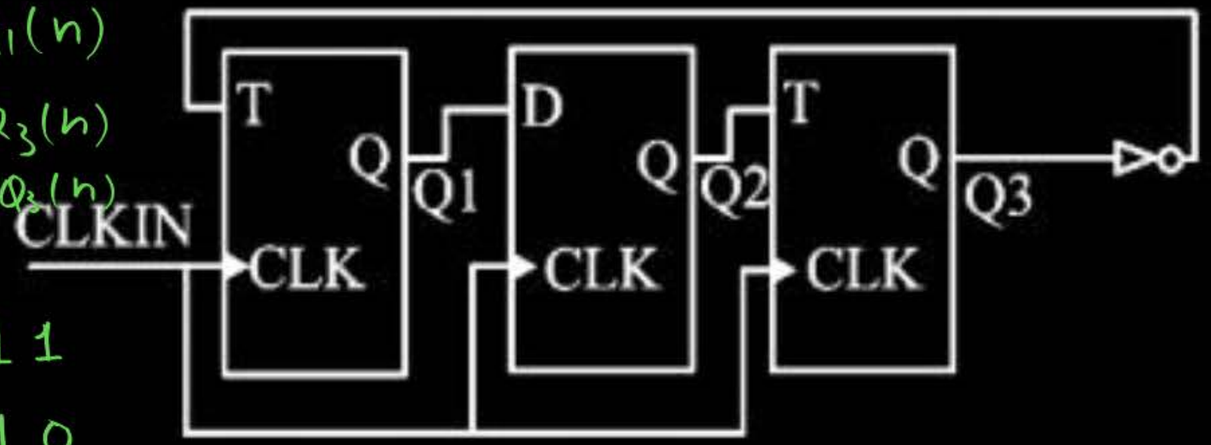
Which one of the given values of (Q1, Q2, Q3) can NEVER be obtained with this digital circuit? [GATE-2023-CS: 2M]

$Q_1(n+1) = \overline{Q_3}(n) \oplus Q_1(n) = Q_1(n) \odot Q_3(n)$

$Q_2(n+1) = D_2 = Q_1(n)$

$Q_3(n+1) = T_3 \oplus Q_3(n)$

$= Q_2(n) \oplus Q_3(n)$



$Q_1 Q_2 Q_3$

0 1 1

0 0 0

1 0 0

0 1 0

1 0 1

1 1 1

1 1 0

0 1 1

A. (0, 0, 1)

B. (1, 0, 0)

C. (1, 0, 1)

D. (1, 1, 1)

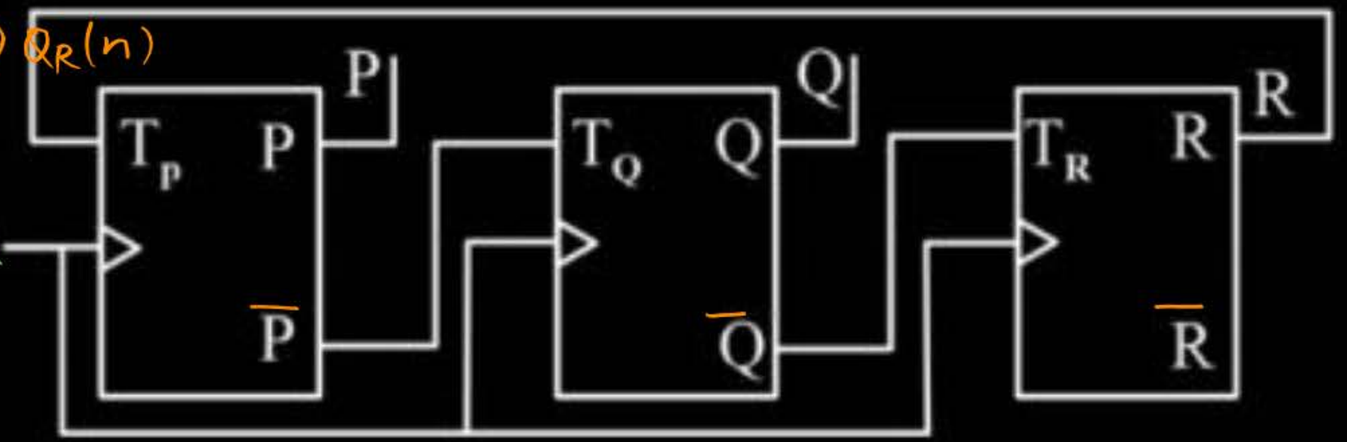
[MCQ]

Consider a 3-bit counter, designed using T flip-flops, as shown below. Assuming the initial state of the counter given by PQR as 000. What are the next three states ? [GATE-2021-CS: 1M]

$Q_P(n+1) = Q_R(n) \oplus Q_P(n)$

$Q_Q(n+1) = Q_P(n) \odot Q_Q(n)$

$Q_R(n+1) = Q_Q \odot Q_R(n)$



P Q R

0 0 0

↓ 0 1 1

↓ 1 0 1

↓ 0 0 0

(A) 011,101,000

(B) ~~001,010,111~~

(C) 011,101,111

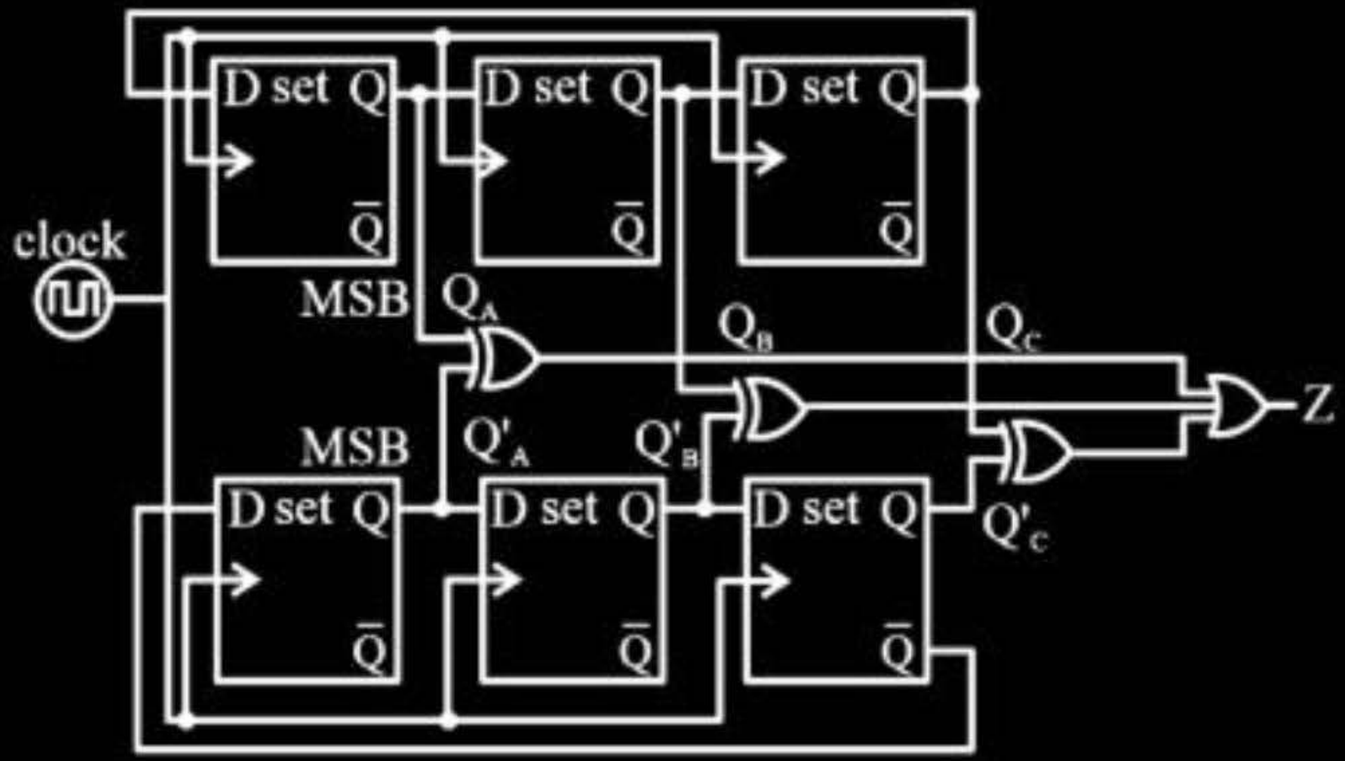
(D) ~~001,010,000~~

#Q. For the synchronous sequential circuit shown below, the output Z is zero for the initial conditions

$$Q_A Q_B Q_C = Q'_A Q'_B Q'_C = 100$$

The minimum number of clock cycles after which the output z would again become zero is _____.

H.W



[NAT]

The minimum number of JK flip-flops required to construct a synchronous counter with the count sequence (0,0,1,1,2,2,3,3,0,0....)is. [GATE-2021-CS: 2M]

0 – 0 – 1 – 1 – 2 – 2 – 3 – 3 MOD = 8

Q_2	Q_1	Q_0	
0	0	0	0
1	0	0	4
0	0	1	1
1	0	1	5
0	1	0	2
1	1	0	6
0	1	1	3
1	1	1	7

- 0 – 0 – 1 – 1 – 1 – 2 – 2 – 3. MOD = 8

Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	1	0	0
0	0	0	1
0	1	0	1
1	0	0	1
0	0	1	0
0	1	1	0
0	0	1	1

- 0 – 1 – 2 – 0 – 1 – 3 – 0 – 1 – 4 – 0 – 1 – 5 – 0 – 1 – 2 – 3

no. of ff = 6

MOD = 16

$Q_2 Q_1 Q_0$

1 0 1

3 extra bits for 5 different '0's or 5 different 1's

[MCQ]

The next state table of a 2-bit saturating up-counter is given below.
The counter is built as a synchronous sequential circuit using T flip-flops.
The expressions for T_1 and T_0 are [GATE-2017-CS: 1M]

0 – 1 – 2 – 3 – 3

Q_1	Q_0	Q_1^+	Q_0^+
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	1

T_1	T_0
0	1
1	1
0	1
0	0

(A) $T_1 = Q_1Q_0, T_0 = \overline{Q_1} + \overline{Q_0}$

(B) $T_1 = \overline{Q_1}Q_0, T_0 = \overline{Q_1} + \overline{Q_0}$

(C) $T_1 = Q_1 + Q_0, T_0 = \overline{Q_1} + \overline{Q_0}$

(D) $T_1 = \overline{Q_1}Q_0, T_0 = Q_1 + Q_0$

$T_1[Q_1, Q_0] = \Sigma(1) = \overline{Q_1}Q_0$

$T_0[Q_1, Q_0] = \Sigma 0,1,2 = \Pi(3) = \overline{Q_1} + \overline{Q_0}$

Design the saturated counter

(0 – 1 – 3 – 4 – 5 – 6 – 6)

H.W.

[MCQ]

Consider a 4-bit Johnson counter an initial value of 0000. The counting sequence of this counter is -

[GATE-2015-CS: 1M]

A. 0,1,3,7,15,14,12,8,0

B. 0,1,3,5,7,9,11,13,15,0

C. 0,2,4,6,8,10,12,14,0

D. 0,8,12,14,15,7,3,1,0

0000
1000
1100
1110
1111
0111
0011
0001
0000

[MCQ]

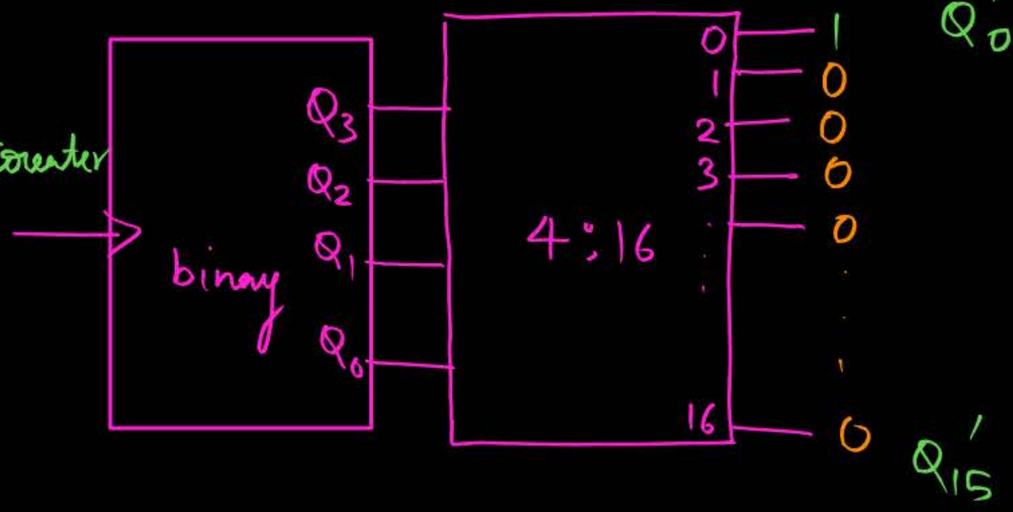
Let $k = 2^n$. A circuit is built by giving the output of an n-bit binary counter as input to an n-to- 2^n bit decoder. This circuit is equivalent to a

[GATE-2014-CS: 1M]

$n = 4$

$2^n = 16$

2^n — ring counter



(A) k-bit binary up counter.

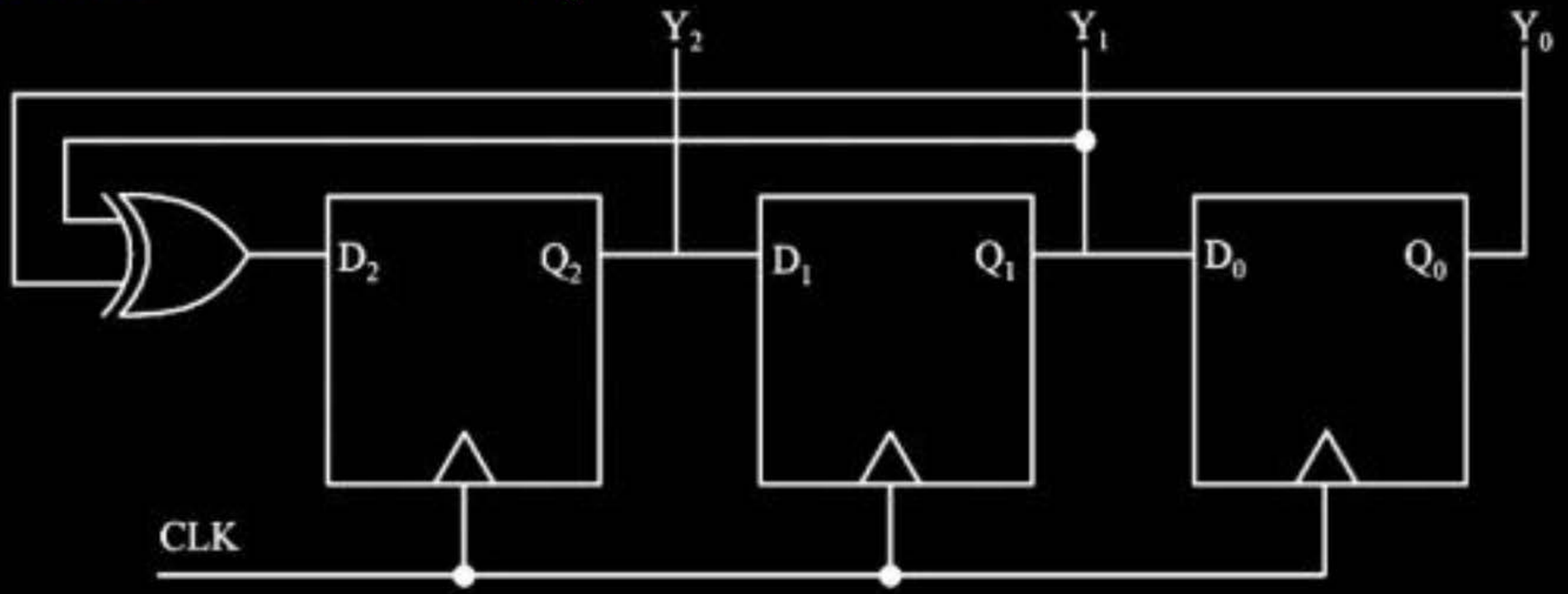
(B) k-bit binary down counter.

(C) k-bit ring counter.

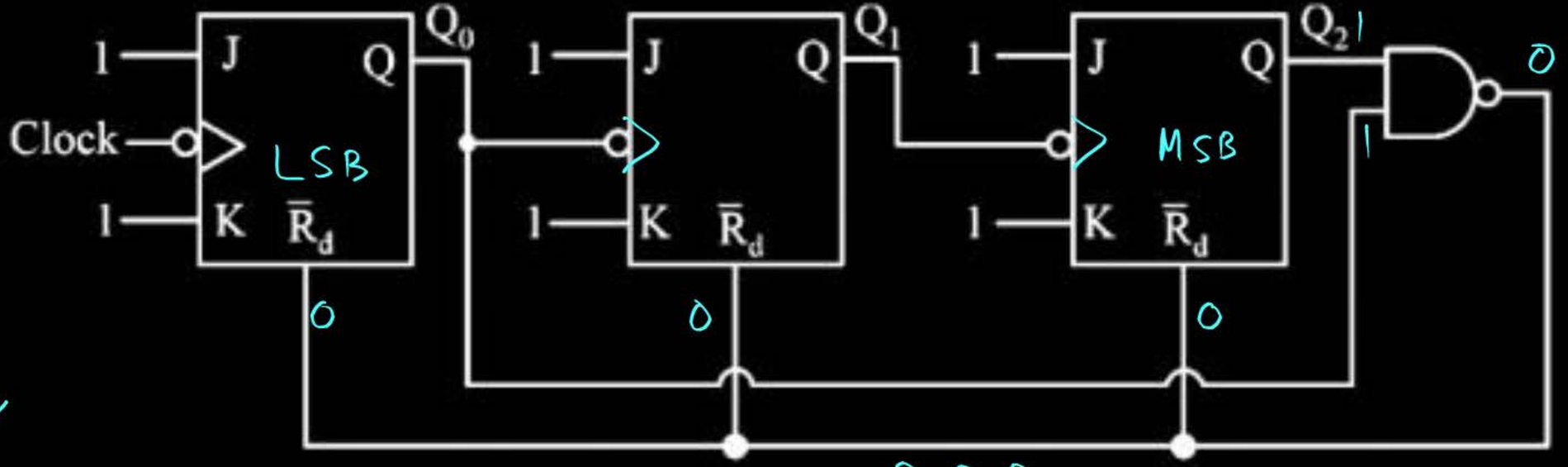
(D) k-bit Johnson counter.

#Q. A three-bit pseudo random number generator is shown. Initially the value of output $Y = Y_2\ Y_1\ Y_0$ is set to 111. The value of output Y after three clock cycles is _____.

H.W.



#Q. The circuit shown consists of J-K flip-flops, each with an active low asynchronous reset ($\overline{R_d}$ input). The counter corresponding to this circuit is



A a modulo-5 binary up counter

B a modulo-6 binary down counter

C a modulo-5 binary down counter

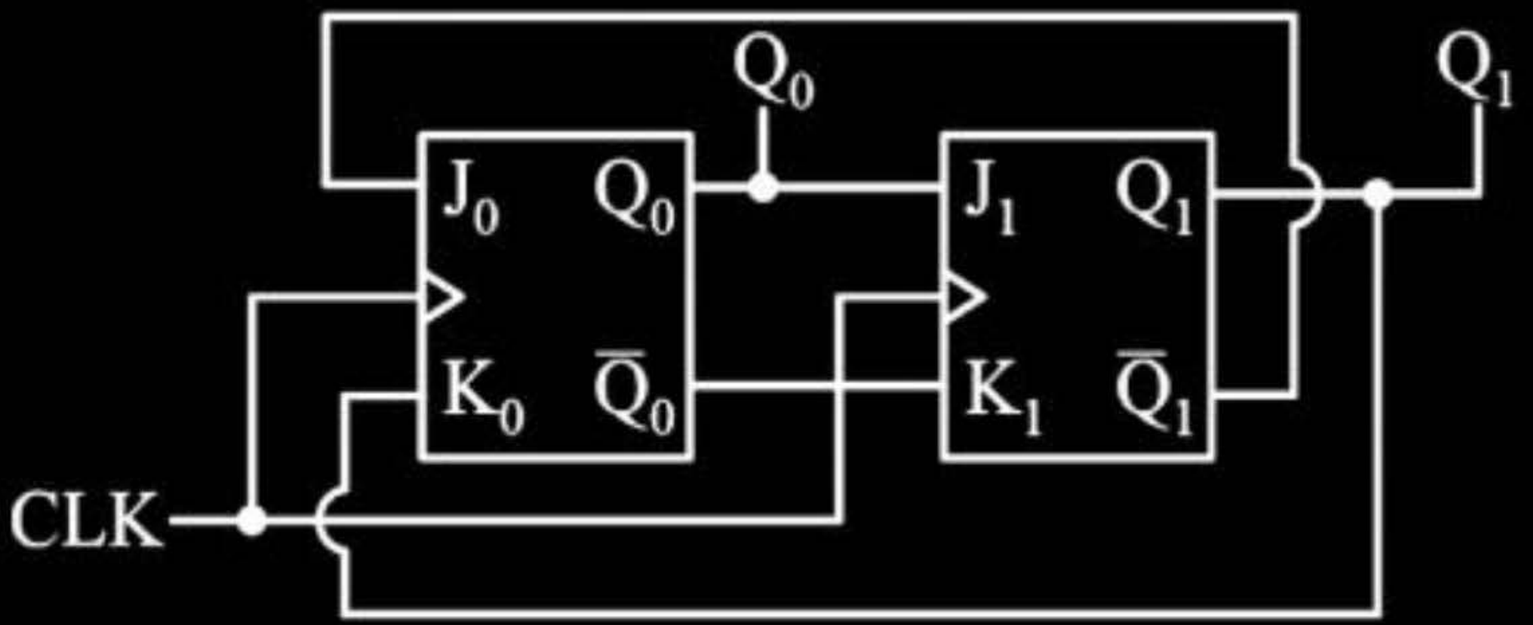
D a modulo-6 binary up counter

Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0

$101 \longrightarrow 000$

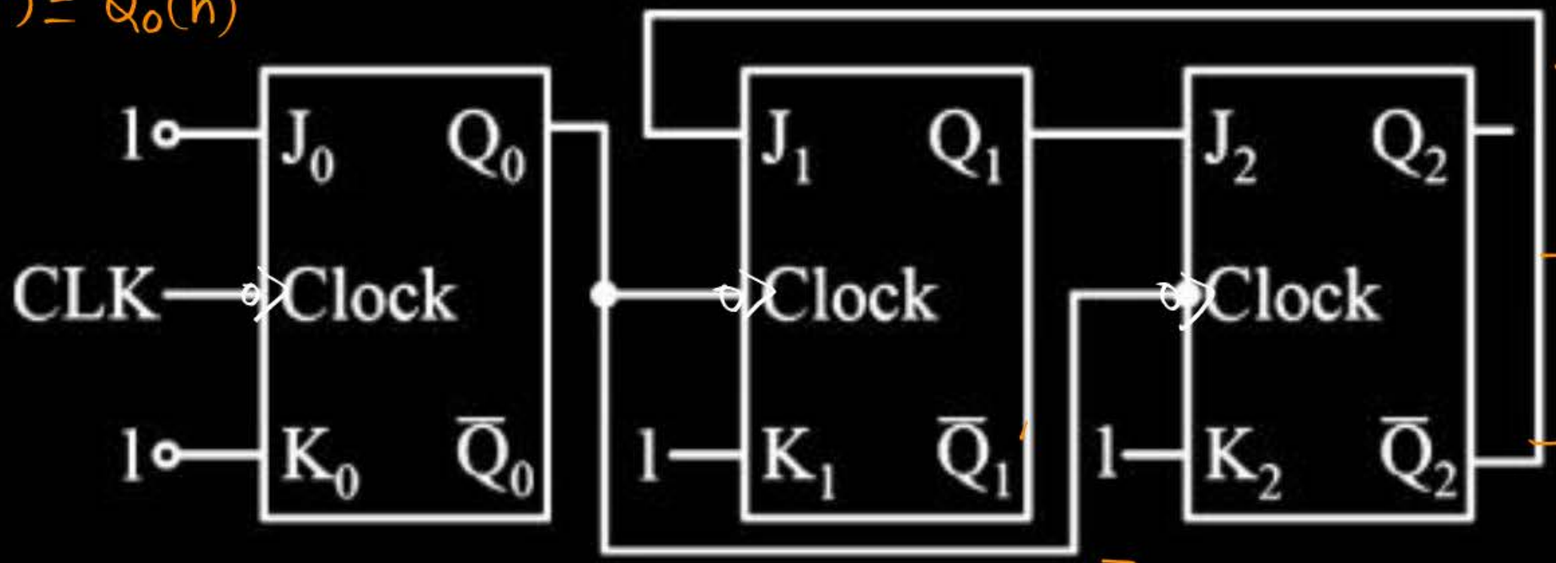
#Q. In the following sequential circuit, the initial state (before the first clock pulse) of the circuit is $Q_1\ Q_0 = 00$. The state $(Q_1\ Q_0)$, immediately after the 333^{rd} clock pulse is _____.

H.W.



#Q. The figure shows a digital circuit constructed using negative edge triggered J-K flip flops. Assume a starting state of $Q_2\ Q_1\ Q_0 = 000$ will repeat after 6 number of cycles of the clock CLK

$Q(n+1) = \overline{Q}_0(n)$



$Q_1(n+1) = \overline{Q}_2(n).\overline{Q}_1(n) = \overline{Q_2(n)+Q_1(n)}$

$Q_2(n+1) = Q_1(n)\overline{Q}_2(n) = \overline{Q}_2(n).Q_1(n)$

Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
0	0	0

MOD-6

Topic : 2 Min Summary

→ Question Discussion.

Thank you

GW

Soldiers !