COMPUTER SCIENCE & IT

DIGITAL LOGIC

Lecture No. 12.

Combinational Circuit

By- Chandan Gupta Sir

Decoder

Encoder

Question Discussion

[NAT]

What is the minimum number of 2-input NOR gates required to implement a 4-variable function expressed in sum-of-minterms form as f = Σ(0, 2, 5, 7, 8, 10, 13, 15)? Assume that all the inputs and their complements are available. 3

[GATE-2019-CS: 2M]

$\boxed{BD + \bar{A}\bar{C}} \rightarrow 4$

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1			1
$\bar{A}B$		1	1	
AB		1	1	
$A\bar{B}$	1			1

1 NOR → R

$BD + \bar{B}\bar{D} = (B+\bar{D})(\bar{B}+D)$

$= B \odot D$

$f = (B+P)(Q+D)$

$\bar{f} = \overline{B+P} + \overline{Q+D}$

$\bar{f} = X + Y$

$f = \overline{X+Y}$

Question

$f(x, y, z)$

A logical function f(x, y, z) is given as

$$f(x,y,z) = x\bar{y} + yz$$

Another logical function

$$f_1(x,y,z) = f[\bar{f}, f, z] \text{ will be}$$

a. $\bar{x} + y + z$

b. $\bar{x}y + yz$

c. $(x+\bar{y})(\bar{y}+\bar{z})$

d. $(x+\bar{y})(\bar{y}+\bar{z})(y+z)$

$f_1(x,y,z) = f[\bar{f}, f, z] = \bar{f}\cdot\bar{f} + f\cdot z$

$= \pi(4) = (\bar{x} + y + z)$

$= \bar{f} + fz$

$= (\bar{f} + z)$

f_1

	$\bar{y}\bar{z}$	$\bar{y}z$	yz	$y\bar{z}$
$\bar{x}$	1	1	1	1
x		1	1	1

$= \bar{x} + y + z$

Question

A 3-input majority gate is defined by the logic function $M(a, b, c) = ab + bc + ca$. Which one of the following gate is $M\left(\overline{M(a,b,c)}, M(a,b,\bar{c}), c\right)$?

$M[1, 1, 0] = 1$

$M[0, 1, 0] = 0$

(a) 3-input NAND gate $\overline{a \cdot b \cdot c}$ 1

(b) 3-input XOR gate $a \oplus b \oplus c$

(c) 3-input NOR gate $\overline{a + b + c}$ 1

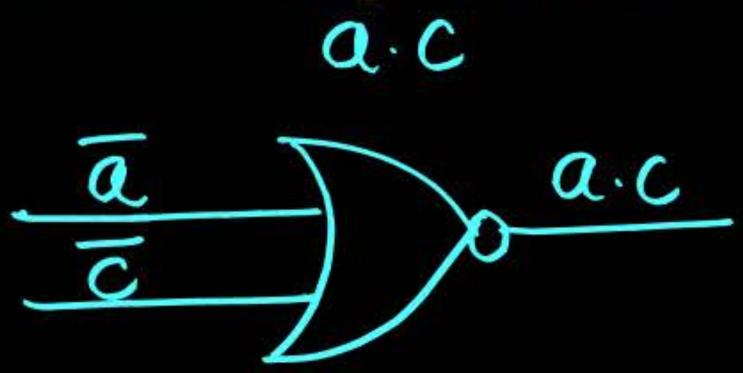
(d) 3-input XNOR gate

$M_1(a, b, c) = M\left[\overline{M(a,b,c)}, M(a,b,\bar{c}), c\right]$

$M_1(0,0,0) = M[1, 0, 0] = 0$

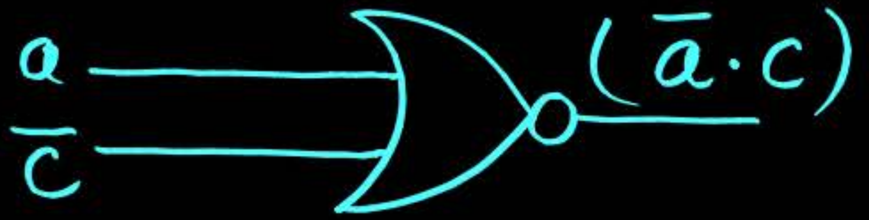
[NAT]

Consider the Karnaugh map given below, where X represents "don't care" and blank represents 0.



dc \ ba	00	01	11	10
00		x	x	
01	1			x
11	1			1
10		x	x	

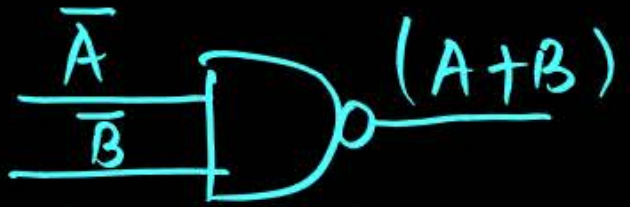
$f = c \cdot \bar{a}$



Assume for all inputs(a, b, c, d) , the respective complements $(\bar{a}, \bar{b}, \bar{c}, \bar{d})$ are also available. The above logic is implemented using 2-input NOR gates only. The minimum number of gates required is ___1___.

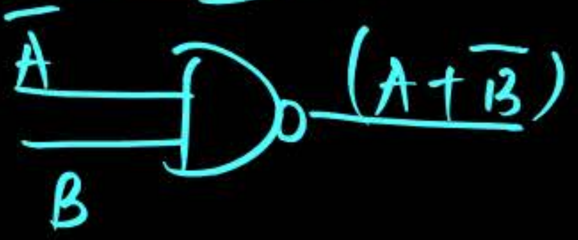
[GATE-2017-CS: 1M]

$A+B$

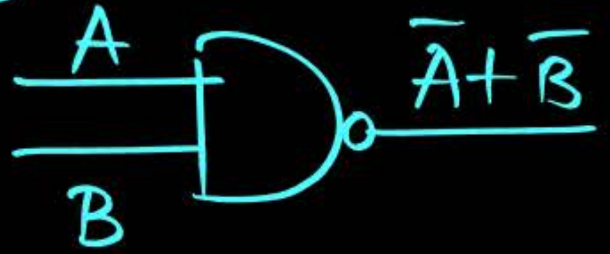


$\bar{A}+B$

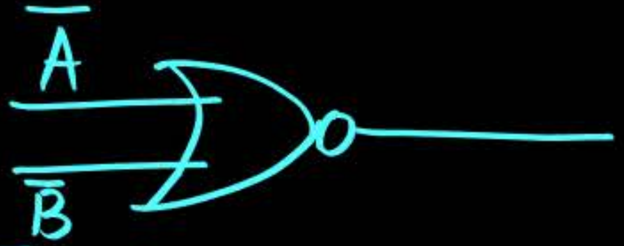
$A+\bar{B}$



$\bar{A}+\bar{B}$



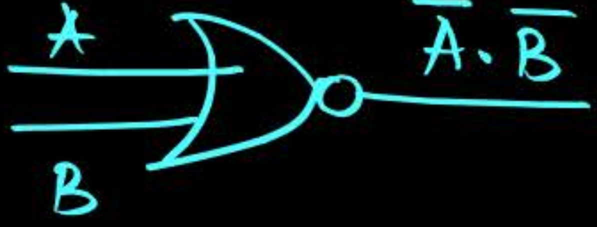
$A\cdot B$



$A\cdot\bar{B}$

$\bar{A}\cdot B$

$\bar{A}\cdot\bar{B}$



[MCQ]

Consider the following Boolean expression for F: $F(P, Q, R, S) = PQ + P'QR + P'QR'S$

The minimal sum-of-products form of F is [GATE-2014-CS: 1M]

(A) $PQ + QR + QS$

(B) $P + Q + R + S$

(C) $\overline{P} + \overline{Q} + \overline{R} + \overline{S}$

(D) $\overline{P}R + \overline{P}\overline{R}S + P$

	$\overline{R}\,\overline{S}$	$\overline{R}S$	RS	$R\overline{S}$
$\overline{P}\,\overline{Q}$				
$\overline{P}Q$		1	1	1
PQ	1	1	1	1
$P\overline{Q}$				

$\to QR$

$= PQ + QR + QS$

$\to PQ$

$\to QS$

[MCQ]

Consider the following minterm expression for

F: $F(P,Q,R,S) = \sum 0, 2, 5, 7, 8, 10, 13, 15$

The minterms 2, 7, 8 and 13 are 'do not care' terms.

The minimal sum-of-products form for F is

[GATE-2014-CS: 1M]

	$\bar{R}\bar{S}$	$\bar{R}S$	RS	$R\bar{S}$
$\bar{P}\bar{Q}$	1			X
$\bar{P}Q$		1	X	
PQ		X	1	
$P\bar{Q}$	X			1

$\bar{Q}\bar{S} + QS$

(A) $Q\bar{S} + \bar{Q}S$

(B) $\bar{Q}\bar{S} + QS$

(C) $\bar{Q}\bar{R}\bar{S} + \bar{Q}R\bar{S} + Q\bar{R}S + QRS$

(D) $\bar{P}\bar{Q}\bar{S} + \bar{P}QS + PQS + P\bar{Q}\bar{S}$

[MCQ]

What is the minimal form of the karnaugh map shown below? Assume that X denotes a don't care term

[GATE-2012-CS: M]

cd \ ab	00	01	11	10
00	1	×	×	1
01	×			1
11				
10	1			×

(A) $\bar{b}\bar{d}$

(B) $\bar{b}\bar{d} + \bar{b}\bar{c}$

(C) $\bar{b}\bar{d} + a\bar{b}\bar{c}d$

(D) $\bar{b}\bar{d} + \bar{b}\bar{c} + \bar{c}\bar{d}$

$\bar{b}\bar{d} + \bar{c}\bar{b}$

[MCQ]

In the Karnaugh map shown below, X denotes a don't care term. What is the minimal form of the function represented by the Karnaugh map?

[GATE-2008-CS: M]

(A) $\bar{b}.\bar{d} + \bar{a}.\bar{d}$

(B) $\bar{a}.\bar{b} + \bar{b}.\bar{d} + \bar{a}.b.\bar{d}$

(C) $\bar{b}.\bar{d} + \bar{a}.b.\bar{d}$

(D) $\bar{a}.\bar{b} + \bar{b}.\bar{d} + \bar{a}.\bar{d}$

cd \ ab	00	01	11	10
00	1	1		1
01	X			
11	X			
10	1	1		X

$\bar{a}\bar{d} + \bar{b}\bar{d}$

[MCQ]

Consider the following Boolean function of four variables $f(A, B, C, D) = \Sigma(2, 3, 6, 7, 8, 9, 10, 11, 12, 13)$ The function is

[GATE-2008-CS: 1M]

(A) independent of one variable

(B) Independent of two variables

(C) Independent of three variables

(D) Dependent on all the variables

H.W

[MCQ]

Given $f(w, x, y, z) = \Sigma m(0, 1, 2, 3, 7, 8, 10) + \Sigma d(5, 6, 11, 15)$, where d represents the don't-care condition in Karnaugh maps. Which of the following is a minimum product-of-sums (POS) form of $f(w, x, y, z)$? [GATE-2017-CS: 1M]

(A) $f = (\bar{w} + \bar{z})(\bar{x} + z)$

(B) $f = (\bar{w} + z)(x + z)$

(C) $f = (w + z)(\bar{x} + z)$

(D) $f = (w + \bar{z})(\bar{x} + z)$

	$\bar{y}\bar{z}$	$\bar{y}z$	yz	$y\bar{z}$
$\bar{w}\bar{x}$	1	1	1	1
$\bar{w}x$		X	1	X
wx			X	
$w\bar{x}$	1		X	1

$= \bar{x}\bar{z} + \bar{w}z = (z + \bar{x})(\bar{z} + \bar{w})$

[MCQ]

Consider the 4 – to – 1 multiplexer with two select S_1 and S_0 given below. The minimal sum of products from the Boolean expression for the output F of the multiplexer is -

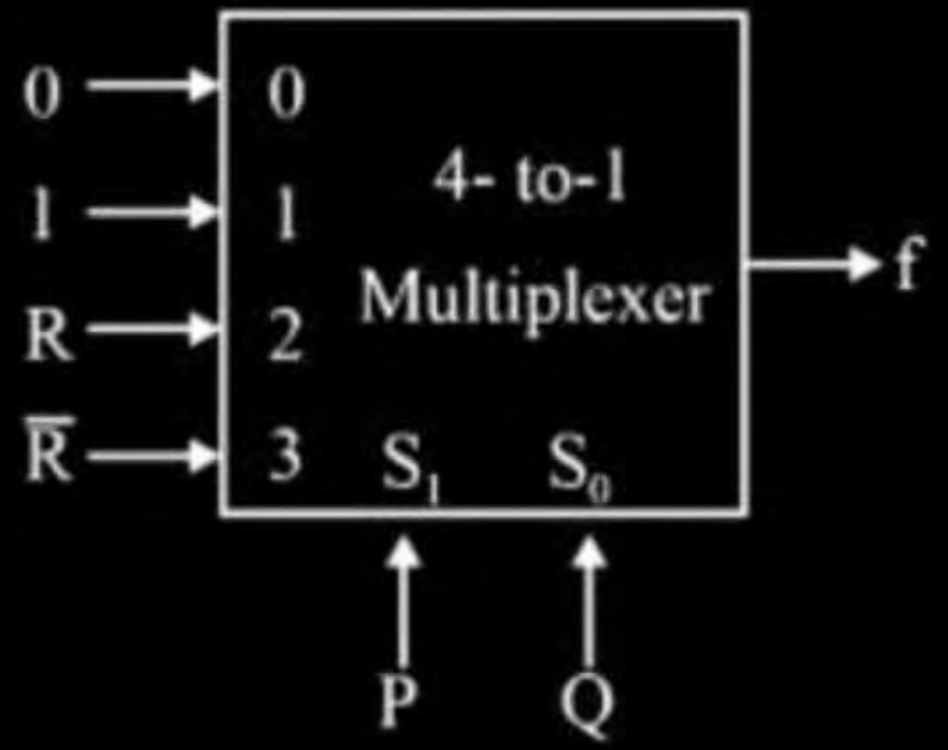
[GATE-2014-CS: 2M]

(A) $\bar{P}Q + Q\bar{R} + P\bar{Q}R$

(B) $\bar{P}Q + \bar{P}Q\bar{R} + PQ\bar{R} + P\bar{Q}R$

(C) $\bar{P}QR + \bar{P}Q\bar{R} + Q\bar{R} + P\bar{Q}R$

(D) $PQ\bar{R}$

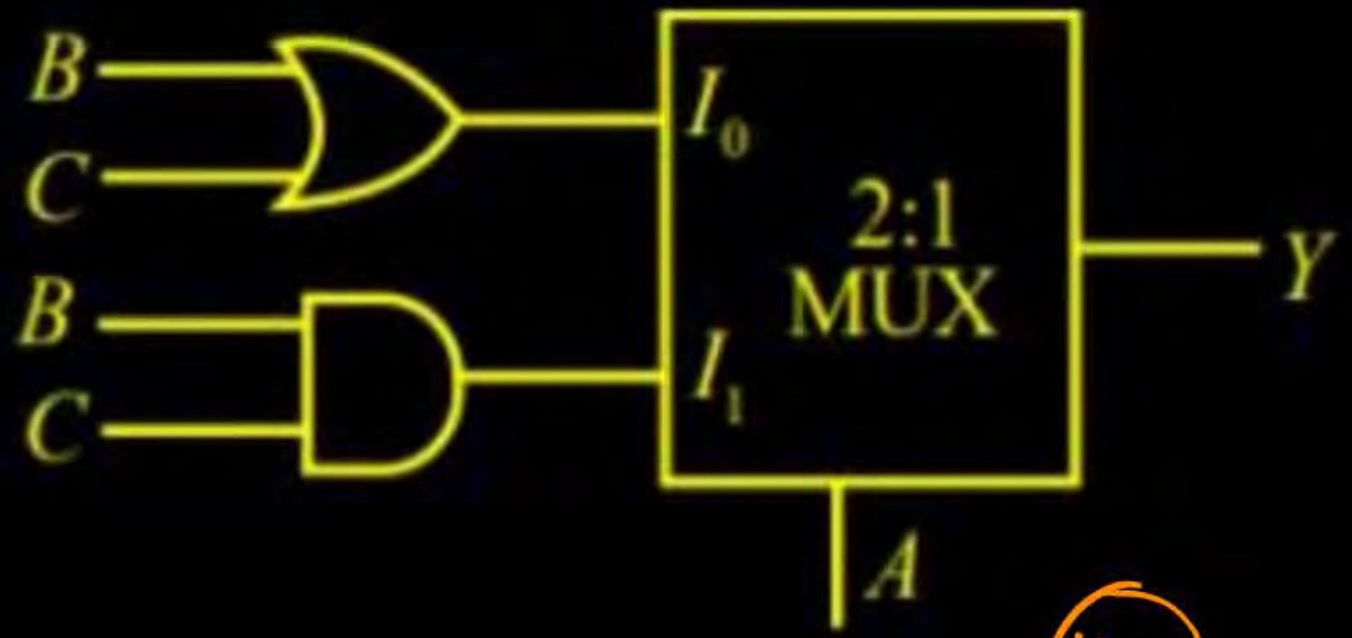


H.W

Question

Logical circuit is implemented as

Y represents



H.W

(A) Borrow output of full subtractor

(B) Carry output of full adder

(C) 3-input XOR gate

(D) 3-input NOR gate

[MCQ]

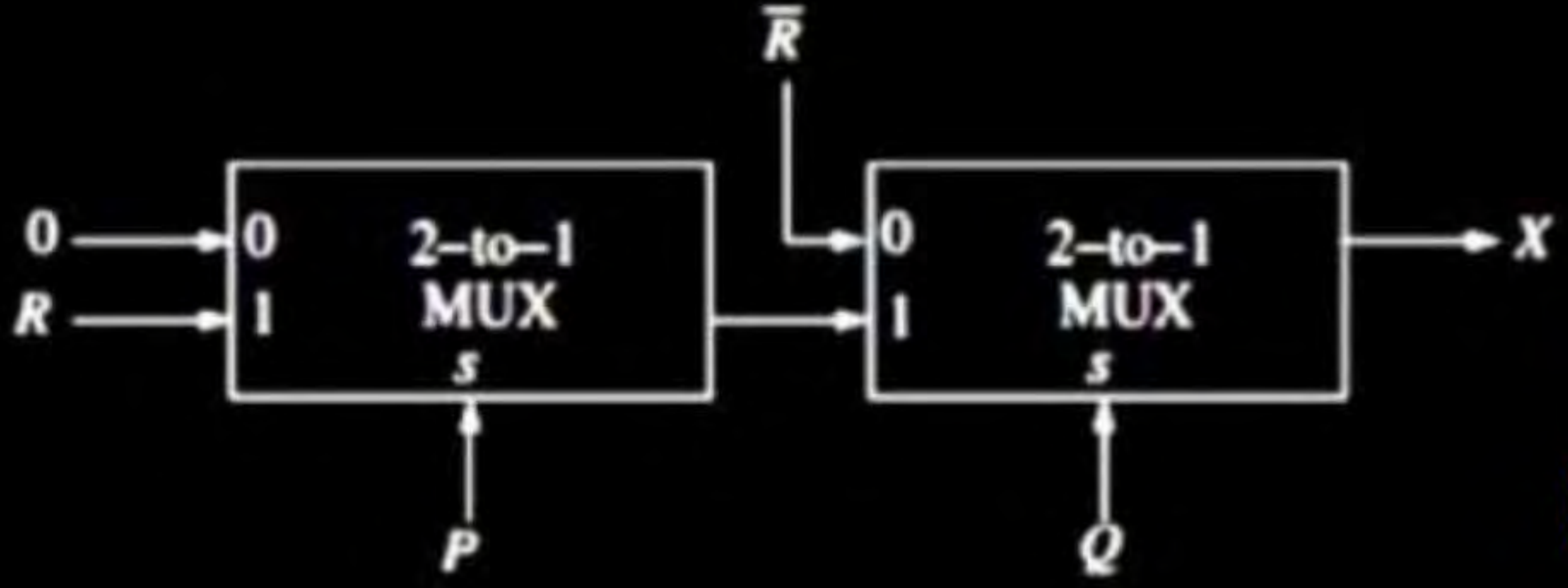
Consider the two cascaded 2 to 1 multiplexers as shown in the figure.
The minimal sum of products form of the output X is : [GATE-2016-CS: 1M]

(A) $\overline{P}\,\overline{Q}+PQR$

(B) $\overline{P}Q+QR$

(C) $PQ+\overline{P}\,\overline{Q}R$

(D) $\overline{Q}\,\overline{R}+PQR$

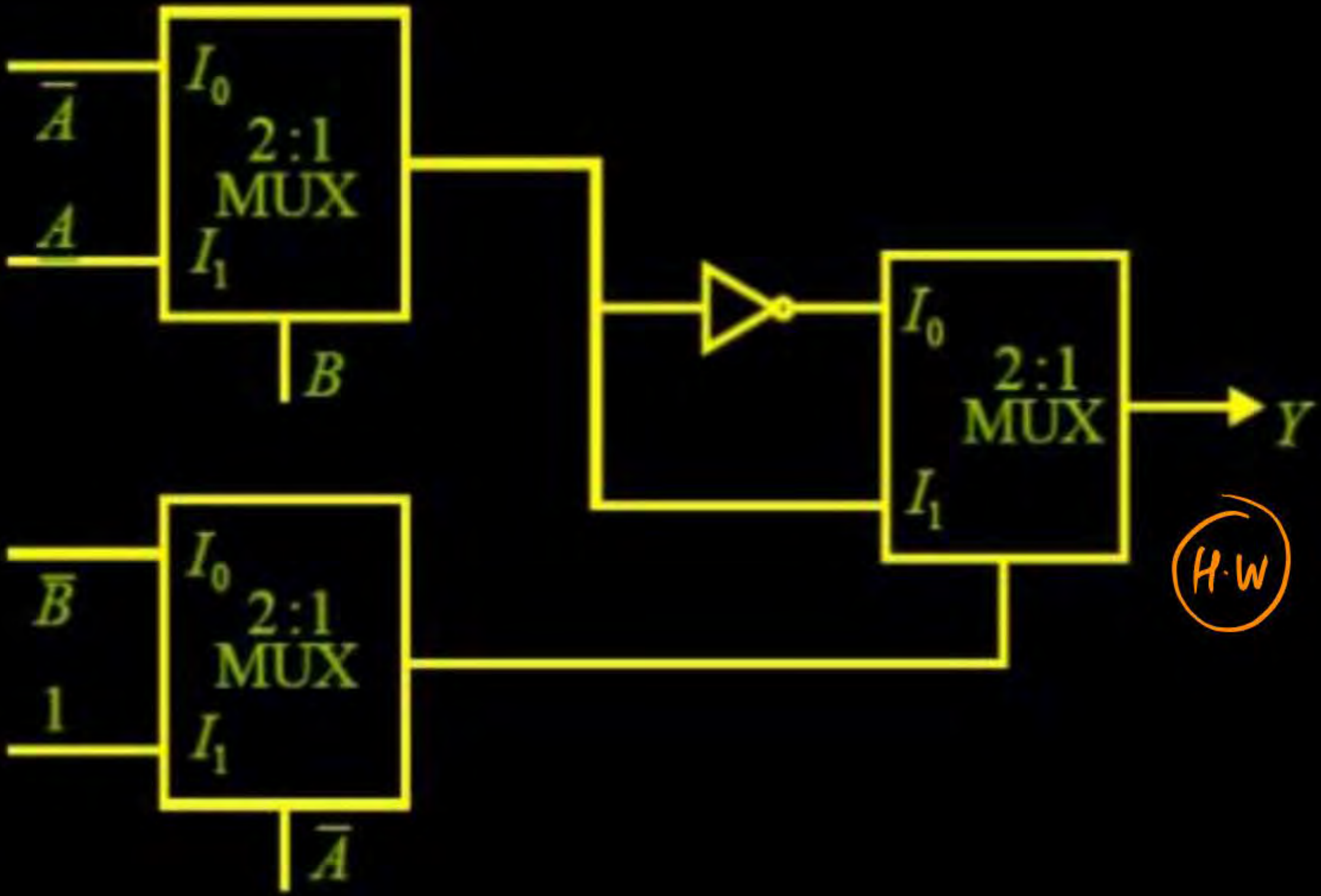


H.W

[Question]

Combination circuit in designed as shown below:-

Output Y is



(a) 2 input NOR gate

(b) 2 input AND gate

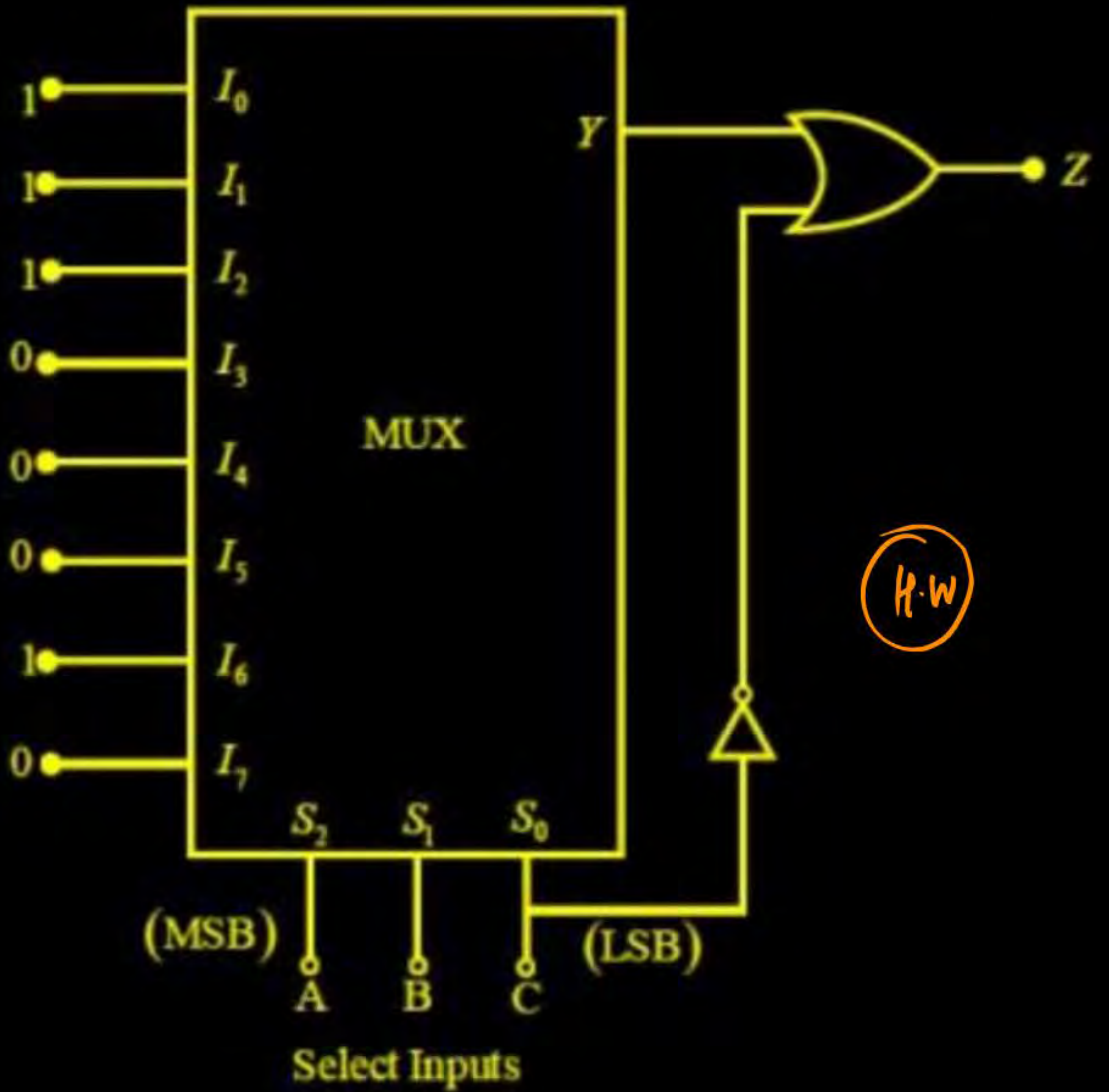
(c) 2 input OR gate

(d) 2 input NAND gate

H.W

Question

A combinational circuit using an 8 to 1 multiplexer is shown in the following figure. The minimized expression for the output (Z) is



(a) $C(\overline{A}+\overline{B})$

(b) $C(A+B)$

(c) $\overline{C}+\overline{A}\overline{B}$

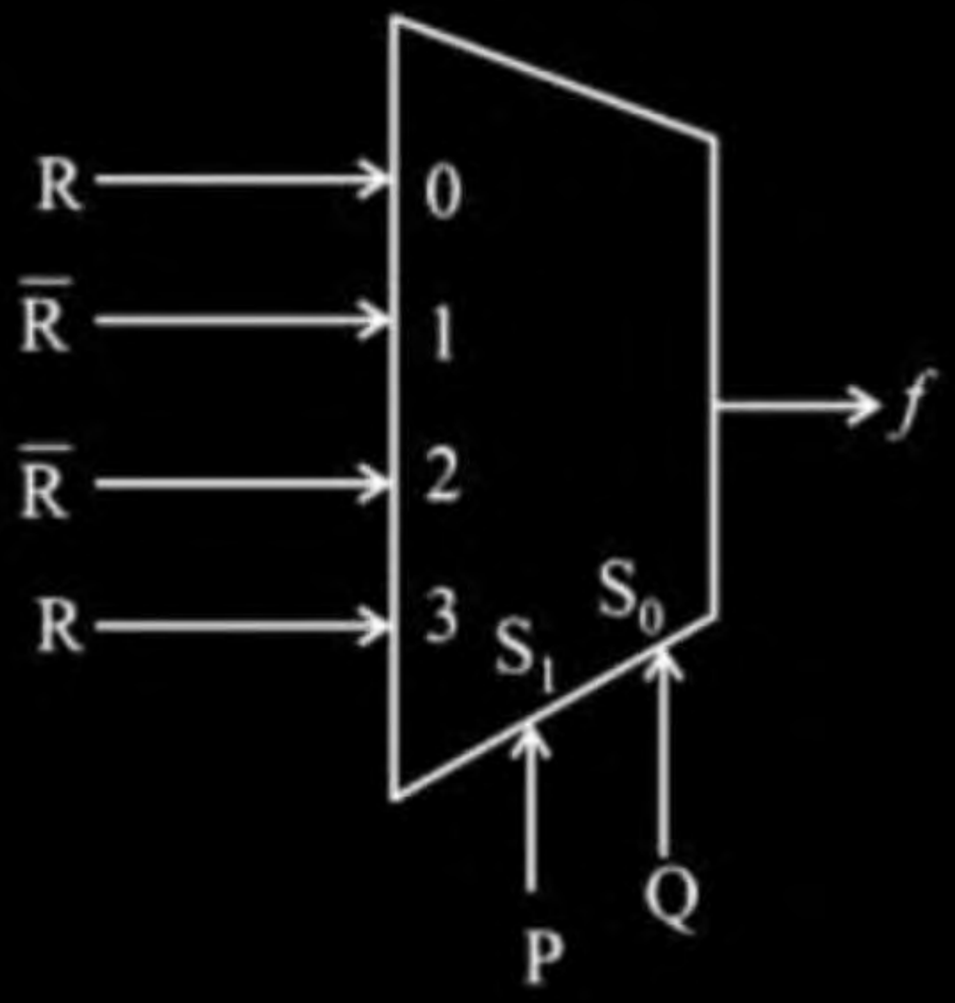
(d) $\overline{C}+AB$

H.W

[MCQ]

The Boolean expression of the output f of the multiplexer shown below is :

[GATE-2010-CS: 1M]



(A) $\overline{P \oplus Q \oplus R}$

(B) $P \oplus Q \oplus R$

(C) $P + Q + R$

(D) $\overline{P + Q + R}$

H.W

Question

logical function f (A, B, C) is given as

$$f(A,B,C)=\overline{AB+BC+CA}$$

Then $f_1(A,B,C)=f[AB,BC,CA]$

f_1 implemented using 2 : 1 MUX with C as select input then input I_0 & I_1 of 2: 1 MUX will be

H.W

(a) $I_0=1, I_1=\overline{A}$

(b) $I_0=0, I_1=\overline{A}+\overline{B}$

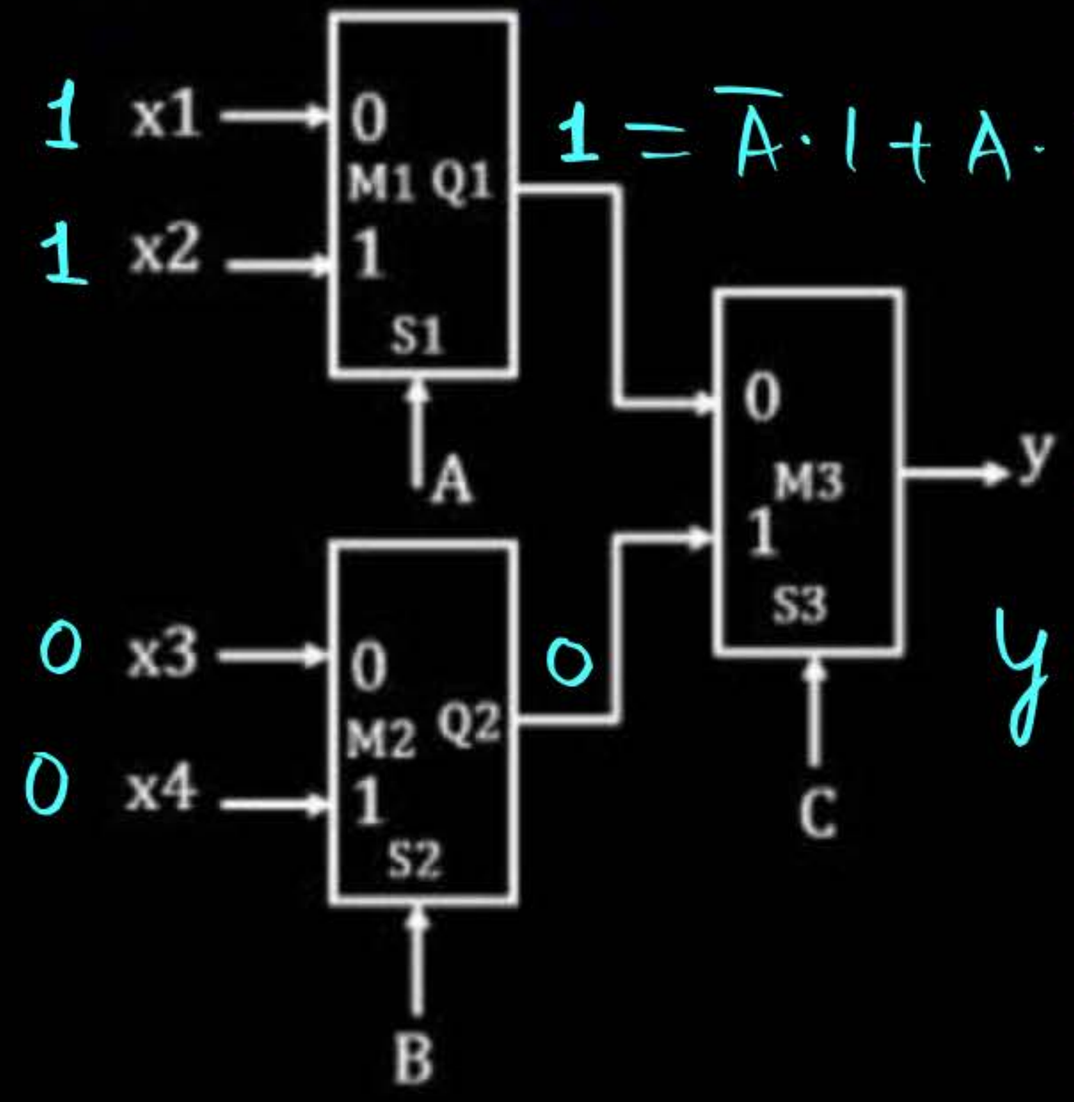
(c) $I_0=1, I_1=\overline{A}+\overline{B}$

(d) $I_0=0, I_1=\overline{A}+B$

[NAT]

Consider a digital logic circuit consisting of three 2-to-l multiplexers Ml. M2, and M3 as shown below. Xl and X2 are inputs of Ml. X3 and X4 are inputs of M2. A. B. and C are select lines of Ml. M2, and M3, respectively.

For an instance of inputs X1 = l, X2 = l, X3 = 0. and X4 = 0. the number of combinations of A. B. C that give the output Y=1 is ___4___ [GATE-2024-CS: 1M]



$1 = \bar{A}\cdot 1 + A \cdot 1$

$\bar{C}$

0 0 0 → 0
0 1 0 → 2
1 0 0 → 4
1 1 0 → 6

$y = \bar{C}\cdot 1 + C\cdot 0 = \bar{C}$

$y(A,B,C) = \bar{C} = \Sigma(0,2,4,6)$

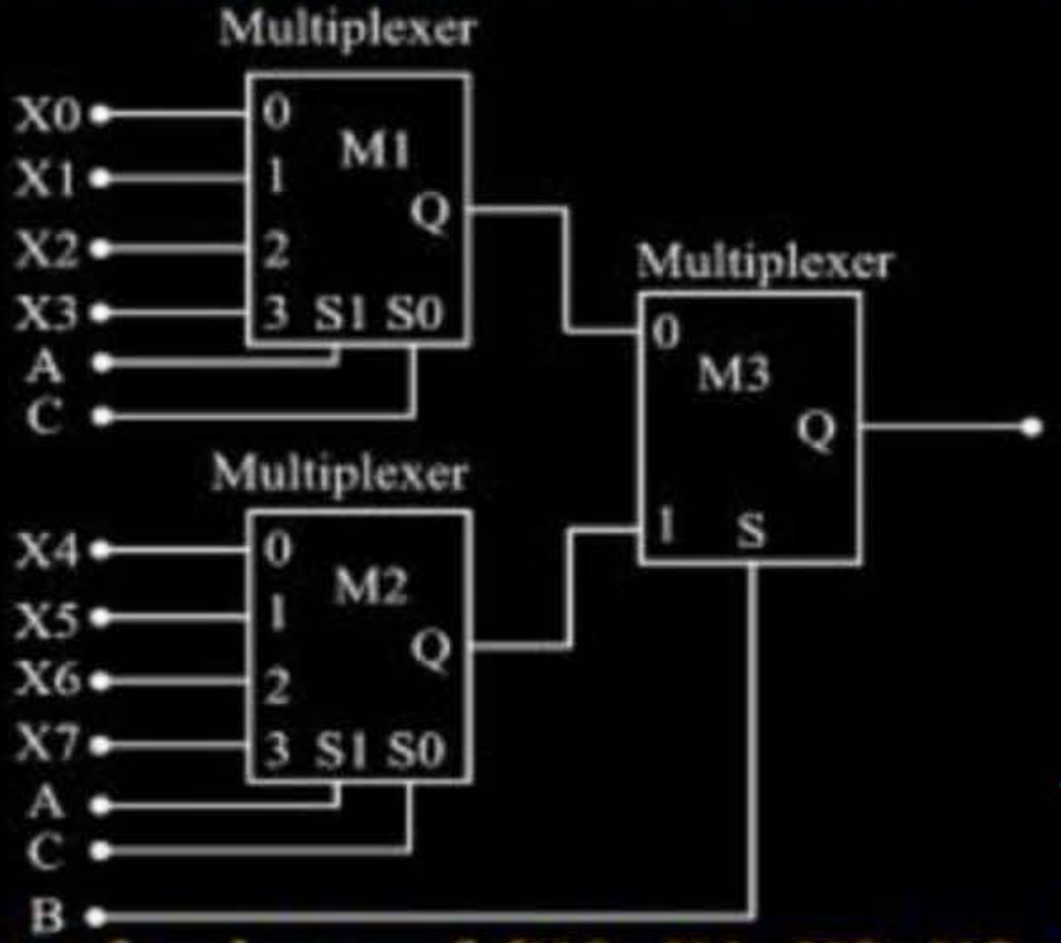
4 term

[MCQ]

A Boolean digital circuit is composed using two 4-input multiplexers (M1 and M2) and one 2-input multiplexer (M3) as shown in the figure. X0-X7 are the inputs of the multiplexers M1 and M2 and could be connected to either 0 or 1. The select lines of the multiplexers are connected to Boolean variables A, B and C as shown.

$f(A,B,C) = \bar{A} + \bar{A}\bar{C} + A\bar{B}C$

$S_2 \; S_1 \; S_0$



$8:1 \xrightarrow{4:1} 2(4:1) + 1(2:1)$

$A=0, C=0, B=0$

$f(0,0,0) = 1, \quad X_0 = 1$

$A=1, B=0, C=1 \rightarrow X_3$

$f(1,0,1) = 1, \quad X_3 = 1$

Which one of the following set of values of (X0, X1, X2, X3, X4, X5, X6, X7) will realise the Boolean function $\boxed{\bar{A} + \bar{A}\bar{C} + A\bar{B}C}$

[GATE-2023-CS: 2M]

A. $(1, \underline{\underline{1}}, 0, 0, 1, 1, 1, 0)$ ✗

B. $(1, \underline{\underline{1}}, 0, 0, 1, 1, 0, 1)$ ✗

C. $(1, \underline{\underline{1}}, 0, 1, 1, 1, 0, 0)$ ✓

D. $(0, 0, 1, 1, 0, 1, 1, 1)$ ✗

[MCQ]

In the following truth table, V = 1 if and only if the input is valid. What function does the truth table represent ?

What function does the truth table represent ? [GATE-2013-CS: 1M]

Inputs				Outputs		
D_0	D_1	D_2	D_3	X_0	X_1	V
0	0	0	0	x	x	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	x	1	0	1	0	1
X	x	x	1	1	1	1

(A) Priority encoder

(B) Decoder

(C) Multiplexer

(D) Demultiplexer

[MSQ]

Consider a Boolean expression given by $F(X, Y, Z) = \Sigma(3,5,6,7)$.

Which of the following statements is/are CORRECT? [GATE-2024-CS: 1M]

(A) $F(X, Y, Z)$ is independent of input X

(B) $F(X, Y, Z) = XY + YZ + XZ$

(C) $F(X, Y, Z)$ is independent of input Y

(D) $F(X, Y, Z) = \pi(0, 1, 2, 4)$

H.W

[MCQ]

The number of min-terms after minimizing the following Boolean expression is

[GATE-2015-CS: 1M]

_____. $[D' + AB' + A'C + AC'D + A'C'D]' = \Sigma(15) = ABCD$

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$				
$\bar{A}B$				
AB			1	
$A\bar{B}$				

(A) 1

(B) 2

(C) 3

(D) 4

[MSQ]

Let, $x_1 \oplus x_2 \oplus x_3 \oplus x_4 = 0$ where x_1, x_2, x_3, x_4 are Boolean variables, and $\oplus$ is the XOR operator. Which one of the following must always be TRUE?

[GATE-2022-CS: 1M]

H.W.

(A) $x_1 x_2 x_3 x_4 = 0$

(B) $x_1 x_3 + x_2 = 0$

(C) $\overline{x_1} \oplus \overline{x_3} = \overline{x_2} \oplus \overline{x_4}$

(D) $x_1 + x_2 + x_3 + x_4 = 0$

[MCQ]

What is the minimum number of gates required to implement the Boolean function (AB + C) if we have to use only 2-input NOR gates? [GATE-2009-CS: 1M]

A. 2

B. 3

C. 4

D. 5

H.W

Question

A 2-bit binary multiplier can be Implemented using

(a) 2 input AND gates only

(b) Six 2-input AND gates and two XOR gates.

(c) Two 2-input NORs and XNOR gate.

(d) XOR gates and shift registers

$$
\begin{array}{cccc}
 & & a_1 & a_0 \\
 & & b_1 & b_0 \\
\hline
 & & a_1b_0 & a_0b_0 \\
 & a_1b_1 & b_1a_0 & \\
 & c_0 & & \\
\hline
C_3 & S_2 & S_1 & a_0b_0
\end{array}
$$

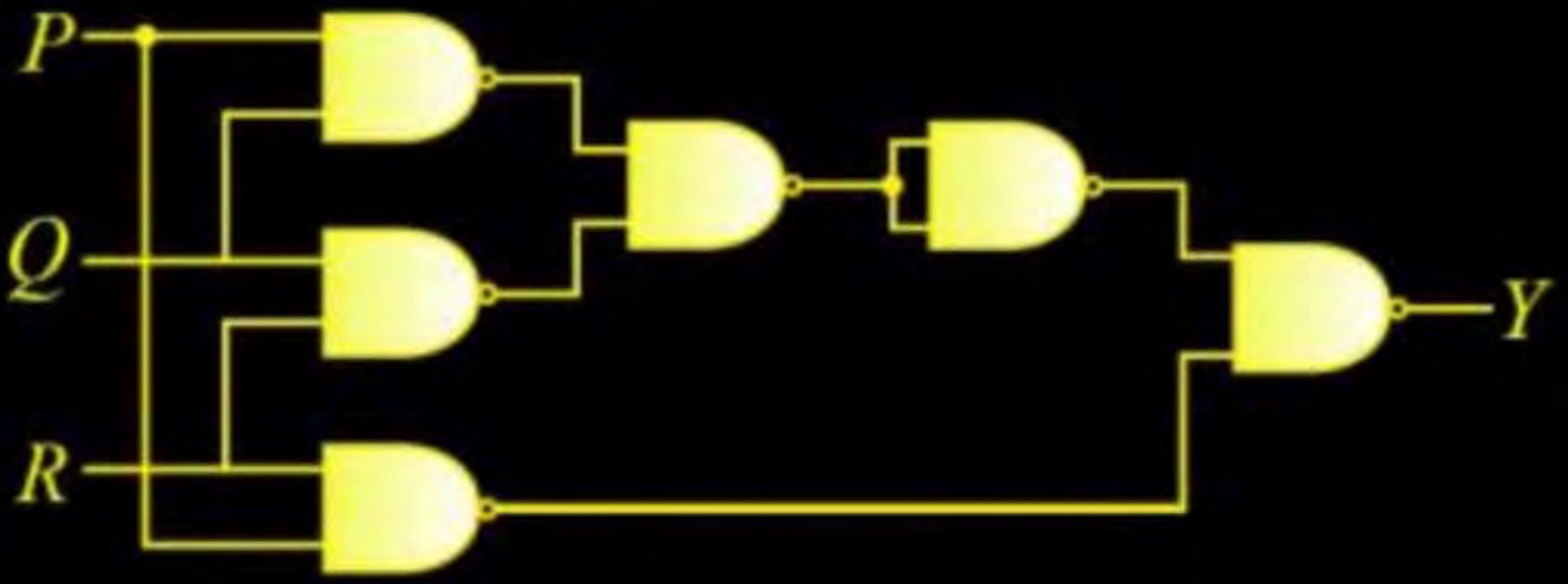
$\underline{4\text{ AND}} + 1\text{HA} + 1\text{HA}$

1HA ↓ 1XOR, 1AND

1HA ↓ 1XOR, 1AND

[**Question**]

The output Y is the circuit below is always "1" when



H.W

(a) Two or more of the input P, Q, R are "0".

(b) Two or more of the inputs P, Q, R are "1".

(c) Any odd number of the inputs P, Q, R are "0".

(d) Any odd number of the inputs P, Q, R are "1".

2 Minute Summary

Question Discussion.

Thank you

GW Soldiers !