Hardware waveforms and what not.

The values which we had derived from the simulations are not worthy anymore - because the hardware itself does not follow it.

I mean the voltage levels are not that high but still.

It really drives home the message that a perfect dead time is crucial - **because even after increasing the dead time - it is highly possible that the ringing voltage itself is causing it.**

So it will still report a very large value at hand. And a 1.25 u inductive load required a 25n deadtime.

That is true because now my Cds is much larger - therefore the time taken for the capacitor to discharge also increases accordingly.

This is the 2nd gate driver that has gone bad - **Now I dont know what to make of this - The realisation is that -**

Either the board which I have made is wrong - which is a very bad realisation for me - or the fact that the gate drivers are bad.

Now - this is something that is left to be seen.

I did Check the V_zvs circuitry board that exists - and it was not showing any errors.

I do not know the limits of the TMS board - how much current can 1 GPIO maximum give -

I was about to give square wave voltage across RC - now that could have lead to high currents within the system.

Next day we are checking things and realise the fact that - the waveforms were pretty much decent. Though the waveforms themselves were not acting good - at the source place.

<u>I used to have this thinking that If I keep the ground floating - then the floating values will only be 0.2 0.3 etc - so the nature of the curve wont change.</u>

<u>I was wrong - it sometimes showed -6 to 3 as -5 to -5.</u> *<u>And maybe</u> that was the case for the -7 to 8 stuff also. IDK.* ***Or it repaired itself somehow.***

Nonetheless - always connect to other potential - cause it is not only voltage - but the impedance that the circuit itself sees .

Also - *It turned out the upper device source ka solder pad had essential disconnected from the rest of the circuit - and therefore was causing lots of issues. We fix that issue.*

3rd issue - ***Now we repair the guy and test things. It works brilliantly - but the lower device does not.***

Turns out one of the resistors went bad on us. *And also the diode which is not very surprising.*

Before soldering the entire ZVS Pcb - I have to properly know how much simulation and actual variation is there between different RC time constants and - Different Voltage values and Dead times - This exercise though cumbersome now - will give fruition later - as you will know what to expect of the system at hand.

The ADVICE - NOT TO TAKE A SINGLE STEP LIGHTLY IS VERY IMPORTANT AT THESE TIMES BECAUSE PEOPLE OFTEN FORGET THAT

The ones below are without load
We shall attempt the same with the load as well

Without load - we will witness that the simulation values will have no difference - **because the capacitors have no path to discharge, unless when on - Then the things are different.**

At 60 n - ambient temp 38

30V - 49 cel , 15 v - 42.5 cel

30V - 46.7 at 76 ohm resistor point 20n - Goes from 43.5 to -15.5

At 60n , 76 ohm - 48.6 max temp

At 20n - The received actual dead time is 17.8ns - becuase rise and fall times do take some space - 1n each roughly.

And 25v - the ringing went from 35v to -16v - **Such huge ringing leads to concern**

In Our case - realise that - if you try to test things without gnd - things will definitely end in a failure.

R	C	T_dead	V_in	V_R(sim)p-p	V_R(Real)p-p
39	40pF	60n	30	16 to - 9.5 or vice versa	10.6 to -6.8 or -12.75 to 6.5
		20n			11.7 to -8.6 or -14 to + 8.5
		60n	15	8 to -5 or vice-versa	6.8 to -5.2 or -7.6 to 5
		20n		‘’ ‘’	7 to -5.3 and -7. To 6
		60n	5	2.8 to -1.8 or vice versa	2.7 to -1.8 or 2 to -3
		20n		‘’’’	Same and 2.2 to-2.8
76	40pf	60n	30	‘’’’’’	17.25 to -7.825 or -16.875 to 8.875
		20n		23.7 to -9 or -23 to 9.2	16.5 to -8 or -18.9 to 6.675
		60n	15	‘’’’’	10 to -5.68 or -10.75 to 6.25
		20n		11.77 to -4.75 or -11.7 to -5	9.9 to -5 or -10.9 to 5.75

		60n	5	“””	2.8 to -2.3 or -4.1 to -2.5
		20n		4 to -1.7 or vice versa	3.5 to -2 or -4.2 to 2.35
76	20	60n	30	16 to -9.66 or vice versa	10.3125 to -6.5 or -10.18 to 5.625
		20n		“””	10.625 to -7 or 10.375 to -6.875
		60n	15	8 to -4.75 or vice versa	6.5 to -4.375 or 6.4375 to -4.1875
		20n		“”	6.56 to -4.06 or-6.5 to 4
		60n	5	2.739 to -1.66 or vice versa	2.5 to -2 or -2.7 to 1.7
		20n		“””	2.6 to -1.7 or -2.42 to 1.7
39	20	60n	30	“””	7.43 to -5.875 or -5.8 to 4.875
		20n		9.19 to -7.22 or vice versa	7.25 to -5.31 or -6 to 4.6
		60n	15	“””	4.85 to -3.42or -3.6 to 3
		20n		4.64 to -3.83 or vice versa	4.4 to -3.3 or -3.8 to 3.3
		60n	5	1.9 to -1.3 or vice versa	1.975 to -1.4 or -1.4 to 1.4
		20n		“””	2 to -1.625 or -1.5 to 1.5

The load is now 1.25u and with it in tow is a capacitor

5v - 60n - 1v to -1 or 1vto -1.3

My issue also lies with the fact that I am unable to tell other things apart - basically that I am unable to probe multiple things at once is a limitation - a huge one

30v = 1.3v to -1.8v

Now the case where - 39 ohm and 40 pf with the load 1.25 u and 60ns dead time

IRL

5V - 2.3to -1.55 or -2 to 1.625
15V - 2.35 to -1.4 or -2 to 1.4
30V - 3.1 to -2 or -2.8 to 2.89

20ns

5V
15V 1.5 to -950mv or -2.3 to 1.5
30V 3.1 to -925mv or -3.5 to 2

This discrepancy is not well understood - The only explanation that comes to my mind is that 60ns was giving more rining behaviour and thus *There was more hard switching behaviour that was getting exhibited over there as opposed to 20ns .*

Other than that there seems to be no plausible explanation - I cannot measure all 3 alone simultaneously - This really does call the probe point things - because elsewise it really is very hard to see trends.

The circuit is not behaving the way I had simulated or anyway near it.

What I am seeing is that 1) I am seeing the switch node voltage across the resistor which Does not make sense. Although a scaled version of it.

*The resistance is having a 0 avg when the vzvs is positive - but a neg avg when it takes a negative dip ie switch 2 turning on - **Because it has a overall avg - it means there is some current that is flowing thru it.***

That current is dvdt - which means that the switch node voltage is changing during this time period as well - otherwise there ideally should be no current in the resistor.

There should also be this study done as to because there is a slight change in this topology - is it possible that the inductor current is somehow contributing to this issue at hand. - **The simulation does not show any major value changes or nature changes.**
Therefore this is definitely not the reason.

After checking the waveforms I can tell that the switch_node voltage is perfectly alright.

It does not make sense for the resistor voltage to copy the switchnode voltage - **We right now checked it at the Diode input terminal - let us check it at the proper resistor terminal. - they r the same.**

Yes , The capacitor is posing an issue - there looks like an RC delay within the circuit which is eating it - now it still does not say why the current is constant - but still - This needs some analysis.

The actual V_cap is **a very sorry function - it does explain the behaviour of the resistor.**

Now we have to figure out whether the amplitudes match -what is the behaviour during the switching cycles and why is it exhibiting such a behaviour.

According to me the voltage levels themselves are not matching up - therefore there is something wrong with the way we have done this.

It is also possible - we have not connected the diode properly or something

Simulation

The circuit stopped working - it was effectively shorting something inside - I removed the loads and the zvs circuitry and checked.

Luckily the gate drivers have survived this assault. ***This was deadly. I think the issue is with the zvs circuitry.***

Let us reaffirm ourselves with the fact that it is working .

I think I inadvertently- shorted the capacitor or something akin to it.

Dikkat was in the way you had soldered the 2nd part - now that second part is needed because the current voltage values are not that high.

2 Hours it took - wow.

It is finally working !!

The entire thing I had written is deleted for some reason I will not understand.

The fact remains that -

V_zvs is pulsating in value and is not taking any dc value whatsoever -

The resistor in question is taking ringing ofcourse - 0v to -1.1 V - which was never supposed to happen.

It is supposed to have voltage in *the switching instants only - it should not have a negative voltage.*

Which clearly implies that - there is a dv/dt within the capacitor - which is acting up.

When the Switch node turns off - ie when Vsw rises - the capacitor is doing good work and so is the resistor and I think so is the Diode at hand.
It is behaving the way it should.

While turning down - it is not behaving the way it should - it is rather - seeing a negative current.

Also ***the switch is on - therefore the net voltage across it should be zero - that after that small dv/dt instant crosses - the capacitor should have vdd or 0 voltage - and nothing in between.***

What we see is that it goes slightly above VDD and also it has a *natural potential if we may call it.*

It looks like an RC decay of some sort - but the voltage across the resistor is pretty fixed. -1and 0 .

Changing the dead time and changing the RC time constants is the only thing that I can think of that can have an effect on this system.

Why such a behaviour exists is something I am unable to understand clearly.

The initial 2 photos are of 20 ns deadtime.

We shall look into this - Though I do not believe this is the result of RC time constant of the system.

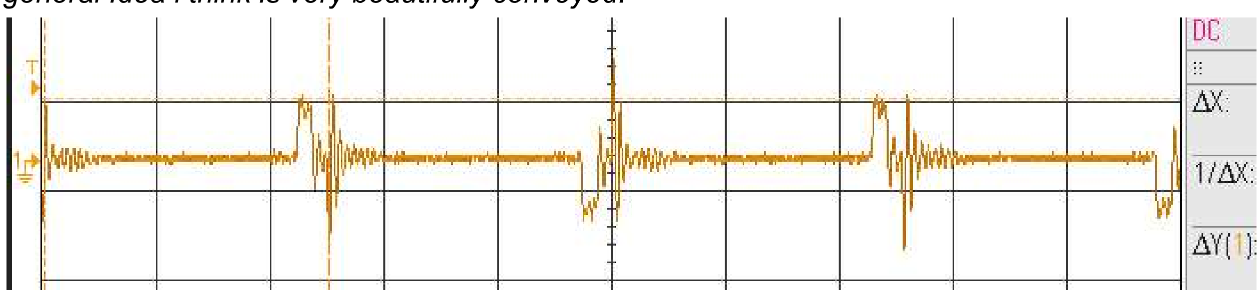
The reason being 1) The RC comes out as 1.6ns 2) *The time over which this occurs is farr to great.*
This we are talking about like within the switching cycle itself - it is when the things should be constant - they are not constant - they are giving this squiggly behaviour which even is bad.

Even the current started increasing which is very surprising for me - I have no idea how I should be taking this - ***the load qualities themselves are not that different .***

What I am witnessing is that - 60n par 15v 40mA and uske pehle at 20ns = 15 v and 10mA.

This behaviour makes no sense to me. ***Well Even the simulation shows that this is the behaviour we are seeing.***

Though ofc it gave 3.6mA and 10mA - *The scale factors adn everything are wrong - but the general Idea i think is very beautifully conveyed.*



These are the scopes or ***some snapshots of the resistor voltage before putting the diode circuitry within place - Now - this follows the idealised behaviour.***

But with the diode circuitry it is not.

Infact it is showing something else entirely - *Therefore the issue lies with either the way I have soldered it - which may have caused some issue - or* ***There is something else within the***

circuit that happens when we connect the diode and I have not taken that picture into acct.

We can immediately discard the RC time constant logic - ***because it would have been within play over here as well.***

Iff there is some phenomenon of such kind taking place - then it definitely is not taking place within the original ones - it is certainly only taking place after

So the different dead time does lead to an overall different current flowing. Something it is not doing right.

Some effect huh - 1 person hardware is a nightmare..

There is some other dominant effect - though we shall try

After talking to the senior - he told yes - there is some sort of RC dominant effect which we are not able to capture - now the idea is to figure out what might be causing that effect - the

Diode sizes which we use for high frequency applications are very small - *Parasitics minimization being the primary concern - The diode which I had ordered - it had huge parasitics within itself - The base it had itself was farr to large to my liking.*

Another concerning thing it had was - the footprint itself was different - toh we applied jugaad and put it.

Maybe some contact stuff is affecting it - I cannot really predict these things - ***Though what I have realised is that - it is possible that it was the one contributing to it.***

Now we are looking at existing diodes which will be used within this - The ones present in the lab
https://assets.nexperia.com/documents/data-sheet/PMEG3020EGW.pdf
This is a very promising replacement candidate

Have not checked all - though for low currents <4A - this is a very good replacement

Well The good Replacement is giving me bad results - There is something inherently working wrong within the system - that I am unable to figure out.

The issue it turns out I think - is - We had not cleaned the board achese - that lead to issues within it - and A resistor also came out.

Therefore I think the Reff within the RC time constant must have increased and was causing this issue within the RC which we were seeing and what actually should be.

The Issue we are facing now is - The diode is roughly giving the drop like it should - roughly 2V across it. **We are using the diode which is typically found in gate drivers. As mentioned.**

But the voltage is not being seen across the R and C of the DBR.

Which is a very curious case - because that should be visible to us - but it is not - which means - SOmehow it is catching some voltage which we are unable to see.

I do not think the issue lies within the capacitor - Otherwise the Diode will not have been giving a -ve avg.

The only way it can - is if the cap has some energy within it **but that is not visible.**

Curious case.

Different probes are giving different readings - either the probe is bad

There seems to be no issue because of the change in the slight configuration as we have already confirmed.