README

CAD_PROJECT 2
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Generate Design:
cd source_code
make
./M11215084 -h/-e ../aoi_benchmark/<filename.blif> and or not

-h: using heuristic solver
./M11215084 -h ../aoi_benchmark/test.blif 2 1 1

-e: using heuristic solver
./M11215084 -e ../aoi_benchmark/test.blif 2 1 1

Validate Design:
./M11215084 -v \<filename.blif> 2 1 1 \<result_to_validate>

Test case: Result with different latencies
1. using heuristic solver: latency=10
./M11215084 -h ../aoi_benchmark/test.blif 2 1 1

Heuristic Scheduling Result
1: {b1 b2} {} {}
2: {b3 b4} {} {}
3: {c1 b5} {} {}
4: {d1} {c2} {}
5: {} {c5} {e1}
6: {} {c3} {}
7: {} {d2} {}
8: {} {c4} {}
9: {} {d3} {}
10: {} {e2} {}
LATENCY: 10
END

2. using ILP solver: latency=8

./M11215084 -e ../aoi_benchmark/test.blif 2 1 1

ILP-based Scheduling Result
1: {b3 b5} {} {}
2: {b1 b2} {c3} {}
3: {b4 c1} {c4} {}
4: {d1} {c5} {}
5: {} {c2} {}
6: {} {d3} {e1}
7: {} {d2} {}
8: {} {e2} {}
LATENCY: 8
END