

硬體描述語言設計與模擬

Homework #1

Title :4_BIT_ALU

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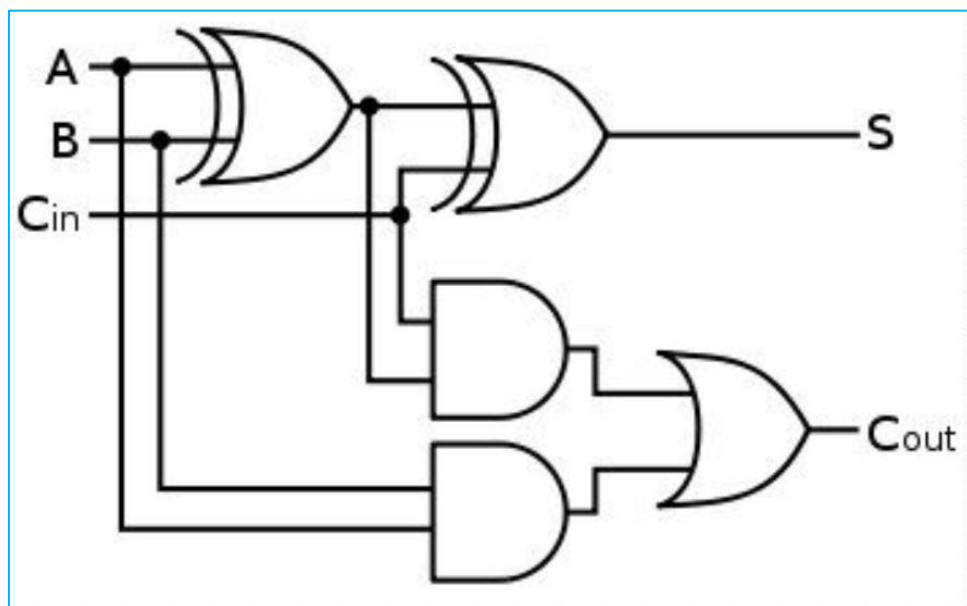
繳交日期:2019/09/24

電路原理

利用一個全加器和 4*1 多工器與邏輯單元 AND,NOR,XOR 組合成一個 1BIT ALU,再利用 1BIT ALU 組合成 4BIT ALU，根據多工具選擇的不同，可作 4 種不同計算方式,當選擇線為 00 時，為加法，當選擇線為 01 時，為 AND，當選擇線為 10 時，為 NOR，當選擇線為 11 時，為 XOR。

電路架構

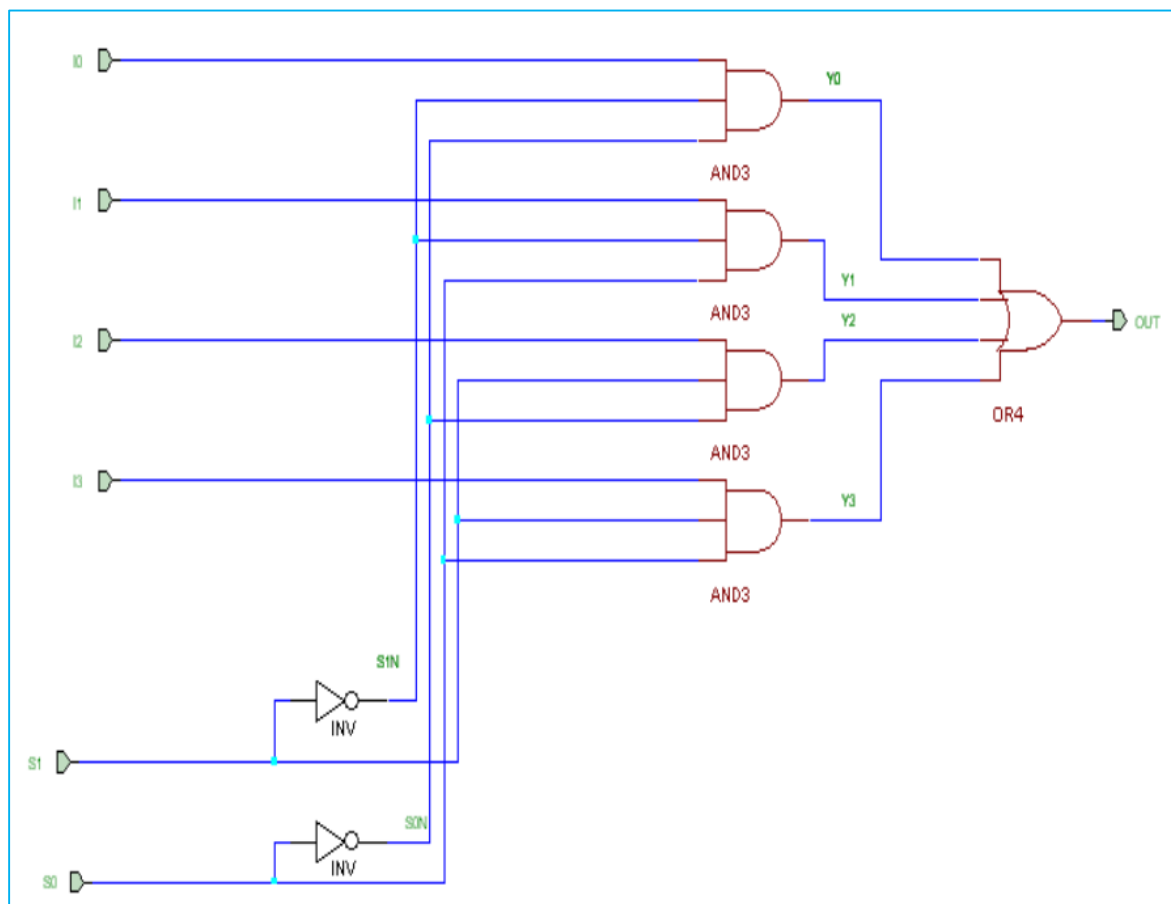
全加器



$$S = AB'Cin' + A'BCin' + A'B'Cin + ABCin$$

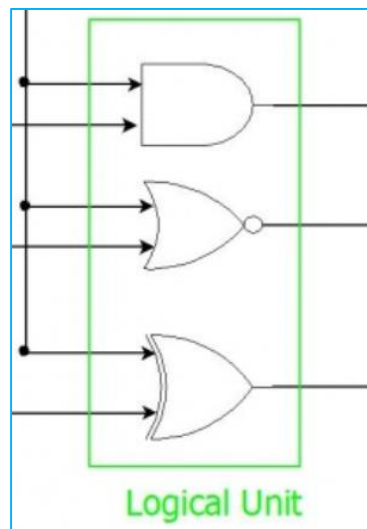
$$Cout = AB + BCin + ACin$$

多工器

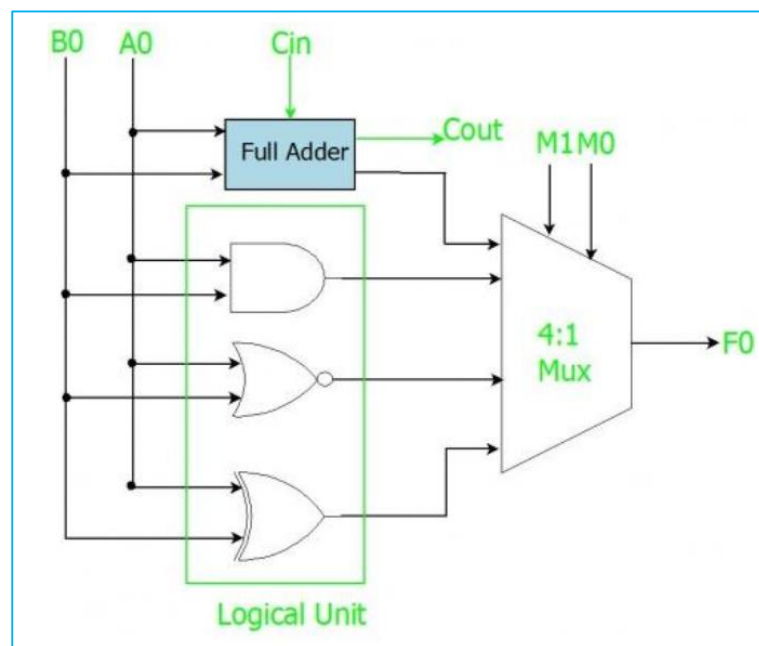


$$OUT = I_0 S_1' S_0' + I_1 S_1' S_0 + I_2 S_0 S_1' + I_3 S_0 S_1$$

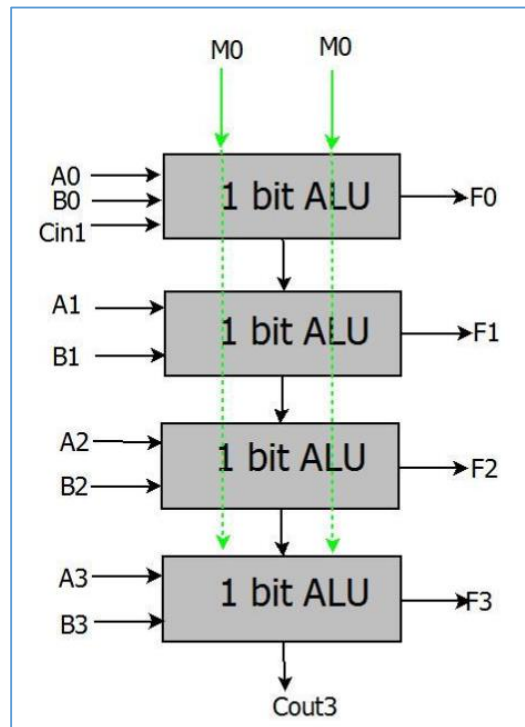
邏輯單元



1 BIT ALU



4 BIT ALU



程式擷取畫面 (含 windows 下方工具列)

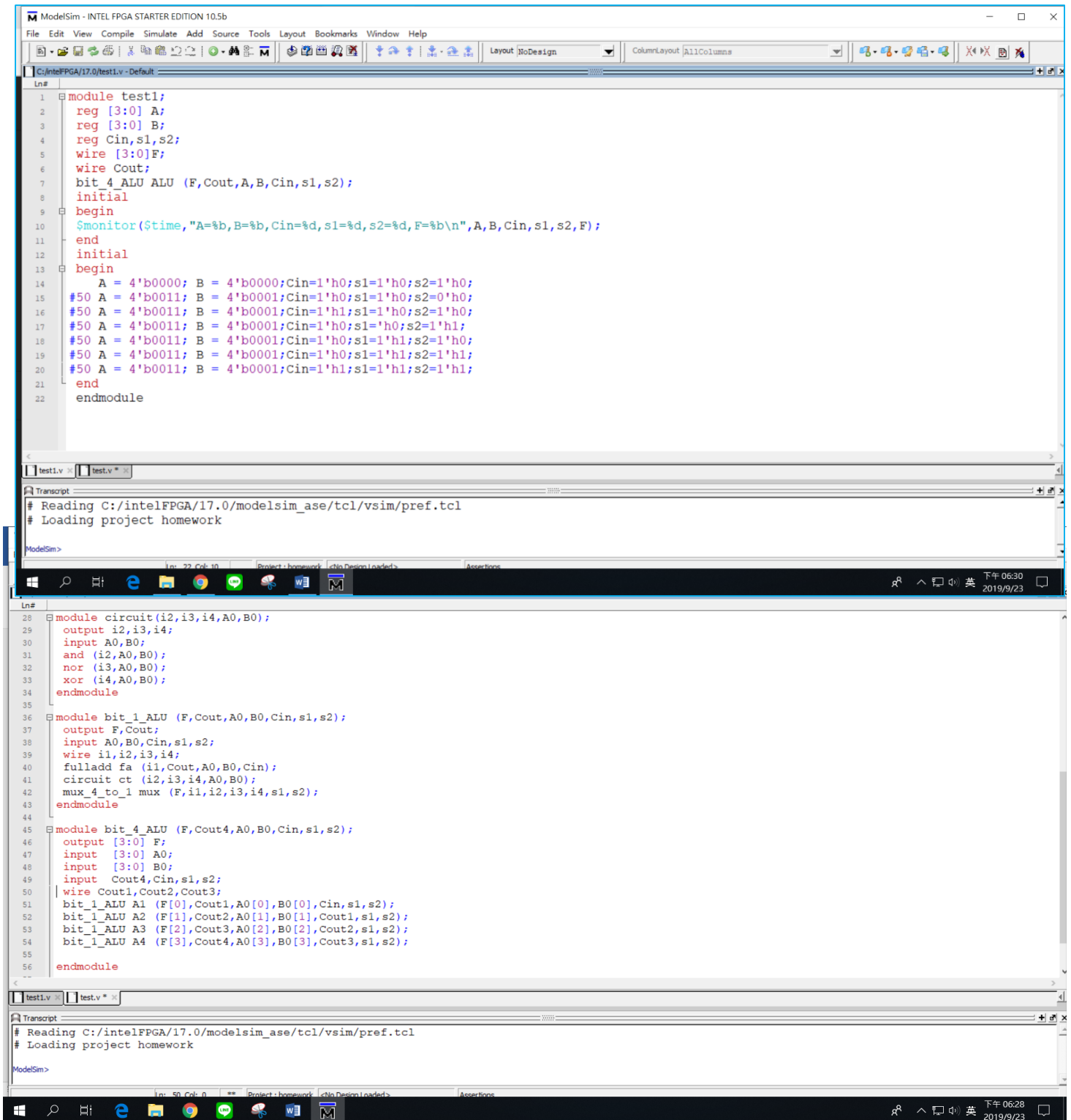
```

ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
C:/intelFPGA/17.0/test.v - Default *
Ln#
1 module mux_4_to_1 (out,i1,i2,i3,i4,s1,s2);
2   output out;
3   input i1,i2,i3,i4;
4   input s1,s2;
5   wire s1w,s2w;
6   wire w1,w2,w3,w4;
7   not (s1w,s1);
8   not (s2w,s2);
9   and (w1,i1,s1w,s2w);
10  and (w2,i2,s1w,s2w);
11  and (w3,i3,s1w,s2w);
12  and (w4,i4,s1w,s2w);
13  or (out,w1,w2,w3,w4);
14
15 endmodule
16
17 module fulladd(i1,Cout,A0,B0,Cin);
18   output i1,Cout;
19   input A0,B0,Cin;
20   wire w5,w6,w7;
21   xor (w5,A0,B0);
22   and (w6,A0,B0);
23   xor (i1,w5,Cin);
24   and (w7,w5,Cin);
25   xor (Cout,w7,w6);
26 endmodule
27
28
29
< test1.v test.v *
Transcript
# Reading C:/intelFPGA/17.0/modelsim_ase/tcl/vsim/pref.tcl
# Loading project homework
ModelSim>

```

多工器與全加器的主程式

邏輯單元與 1BIT ALU 與 4BIT ALU 的主程式



```
1 module test1;
2   reg [3:0] A;
3   reg [3:0] B;
4   reg Cin,s1,s2;
5   wire [3:0] F;
6   wire Cout;
7   bit_4_ALU ALU (F,Cout,A,B,Cin,s1,s2);
8   initial
9   begin
10    $monitor($time,"A=%b,B=%b,Cin=%d,s1=%d,s2=%d,F=%b\n",A,B,Cin,s1,s2,F);
11  end
12  initial
13  begin
14    A = 4'b0000; B = 4'b0000;Cin=1'h0;s1=1'h0;s2=1'h0;
15    #50 A = 4'b0011; B = 4'b0001;Cin=1'h0;s1=1'h0;s2=0'h0;
16    #50 A = 4'b0011; B = 4'b0001;Cin=1'h1;s1=1'h0;s2=1'h0;
17    #50 A = 4'b0011; B = 4'b0001;Cin=1'h0;s1=1'h0;s2=1'h1;
18    #50 A = 4'b0011; B = 4'b0001;Cin=1'h0;s1=1'h1;s2=1'h0;
19    #50 A = 4'b0011; B = 4'b0001;Cin=1'h0;s1=1'h1;s2=1'h1;
20    #50 A = 4'b0011; B = 4'b0001;Cin=1'h1;s1=1'h1;s2=1'h1;
21  end
22 endmodule
```

```
28 module circuit(i2,i3,i4,A0,B0);
29   output i2,i3,i4;
30   input A0,B0;
31   and (i2,A0,B0);
32   nor (i3,A0,B0);
33   xor (i4,A0,B0);
34 endmodule
35
36 module bit_1_ALU (F,Cout,A0,B0,Cin,s1,s2);
37   output F,Cout;
38   input A0,B0,Cin,s1,s2;
39   wire i1,i2,i3,i4;
40   fulladd fa (i1,Cout,A0,B0,Cin);
41   circuit ct (i2,i3,i4,A0,B0);
42   mux_4_to_1 mux (F,i1,i2,i3,i4,s1,s2);
43 endmodule
44
45 module bit_4_ALU (F,Cout4,A0,B0,Cin,s1,s2);
46   output [3:0] F;
47   input [3:0] A0;
48   input [3:0] B0;
49   input Cout4,Cin,s1,s2;
50   wire Cout1,Cout2,Cout3;
51   bit_1_ALU A1 (F[0],Cout1,A0[0],B0[0],Cin,s1,s2);
52   bit_1_ALU A2 (F[1],Cout2,A0[1],B0[1],Cout1,s1,s2);
53   bit_1_ALU A3 (F[2],Cout3,A0[2],B0[2],Cout2,s1,s2);
54   bit_1_ALU A4 (F[3],Cout4,A0[3],B0[3],Cout3,s1,s2);
55 endmodule
```

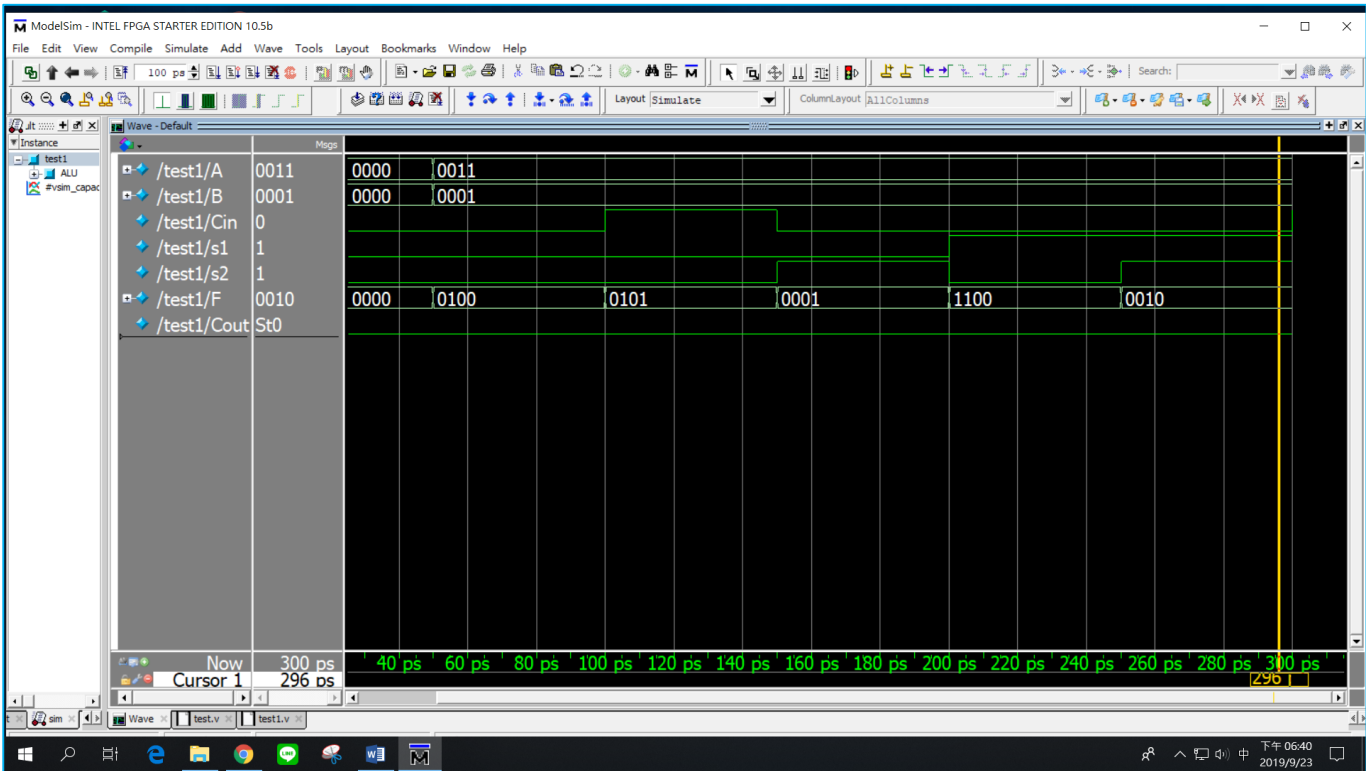
模擬程式

執行結果

```
Transcript
File Edit View Bookmarks Window Help

# Reading C:/intelFPGA/17.0/modelsim_ase/tcl/vsim/pref.tcl
# Loading project homework
# Compile of test.v was successful.
# Compile of test1.v was successful.
# 2 compiles, 0 failed with no errors.
ModelSim> Vsim -gui work.test1
# vsim -gui work.test1
# Start time: 18:33:55 on Sep 23, 2019
# Loading work.test1
# Loading work.bit_4_ALU
# Loading work.bit_1_ALU
# Loading work.fulladd
# Loading work.circuit
# Loading work.mux_4_to_1
VSIOM 2> run -all
#
#          0A=0000,B=0000,Cin=0,s1=0,s2=0,F=0000
#
#          50A=0011,B=0001,Cin=0,s1=0,s2=0,F=0100
#
#          100A=0011,B=0001,Cin=1,s1=0,s2=0,F=0101
#
#          150A=0011,B=0001,Cin=0,s1=0,s2=1,F=0001
#
#          200A=0011,B=0001,Cin=0,s1=1,s2=0,F=1100
#
#          250A=0011,B=0001,Cin=0,s1=1,s2=1,F=0010
#
#          300A=0011,B=0001,Cin=1,s1=1,s2=1,F=0010
#
VSIOM 3>
```

模擬結果



模擬波形

心得(100 字以上)

這一次是第一次接觸到硬體描述語言，雖然之前有一點寫程式的經驗，但是還是有些生疏，要花不少時間去理解，在過程中遇到了很多問題，有些是很難自己發覺的，很容易就會陷入窘境，而透過細心思考與利用工具找尋資料，幫助了我在這方面的問題，問題解決了之後更是有一種莫大的成就感，期待在之後的課程中能學到更多的知識。