SHANGKORONG KHALING

"Thinking fuels exploration by raising more questions than answers, opening new avenues for discovery."

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LinkedIn Portfolio GitHub

CAREER OBJECTIVE

Highly motivated and dedicated individual, equipped with contemporary and cultivated engineering skills, proficient management acumen, and a robust technical foundation, seeks to secure a challenging position within your esteemed organization.

EDUCATION

B.Tech in ECE

2018 - 2022

Panipat Institute of Engineering and Technology, Samalkha, Haryana, India.

Percentage: 75%

TECHNICAL SKILLS

- **HDL'S :** VERILOG
- **HVL :** SYSTEM VERILOG
- **TB METHODOLOGY :** UVM
- **DOMAIN :** Digital Electronics, Bus Protocols.
- **TECHNOLOGY PROTOCOLS :** APB, AHB, AXI, EthernetMAC, FIFO, Memory.
- **OPERATING SYSTEM :** LINUX (COMMANDS, GVIM EDITOR).

TOOLS & LANGUAGE

- MODEL SIM
- QUESTA SIM
- GVIM
- GIT VERSION CONTROL
- PYTHON
- C++

INTERPERSONAL SKILLS

- CRITICAL THINKING
- EXCELLENT ANALYTICAL SKILLS
- VERY GOOD INTERPERSONAL COMMUNICATION
- VERY GOOD LISTENING SKILLS
- VERY GOOD COMPUTER SKILLS
- EXCELLENT RESEARCH AND ANALYSIS

FIELD OF INTEREST

- SYSTEM ON CHIP (SOC)
- DIGITAL INTEGRATED CIRCUIT DESIGN
- ANALOG INTEGRATED CIRCUIT DESIGN

EXPERIENCE AND PROJECTS

1. **Design and verification of configurable memory (front door & back door access)**
   - Developed a parameterized memory block with configurable depth, width, and size using verilog.
   - Designed and verified multiple test cases.
   - **Tools & Language used:** Modelsim, Questasim, Verilog and System Verilog.
   - **Methodology:** UVM
2. **Design and Verification of Synchronous and Asynchronous FIFO**
   - Designed a FIFO for communication between modules operating at different clock frequencies.
   - Verified functionality with synchronous and asynchronous clock domains using Verilog testbenches.
   - **Tools & Language used:** Modelsim, Questasim, Verilog and System Verilog.
   - **Methodology:** UVM
3. **Design and Verification of Mealy and Moore FSM Sequence Detector**
   - Implemented Mealy and Moore FSMs for sequence detection based on state diagrams.
   - Verified design functionality using Verilog testbenches.
   - **Tools & Language used:** Modelsim, Questasim, Verilog and System Verilog.
   - **Methodology:** UVM
4. **APB, AHB and AXI Protocol Understanding and Verification**
   - Gained an in-depth understanding of the APB (Advanced Peripheral Bus) protocol, AHB (Advanced High-performance Bus) protocol for efficient communication between master and slave components and AXI (Advanced eXtensible Interface) protocol for high-speed data transfer.
   - Verified the protocols for communication between master and slave components by ensuring proper data transfer and handshaking.
   - Developed Verilog-based testbenches to verify proper burst transfers, handshaking, and data integrity in the AHB and AXI protocols.
   - **Tools & Language used:** Modelsim, Questasim, Verilog and System Verilog.
   - **Methodology:** UVM
5. **Memory Design and Verification with Multiple Agents**
   - Designed a memory module and verified it using testbenches with single and multiple agents.
   - Applied semaphores to avoid race conditions during concurrent access.
   - Developed testbench components including generator, BFM, monitor, assertions, and checkers to ensure thorough verification.
   - **Tools & Language used:** Modelsim, Questasim, Verilog and System Verilog.
   - **Methodology:** UVM
6. **Design and Verification of Synchronous FIFO with Test Bench**

RESEARCH INTEREST

- NEUROMORPHIC COMPUTING
- BIO-INSPIRED VLSI DESIGN
- ENERGY-EFFICIENT VLSI DESIGN
- FAULT TOLERANT VLSI DESIGN
- NETWORK ON CHIP (NOC) ARCHITECTURES MEMORY DESIGN AND OPTIMIZATION

TRAINING & OTHER SKILLS

- AI, ML & DL
- INTEL OPENVINO VERIFICATION
- AWS BUILDERS SERIES
- AWS INNOVATE
- PCB DESIGNING
- STM CUBE
- IOT
- AUTOCAD
- MATLAB

ADDITIONAL TRAINING

- DATA SCIENCE

- Designed a synchronous FIFO and developed a testbench to verify the design.
- Implemented a comprehensive testbench with generator, monitor, and coverage to check memory read/write operations.
- **Tools & Language used:** Modelsim, Questasim, Verilog and System Verilog.
- **Methodology:** UVM

7. **Development of UVM Test Bench from Scratch (Memory, FIFO, APB, AHB, AXI)**
   - Developed UVM testbenches from scratch to verify memory, FIFO, AHB, and AXI designs.
   - Created essential UVM components including driver, monitor, scoreboard, and coverage components to ensure thorough verification and coverage metrics.
   - **Tools & Language used:** Modelsim, Questasim, Verilog and System Verilog.
   - **Methodology:** UVM
8. **Design and Implementation of a Pipelined MIPS32 Processor**

   Overview: Designed and implemented a basic pipelined MIPS32 processor using Verilog, incorporating a small subset of instructions.

   Specifications:

   1. 32x32-bit General Purpose Registers (GPRs): 32 registers (R0 to R31), with two read ports and one write port.
   2. Register R0: Contains a constant 0 and is write-protected.
   3. Program Counter (PC): 32-bit special-purpose register to track the next instruction for execution.
   4. No flag registers: The processor does not use zero, carry, sign, or other status flags.
   5. Addressing Modes: Supports basic addressing modes such as register, immediate, and register-indexed addressing.
   6. Memory Access: Only load and store instructions can access memory.
   7. Memory Assumptions: 32-bit word addressable memory.

   Key Features:

   - Implemented basic pipeline stages to improve instruction throughput.
   - Verified the design using a Verilog testbench to ensure correct instruction execution and pipeline behavior.
   - Focused on basic instructions and streamlined memory access for efficient data handling.
   - **Tools & Language used:** Verilog
9. **Design and Implementation of a 16x16-bit ALU with Four-Stage Pipeline**
   - Developed a 16x16-bit ALU with a four-stage pipeline, utilizing non-overlapping two-phase clocks (clk1 and clk2) for optimized pipelining.
   - Integrated 16x16-bit register bank and 256x16-bit memory.
   - Key features:
     - **Inputs**: 3 register addresses (rs1, rs2, rd), an ALU function (func), and a memory address (addr).
     - **Stages**:
       1. **Stage 1**: Read two 16-bit numbers from registers and store them in A and B.
       2. **Stage 2**: Perform ALU operation (based on func) on A and B, storing result in Z.
       3. **Stage 3**: Write Z into the destination register (rd).
       4. **Stage 4**: Write Z into memory at location "addr".
     - **ALU Operations**: Supported operations include ADD, SUB, MUL, AND, OR, XOR, shifts (SRA, SLA), and others.
   - Achieved efficient memory access using 256x16-bit memory and 16x16-bit registers, with support for two reads and one write per cycle.
   - **Tools & Language used:** Verilog
10. **EthernetMAC protocol**
    - Implemented a UVM-based verification environment to validate the ethernet mac module developed in Verilog. Focused on verifying register configuration, write/read access, and reset handling through comprehensive UVM testcases.

- Designed and implemented UVM driver logic to generate protocol-compliant register transactions and monitor MAC behavior. Test scenarios included write/read to configuration and status registers, reset to ensure proper initialization and operational correctness. The UVM environment included sequencers, drivers, monitors, and a scoreboard to check end-to-end data flow and register-level accuracy. Simulated and debugged using Questa Sim.
- **Tools & Language used:** Modelsim, Questasim, Verilog and System Verilog.
- **Methodology:** UVM

SCHOLARSHIPS

- 2nd Rank (ST category, State) in **National Talent Search Examination (NTSE)** – **High School**
- Panipat Institute of Engineering and Technology **Career Acceleration Programme (CAP)** - **Undergraduate**

ACHIEVEMENTS AND AWARDS.

- Got Distinction in Mathematics in **International Assessments For Indian Schools (IAIS)** – **High School**
- 1st Rank **Crossword competition** held by ECE department Panipat Institute of Engineering and Technology – **Undergraduate**
- 3rd Rank **Speech competition on Human Rights Day** held by ECE department Panipat Institute of Engineering and Technology - **Undergraduate**

EXPERIENCE AND PROJECTS

Quadcopter Designing.

2018-2019

During my first year of undergraduate studies, I successfully completed a project on quadcopter design and construction. This experience provided valuable insights into the intricacies of achieving flight. The project involved working with **PID controllers, wireless communication, PWM modulation, and firmware programming**. Overall, it was a rewarding endeavor that significantly expanded my knowledge in this field.

Churn modelling using Artificial Neural Network (ANN).

2020-2021

I developed a predictive model using an **Artificial Neural Network (ANN)** to assess individual customers' propensity to churn, i.e., their likelihood of leaving. The model acts as a binary classifier, categorizing customers into two groups: those who are likely to churn and those who are not. Additionally, the model provides the probability of a customer belonging to each group. This project involved training and testing the ANN on a **dataset comprising 10,000+ customer** records from a bank.

Automatic Number Plate Recognition (ANPR) RTLS System - 2022

In my research, I explored the challenges associated with Automatic Number Plate Recognition (ANPR) systems. These systems face difficulties in handling factors such as high-speed vehicles, non-uniform number plates, diverse languages on plates, and varying lighting conditions, all of which can impact the recognition rate. While many existing ANPR systems operate within these limitations, my paper focused on **a novel approach that utilizes UHF active RFID for Real-Time Location System (RTLS)**. The approach was evaluated based on parameters such as success rate and processing time.

RESEARCH WORKS

Accent Classification of 3 Indian Languages (Bangla, Malayalam, and Telugu) using LSTM CNN 1D.

2021 - 2022

This research project was conducted under the guidance of **Ms. Swati Gupta**, Head of the Department of Electronics and Communication Engineering at P.I.E.T., and **Dr. Ayodeji Olalekan Salau** from the Department of Electrical/Electronics and Computer Engineering at Afe Babalola University. Accent classification poses a significant challenge in **Natural Language Processing (NLP)** and plays a vital role in **Automatic Speech Recognition (ASR) systems**, greatly enhancing their performance. This research provided me with comprehensive knowledge on the production of sounds and speech by vocal cords, offering new perspectives and deep admiration for these acoustic phenomena. Working with AI on this invaluable research project was truly a rewarding experience.

ADDITIONAL WORKS

Digital Calculator for physically challenged.

2020-2021

Developed and designed a user-friendly digital calculator specifically tailored for individuals with physical disabilities, which **seamlessly integrates with wheelchair interfaces**. The joystick-operated digital calculator offers enhanced accessibility, providing a convenient solution for users to perform calculations without any limitations.

Music/Audio Genre Classification using RNN-LSTM.

2020-2021

Audio processing is a complex task within data science, presenting unique challenges compared to image processing and other classification techniques. My passion for music and experience with digital synthesizers and DAWs inspired me to explore audio processing further. Using **TensorFlow and Keras**, I undertook a project that involved training a **Recurrent Neural Network - Long Short Term Memory (RNN-LSTM)** model to classify various music genres. This project entailed working with a **dataset of over 10,000 audio samples spanning multiple genres.** Through this experience, I gained a deeper appreciation for the intricate computation involved in identifying different types of sounds and music, paralleling the effortless abilities of the human brain.

Image classification using CNN.

2020-2021

Image classification is the process of categorizing and labeling groups of pixels or vectors within an image based on specific rules. The categorization law can be devised using one or more spectral or textural characteristics. Two general methods of classification are 'supervised' and 'unsupervised'. In this project, a CNN model is used to classify between different animals. The model is trained and tested using images of various animals.

Music Genre Classification using CNN

2020

Music genre classification aims to classify the audio files in certain categories of sound to which they belong. The application is very important and requires automation to reduce the manual error and time because if we have to classify the music manually then one has to listen out each file for the complete duration.
In this project Convolutional Neural Networks (CNN) is used to classify different genres of the music. Model is **trained and tested on 10000+ music samples collected across all genres.**

ANPR using Computer Vision and RFID.

2022

The issue of traffic control and vehicle owner identification has emerged as a significant concern globally. Identifying vehicle owners who violate traffic rules and exceed speed limits can be particularly challenging. The high speed of vehicles hampers the ability of traffic personnel to retrieve the vehicle number, making it difficult to apprehend and penalize offenders. To address this issue, the development of an Automatic Number Plate Recognition (ANPR) system is essential. In this project, I employed OpenCV and RFID technologies for identification of the vehicles.