

Project Report: Land rover Figo FSM Design

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Abstract: This project aims to design a Finite State Machine (FSM) for testing the latest ISRO campus. The FSM receives wireless travel plans from ISRO, guiding the Figo to different locations based on the transmitted information. Each location is assigned a state using a 3-bit binary representation. The FSM transitions between states according to a binary sequence received from ISRO, where '0' denotes a clockwise movement and "1" represent anticlockwise movement. The FSM output provides the current location of the Figo.

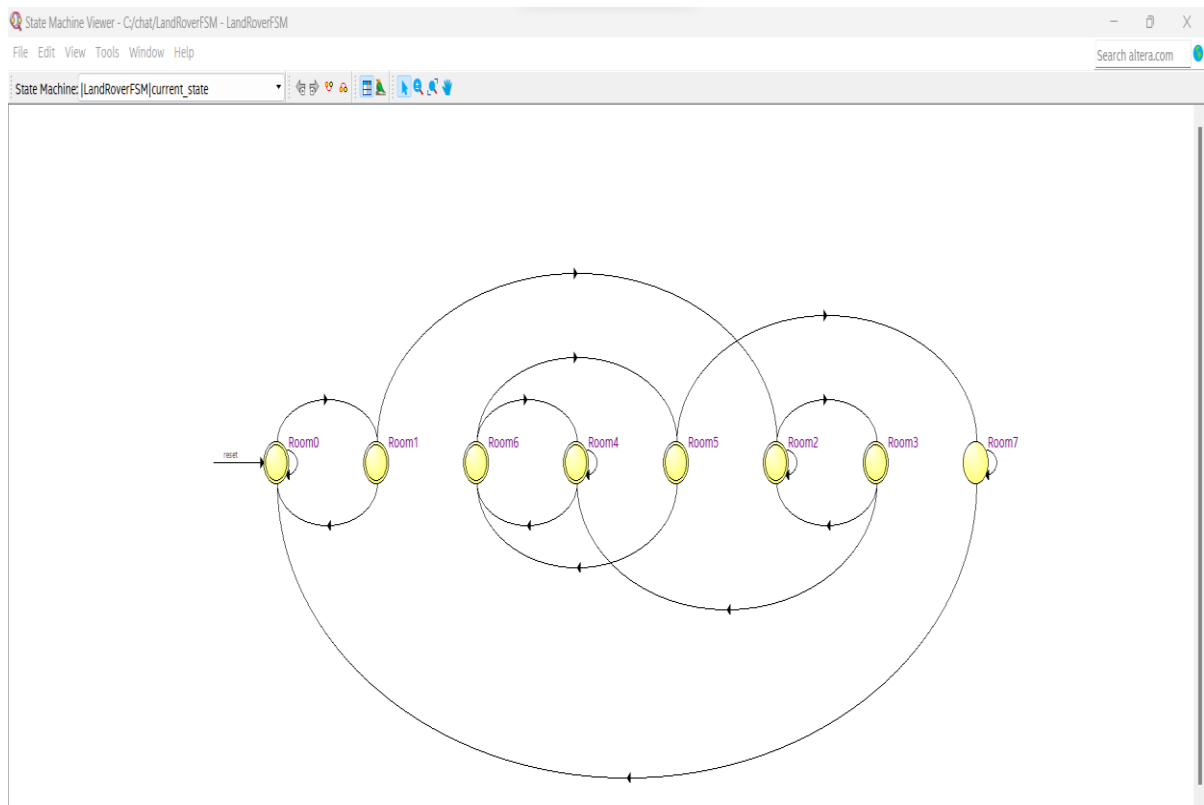
Introduction

To design a FSM, a set of location around the ISRO campus has been selected, with each location assigned a state representation by a 3-bit binary code. These locations include Room0[000], Room1[001], Room2[010], Room3[011], Room4[100], Room5[101], Room6[110], Room7[111]. The FSM will use these states to determine the Figo's current location as it moves through ISRO campus.

The FSM output will provide information about the current location of the Figo based on the assigned states.

Room0[000]	If 0, stay at Room0	If 1, go to Room1
Room1[001]	If 0, go to Room2	If 1, go to Room4
Room2[010]	If 0, go to Room3	If 1, go to Room4
Room3[011]	If 0, stay at Room3	If 1, go to Room0
Room4[100]	If 0, go to Room7	If 1, go to Room5
Room5[101]	If 0, go to Room3	If 1, go to Room6
Room6[110]	If 0, go to Room7	If 1, stay at Room6
Room7[111]	If 0, go to Room1	If 1, go to Room5

State Diagram



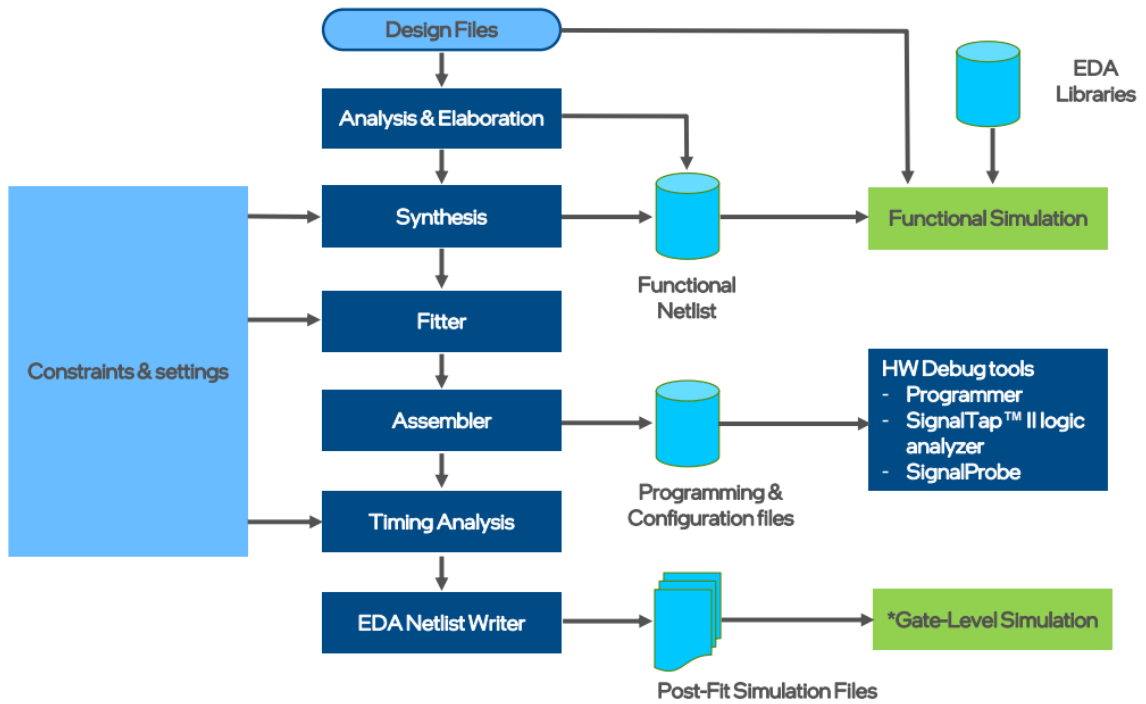
Objective

The objective of this project is to design a Finite State Machine (FSM) and develop Verilog code for the FSM to test the newest Land Rover Figo on the ISRO campus. The FSM will receive wireless travel plans transmitted by ISRO and guide the Figo according to the received information. The primary goal is to ensure that the Figo moves to the specified locations as instructed.

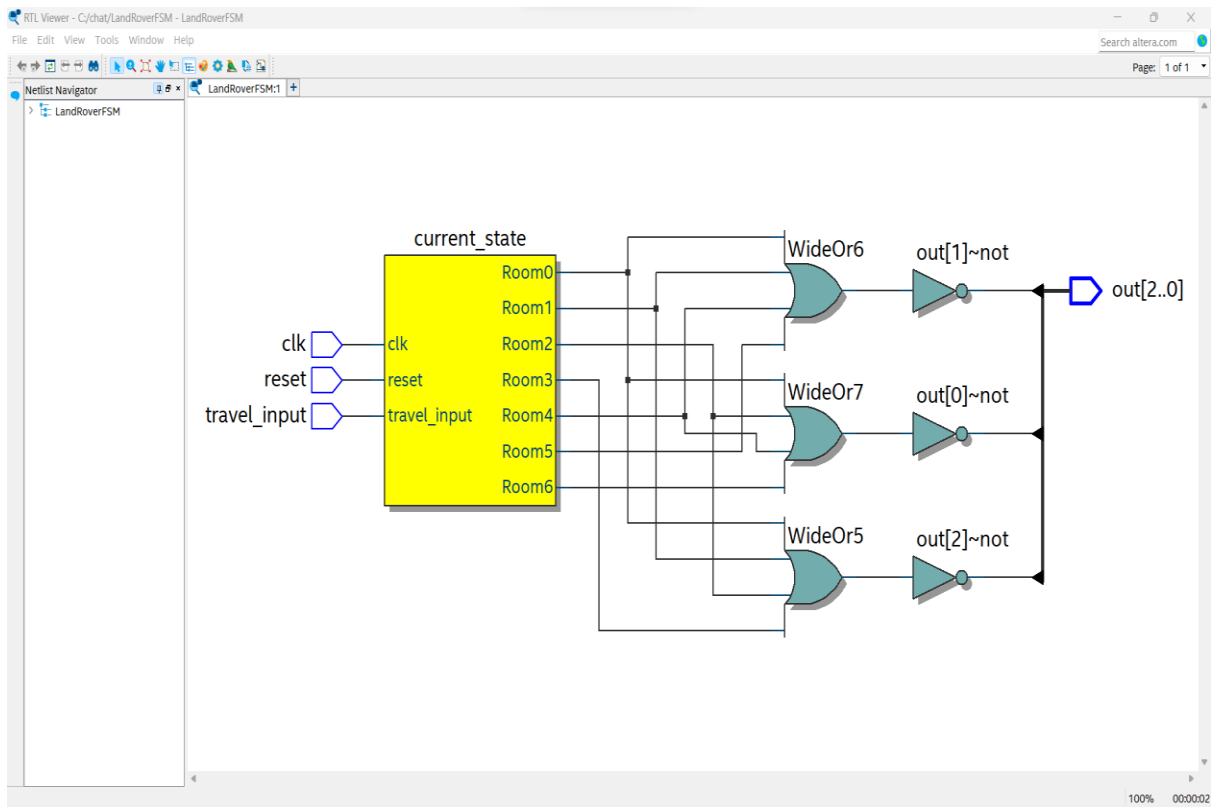
To achieve this objective, the following tasks will be accomplished:

1. **FSM Design:** The FSM will be designed to incorporate the assigned locations around the ISRO campus, where each location is represented by a 3-bit binary code. This design will enable the FSM to accurately interpret the travel plans and guide the Figo to the appropriate destinations.
2. **Verilog Code Development:** The FSM will be implemented using the Verilog hardware description language. The Verilog code will capture the state transitions, input handling, and output generation logic of the FSM. The code will be designed to efficiently handle the binary sequences representing the travel plans and produce the Figo's current location as the output.
3. **Communication Interface:** The Verilog code will include a communication interface that enables the FSM to receive wireless travel plans transmitted by ISRO. This interface will ensure seamless communication between the FSM and the ISRO system.
4. **Travel Plan Interpretation:** The Verilog code will interpret the received binary sequence representing the travel plans. Each '0' or '1' in the sequence will correspond to a move instruction, indicating whether the Figo should move in a clockwise or anticlockwise direction. The code will accurately process these instructions and guide the Figo to the next destination.
5. **Current Location :** The Verilog code will generate an output that indicates the current location of the Figo. By utilizing the assigned states corresponding to the locations, the code will provide real-time information about the Figo's position on the ISRO campus.

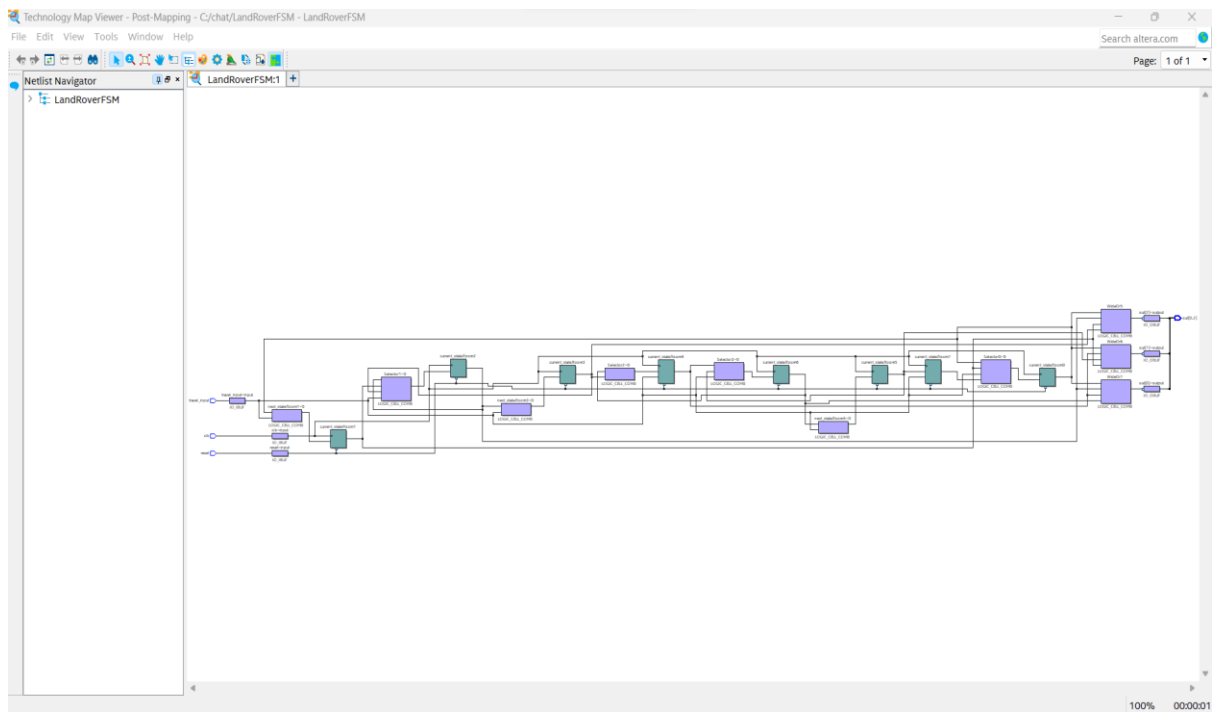
Tool Flow



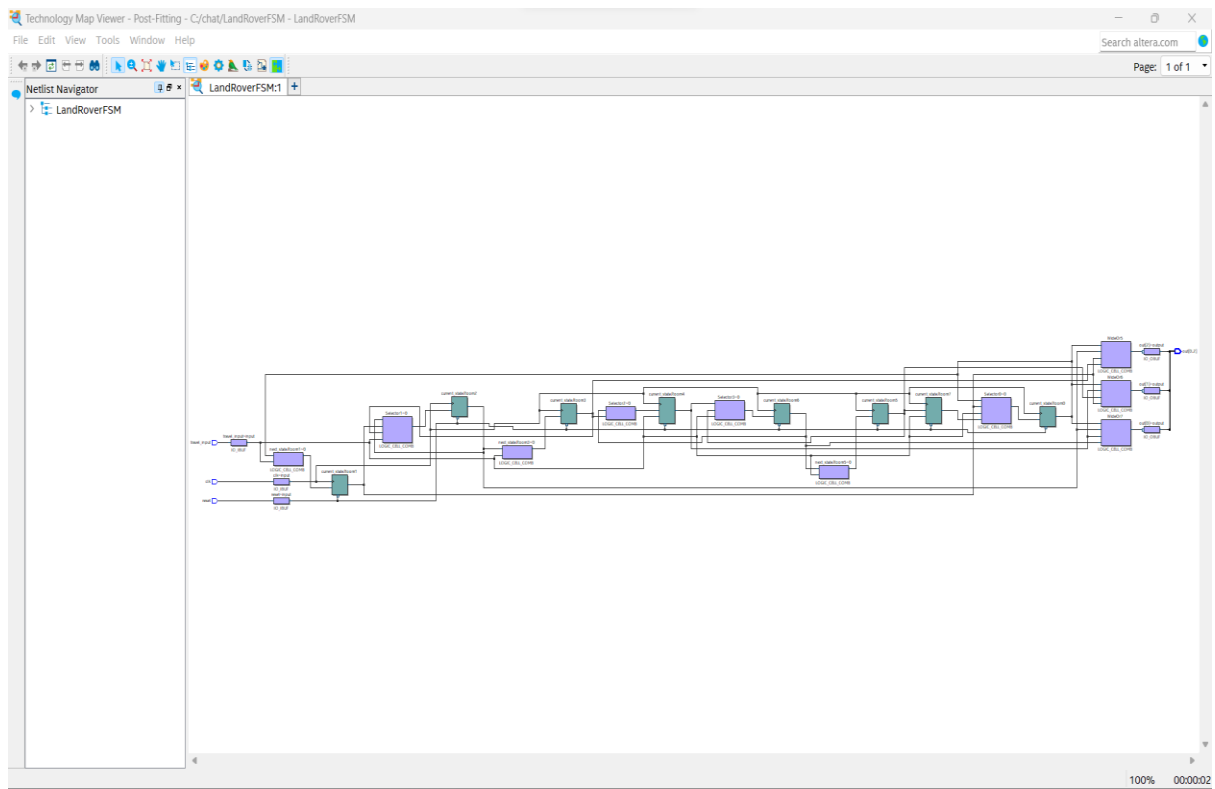
RTL Viewer



Technology Map Viewer(Post-Mapping)



Technology Map Viewer(Post-Fitting)



Reference Paper

1. "Digital Design and Computer Architecture" by David Money Harris and Sarah L. Harris (Link: <https://www.sciencedirect.com/book/9780123704979/digital-design-and-computer-architecture>).

2. "Fundamental of Digital Logic with Verilog Design" by Stephen D. Brown and Zvonko G. Vranesic (Link: <https://notesavior.files.wordpress.com/2018/02/stephen-brown-and-zvonko-vranesic-fundamental-of-digital-logic-with-verilog-design.pdf>).