Sri Shanmugha College of Engineering and Technology

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Pullipalayam, Sankari, Salem (Dt.)

Department of Electronics and Communication Engineering

EC8461 - CIRCUITS AND SIMULATION INTEGRATED LABORATORY

LAB MANUAL

REGULATION : 2017

Prepared by

(M.SARANYA, AP/ECE)

EC8461 - Circuits and Simulation Integrated Laboratory L P T C

0 0 4 2

LIST OF EXPERIMENTS

DESIGN AND ANALYSIS OF THE FOLLOWING CIRCUITS

1. Series and Shunt feedback amplifiers-Frequency response, Input and output impedance calculation
2. RC Phase shift oscillator and Wien Bridge Oscillator
3. Hartley Oscillator and Colpitts Oscillator
4. Single Tuned Amplifier
5. RC Integrator and Differentiator circuits
6. Astable and Monostable multivibrators
7. Clippers and Clampers

SIMULATION USING SPICE (Using Transistor):

1. Tuned Collector Oscillator
2. Twin -T Oscillator / Wein Bridge Oscillator
3. Double and Stagger tuned Amplifiers
4. Bistable Multivibrator
5. Schmitt Trigger circuit with Predictable hysteresis
6. Analysis of power Amplifiers.

TOTAL: 45 PERIODS

Course outcomes:

CO 1	Analyze various types of feedback amplifiers
CO 2	Design oscillators, tuned amplifiers
CO 3	Design wave-shaping circuits.
CO 4	Design multi vibrators
CO 5	Design and simulate feedback amplifiers, oscillators, tuned amplifiers, wave-shaping circuits and multivibrators using SPICE Tool.

CO PO, PSO Mappings

Course Code and Course name	**CO**	**Program Outcomes**												**PSO**		
		1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**1**	**2**	**3**
EC8461 Circuits And Simulation Integrated Laboratory	**CO 1**	3	2	2	2	3	2	-	-	3	3	-	1	3	3	3
	CO 2	3	2	2	2	3	2	-	-	3	2	-	2	3	3	3
	CO 3	3	2	2	2	3	2	-	-	2	3	-	2	3	3	3
	CO 4	3	2	2	3	3	2	-	-	3	3	-	3	3	3	3
	CO 5	3	2	3	3	3	2	-	-	3	2	-	2	3	3	3
Average		3	2	2	2.4	3	2	-	-	3	3	-	2	3	3	3

CONTENTS

Ex. No.: 1.a Date:	CURRENT SERIES FEEDBACK AMPLIFER

AIM:

To design a negative feedback amplifier and to draw its frequency response.

APPARATUS REQUIRED:

S.No	EQUIPMENTS	RANGE	QUANTIT Y
1	Function generator	(0-1)MHz	1
2	CRO	(0-20)MHz	1
3	Resistors	1.5 KΩ, 6KΩ, 2KΩ, 14kΩ, 2.3KΩ, 10KΩ	Each one
4	Power supply	(0-30V)	1
5	Transistors	BC 107	1
6	Capacitors	28μF, 10μF,720μF	1

Design examples:

V_{CC}= 15V, I_C=1mA, A_V= 30, f_L= 50Hz, S=3, hFE= 100, hie= 1.1KΩ

Gain formula is,

$A_V = - h_{FE} R_{Leff} / hie$

Assume, $V_{CE} = V_{CC} / 2$ (transistor in active region)

V_{CE} = 15 /2=7.5V

$V_E = V_{CC} / 10$= 15/10=1.5V

Emitter resistance is given by, re =26mV/ I_E

Therefore r_e =26 Ω

hie= hfe re

hie =2.6KΩ

(i) To calculate R_C:

Applying KVL to output loop,

$V_{CC} = I_C R_C + V_{CE} + I_E R_E$------(1)

Where $R_E = V_E / I_E$ ($I_C = I_E$)

R_E = 1.5 / 1x10-3= 1.5KΩ

From equation (1),

R_C= 6KΩ

(ii) To calculate R_{B1}&R_{B2}:

Since I_B is small when compared with I_C,

$I_C \sim I_E$

$V_B = V_{BE} + V_E = 0.7 + 1.5 = 2.2V$

$V_B = V_{CC} (R_{B2} / R_{B1} + R_{B2})$------(2)

$S = 1 + (R_B / R_E)$

$R_B = 2K\Omega$

We know that $R_B = R_{B1} || R_{B2}$

$R_B = R_{B1}R_{B2} / R_{B1} + R_{B2}$---------(3)

Solving equation (2) & (3),

Therefore,

$R_{B1} = 14K\Omega$

From equation (3), $R_{B2} = 2.3K\Omega$

(iii) To find input coupling capacitor (C_i):

$X_{Ci} = (hie || R_B) / 10$

$X_{Ci} = 113$

$X_{Ci} = 1 / 2\pi f C_i$

$C_i = 1 / 2\pi f X_{Ci}$

$Ci = 1 / 2X3.14X 50 X 113 = 28\mu f$

(iv)To find output coupling capacitor (C_O):

$X_{CO} = (R_C || R_L) / 10$, (Assume $R_L = 10K\Omega$)

$X_{CO} = 375$

$X_{CO} = 1 / 2\pi f CO$

$C_O = 1 / 2x 3.14x 50 x 375 = 8\mu f = 10 \mu f$

(v) To find Bypass capacitor (C_E):

(Without feedback)

$X_{CE} = \{(R_B + hie / 1 + hfe) || R_E\} / 10$

$X_{CE} = 4.416$

$C_E = 1 / 2\pi f XCE$

$C_E = 720 \mu f$

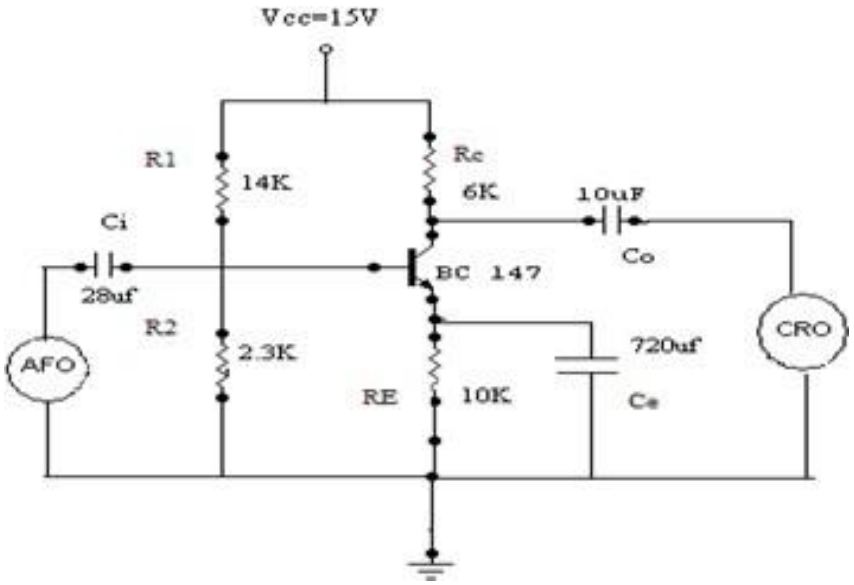
Design with feedback:

To design with feedback remove the bypass capacitor (C_E).

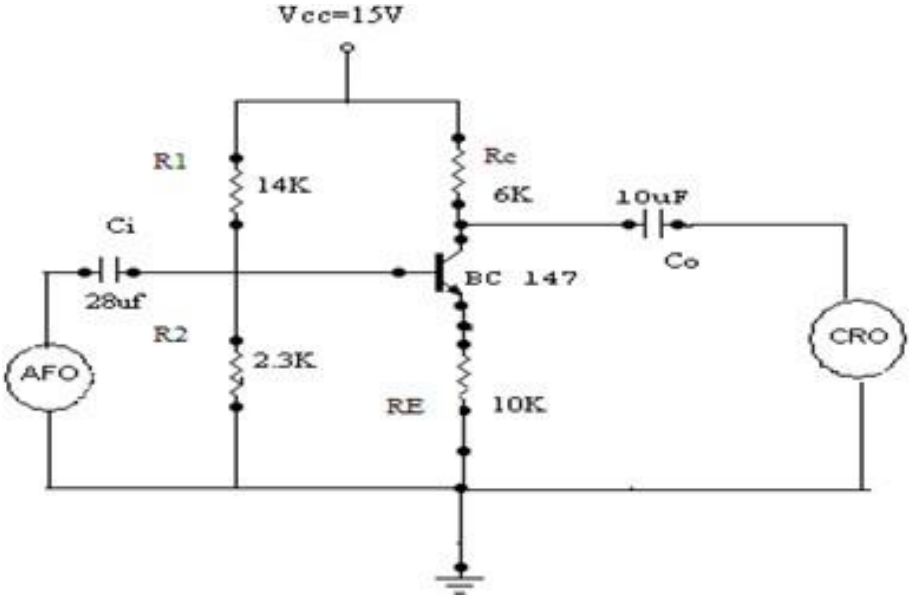
Assume $R_E = 10K\Omega$

CIRCUIT DIAGRAM:

WITHOUT FEED BACK:



WITH FEEDBACK:



MODEL TABULATION:

Without feedback:

Vi=

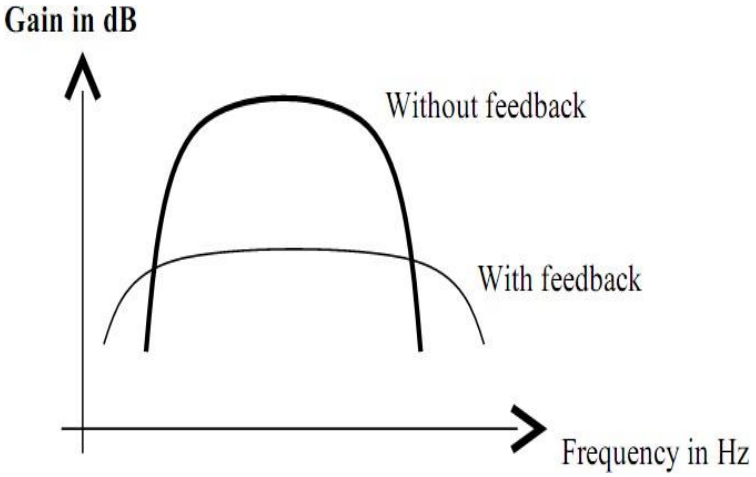
Sl. No	Frequency (Hz)	Output Voltage (V_0) (volts)	Gain = V_0/V_i	Gain = $20\log(V_0/V_i)$ (dB)

With feedback:

Vi=

Sl. No	Frequency (Hz)	Output Voltage (V_0) (volts)	Gain = V_0/V_i	Gain = $20\log(V_0/V_i)$ (dB)

MODEL GRAPH:



THEORY

Negative feedback in general increases the bandwidth of the transfer function stabilized by the specific type of feedback used in a circuit. In Voltage series feedback amplifier, consider a common emitter stage with a resistance R' connected from emitter to ground. This is a case of voltage series feedback and we expect the bandwidth of the trans resistance to be improved due to the feedback through R'. The voltage source is represented by its Norton's equivalent current source Is=Vs/Rs.

PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Set V_{CC} = 10V; set input voltage using audio frequency oscillator.
3. By varying audio frequency oscillator take down output frequency oscillator voltage for difference in frequency.
4. Calculate the gain in dB
5. Plot gain Vs frequency curve in semi-log sheet.
6. Repeat the steps 1 to 6 with feedback
7. Compare this response with respect to the amplifier without feedback.

RESULT:

Thus current series feedback amplifier is designed and studied its performance.

Ex. No.: 1.b Date:	VOLTAGE SHUNT FEEDBACK AMPLIFIER

AIM:

To design and study frequency response of voltage shunt feedback amplifier.

APPARATUS REQUIRED:

S.No	Components	Range	Quantity
1.	Signal generator	(0-30)MHz	1
	CRO	(0-20)V	1
	Regulated Power Supply	(0-30)V	1
2.	Resistor	3kΩ, 1.1 kΩ,5kΩ 2.5 kΩ,1kΩ,	1
	Capacitor	66μF, 30μF,58 μf	1
	Transistors	BC 107	1
3.	Bread board	-	1
	Connecting Wires	Single strand	As required

DESIGN PROCEDURE:

Given specifications:

V_{CC}= 10V, I_C=1.2mA, A_V= 30, f_I = 1 kHz, S=2, h_{FE}= 150, β=0.4

The feedback factor, β= - $1/R_F$= +1/0.4=2.5KΩ

(i) To calculate RC:

The voltage gain is given by,

A_V= -hfe (R_C|| R_F) / hie

h ie = β re

re = 26mV / I_E = 26mV / 1.2mA = 21.6

hie = 150 x 21.6 =3.2K

Apply KVL to output loop,

V_{CC}= I_C R_C + V_{CE}+ I_E R_E ----- (1)

Where V_E = I_E R_E (I_C= I_E)

V_E= V_{CC} / 10= 1V

Therefore R_E= 1/1.2x10-3=0.8K= 1KΩ

$V_{CE}= V_{CC}/2= 5V$

From equation (1), RC= 3 KΩ

(ii) To calculate R_1&R_2:

$S=1+ (R_B/R_E)$

$R_B= (S-1)\ R_E= R_1 \parallel R_2 =1K\Omega$

$R_B= R_1R_2 / R_1+ R_2$------- (2)

$V_B= V_{BE} + V_E = 0.7+ 1= 1.7V$

$V_B= V_{CC}\ R_2 / R_1+ R_2$----- --(3)

Solving equation (2) & (3),

$R_1= 5\ K\Omega$ & $R_2= 1.1K\Omega$

(iii) To calculate Resistance:

Output resistance is given by,

$R_O= R_C \parallel R_F$

$R_O= 1.3K\Omega$

input impedance is given by,

$R_i = (R_B \parallel R_F) \parallel hie = 0.6K\Omega$

Trans-resistance is given by,

$R_m= -hfe\ (R_B \parallel R_F)(\ R_C \parallel R_F) / (R_B \parallel R_F)+ hie$

$R_m= 0.06K\Omega$

AC parameter with feedback network:

(i) Input Impedance:

$R_{if} = R_i /D$ (where $D= 1+\beta\ Rm$)

Therefore D = 25

$R_{if}= 24$

Input coupling capacitor is given by,

$Xci= R_{if} / 10= 2.4$ (since $X_{Ci} << R_{if}$)

$Ci = 1/ 2\pi fX_{Ci} =66\mu f$

(ii) Output impedance:

$R_{Of}= R_O/ D = 52$

Output coupling capacitor:

$X_{CO}=$ Rof /10= 5.2

$C_O = 1/ 2\pi fX_{CO}= 30\mu f$

(iii) Emitter capacitor:

$X_{CE} << R'_E = R'/10$

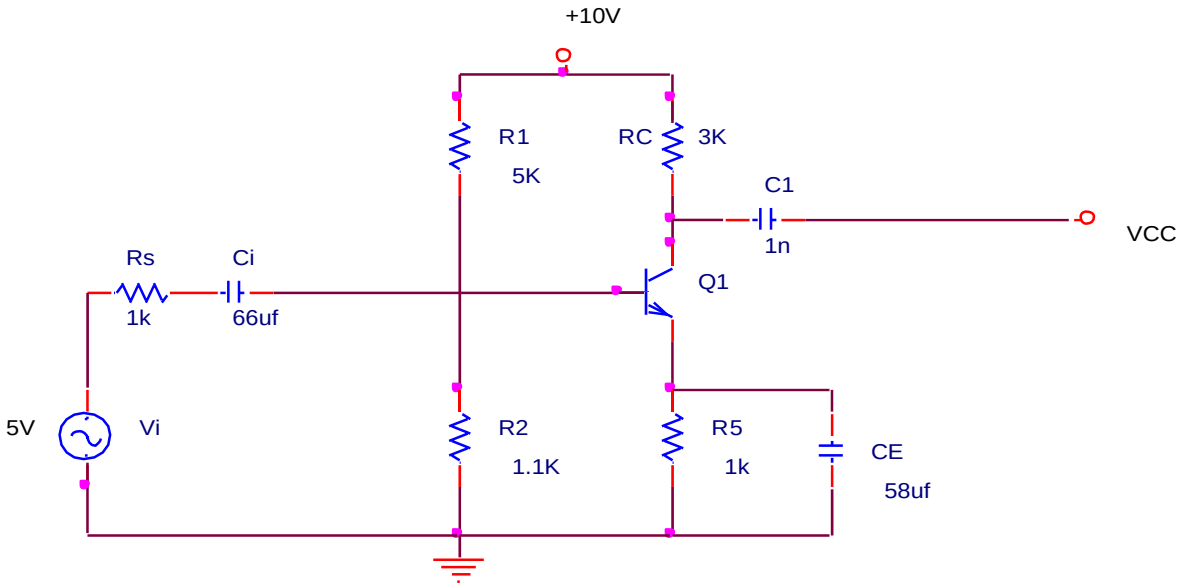
$R'_E= R_E \parallel \{(hie +R_B) / (1+hfe)\}$

$X_{CE}= 2.7$

Therefore $C_E= 58\mu f$

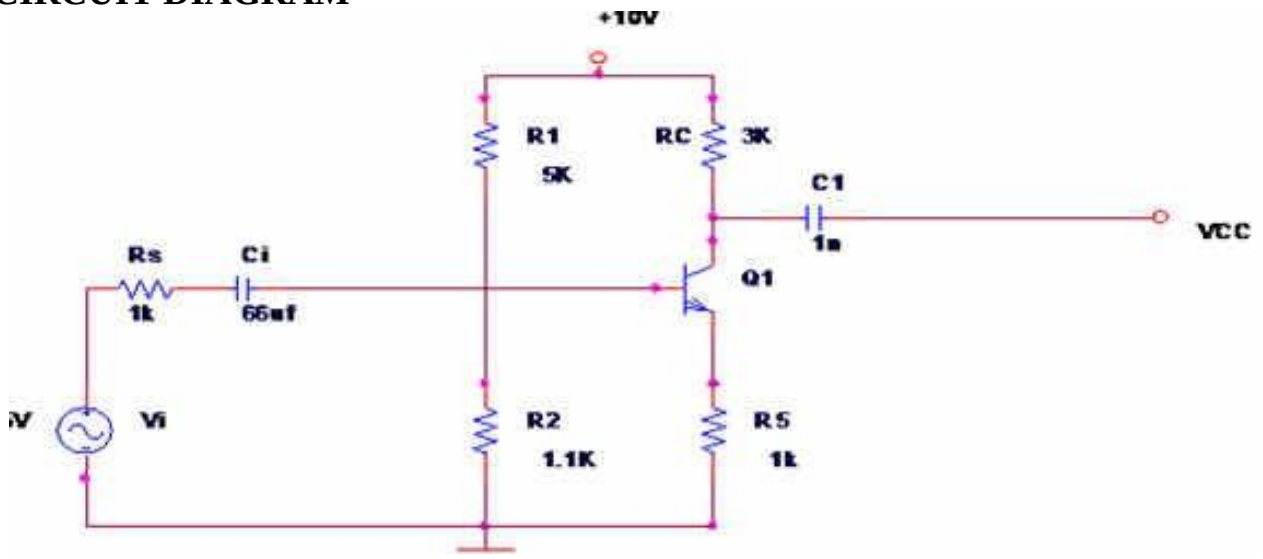
WITHOUT FEED BACK

CIRCUIT DIAGRAM:



WITH FEED BACK

CIRCUIT DIAGRAM



MODEL TABULATION:

Without feedback:

Vi=

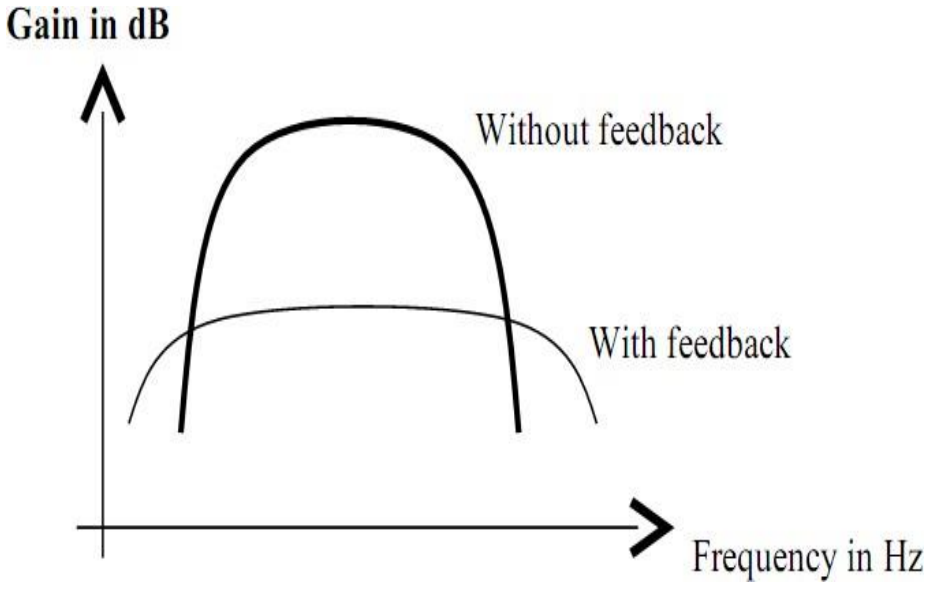
Sl. No	Frequency (Hz)	Output Voltage (V_0) (volts)	Gain = V_0/V_i	Gain = $20\log(V_0/V_i)$ (dB)

With feedback:

Vi=

Sl. No	Frequency (Hz)	Output Voltage (V_0) (volts)	Gain = V_0/V_i	Gain = $20\log(V_0/V_i)$ (dB)

MODEL GRAPH:



THEORY:

Negative feedback in general increases the bandwidth of the transfer function stabilized by the specific type of feedback used in a circuit. In Voltage shunt feedback amplifier, consider a common emitter stage with a resistance R' connected from collector to base. This is a case of voltage shunt feedback and we expect the bandwidth of the Trans resistance to be improved due to the feedback through R'. The voltage source is represented by its Norton's equivalent current source Is=Vs/Rs.

PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Set V_{CC} = 10V; set input voltage using audio frequency oscillator.
3. By varying audio frequency oscillator take down output frequency oscillator voltage for difference in frequency.
4. Calculate the gain in dB
5. Plot gain Vs frequency curve in semi-log sheet.
6. Repeat the steps 1 to 6 with feedback
7. Compare this response with respect to the amplifier without feedback.

RESULT:

Thus voltage shunt feedback amplifier is designed and studied its performance.

Ex. No.: 2.a Date:	RC PHASE SHIFT OSCILLATOR

AIM:

To design a RC phase shift oscillator and to find the frequency of oscillation

APPARATUS REQUIRED:

S. No	Components	RANGE	QUANT ITY
1	Resistors	7.5kΩ,1.4 kΩ 4.8KΩ,1.2KΩ, 19KΩ, 6.5KΩ	1each, 3
2	Power supply	(0-30)V	1
3	Transistor	BC107	1
4	Capacitors	1.3µf , 2.1µf, 1.3µf, 0.01µF	1,1,3
5	CRO	(0-30)MHz	1
6	Bread board	-	1

Design Example:

Specifications:

V_{CC} = 12V, $I_{C}q$ =1mA, β=100, Vceq = 5V, f=1 KHz, S=10, C=0.01 µf, h_{fe}= 330, A_V= 29

Design:

(i) To find R:

Assume f=1 KHz, C=0.01µf

$f=1/2\prod RC\sqrt{6}$

$R=1/2x3.14\sqrt{6}\ x1x10^{3}x0.01x10^{-6}=6.5K\Omega$

Therefore **R=6.5KΩ**

(ii) To find R_E & R_C:

$V_{CE} = V_{CC}/2 = 6V$

$r_e = 26mV / I_E = 26\Omega$

$h_{ie} = h_{fe}\, r_e = 330 \times 26 = 8580\Omega$

On applying KVL to output loop,

$V_{CC} = I_C R_C + V_{CE} + I_E R_E$ ----- (1)

$V_E = I_E R_E$

$R_E = V_E / I_E = 1.2 / 10^{-3} = 1.2K\Omega$

From equation (1), $12 = 10^{-3}(R_C + 1200) + 6 = R_C = 4800\Omega = 4.8K\Omega$

(iii) <u>To calculate R_1 & R_2:</u>

$V_{BB} = V_{CC}\, R_2 / R_1 + R_2$ ------ (2)

$V_B = V_{BE} + V_E = 0.7 + 12 = 1.9V$

From equation (2), $1.9 = 12\, R_2 / R_1 + R_2$

$R_2 / R_1 + R_2 = 0.158$ ---------(3)

$S = 1 + R_B / R_E = R_B = 1.2K\Omega$

$R_B = R_1 \parallel R_2$

$0.15R_1 = 1.2x10^{-3} = 7.5K\Omega$

$R_2 = 0.158\, R_1 + 0.158\, R_2$, $R_2 = 1.425K\Omega$

(iv) <u>To calculate Coupling capacitors</u>:

(i) $X_{Ci} = \{[h_{ie} + (1+h_{fe})\, R_E] \parallel R_B\} / 10 = 0.12K\Omega$

$X_{Ci} = 1 / 2\prod f\, C_i == 1.3\mu f$

(ii) $X_{CO} = R_{Leff} / 10$ $\quad [A_V = - h_{fe}\, R_{Leff} / h_{ie}]$

$R_{Leff} = 0.74K\Omega$, $X_{CO} = 0.075\ K\Omega$

$X_{CO} = 1 / 2\prod f\, C_O$, $C_O = 2.1\mu f$

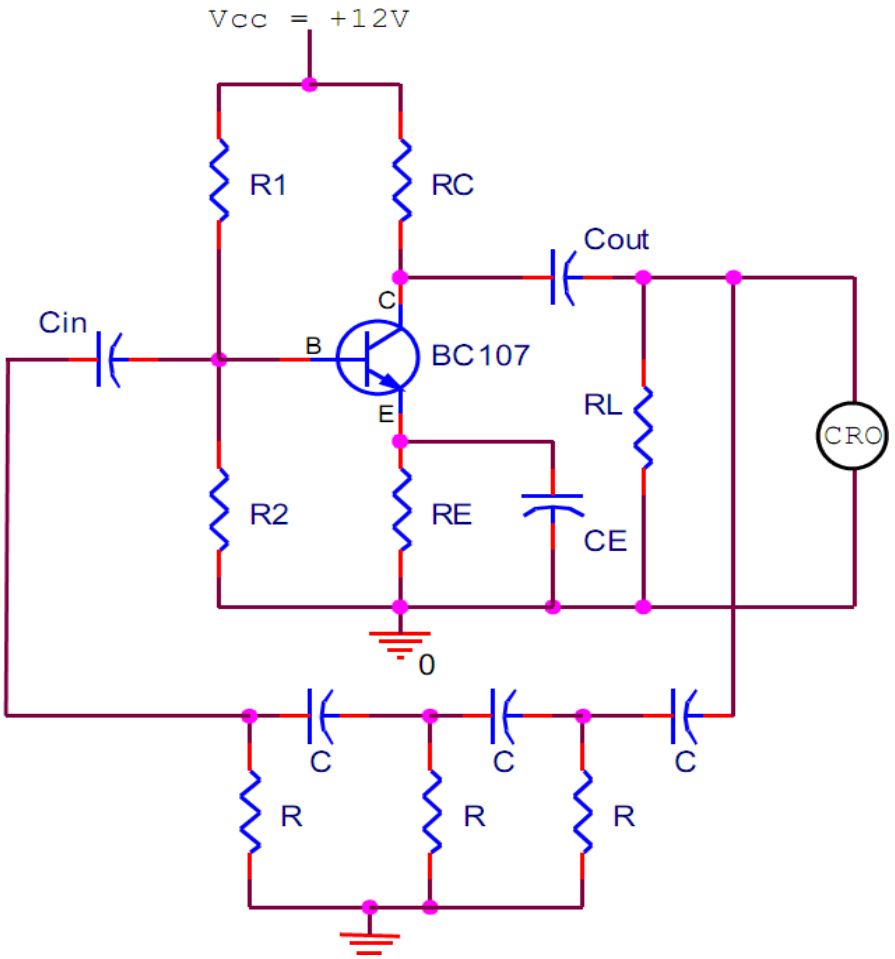
(iii) $X_{CE} = R_E / 10 = 1.326\ \mu f$

$X_{CE} = 1 / 2\prod f\, C_E = 49.27\mu f$

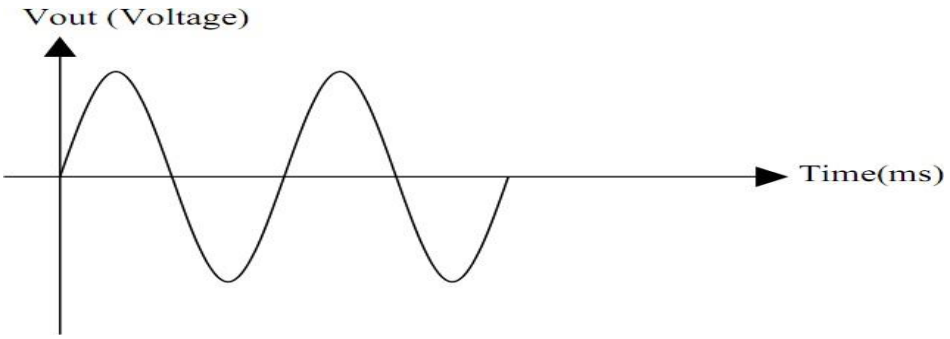
(iv) **Feed back capacitor**, $X_{CF} = R_f / 10$

$C_f = 0.636\mu f = 0.01\mu f$

CIRCUIT DIAGRAM:



MODEL GRAPH:



TABULATION:

S.NO	Amplitude	Time Period (ms)

THEORY:

The low frequencies RC oscillators are more suitable. Tuned circuit is not an essential APPARATUS REQUIRED for oscillation. The essential APPARATUS REQUIRED is that there must be a 180^o phase shift around the feedback network and loop gain should be greater than unity. The 180^o phase shift in feedback signal can be achieved by suitable RC network.

PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Set V_{CC} = 15V.
3. For the given supply the amplitude and time period is measured from CRO.
4. Frequency of oscillation is calculated by the formula f=1/T
5. Amplitude Vs time graph is drawn.

RESULT:

Thus the RC-phase shift oscillator is designed and constructed for the given frequency.

Ex. No.: 2.b Date:	WEIN- BRIDGE OSCILLATOR

AIM:

To design a Wein-bridge oscillator using transistors and to find the frequency of oscillation.

APPARATUS REQUIRED:

S.No	APPARATUS REQUIRED	RANGE	QUANTITY
1	Resistors		
2	Power supply	5V	1
3	Transistor	BC107	1
4	Capacitors		
5	CRO		1
6	Bread board		1

DESIGN EXAMPLE:

Assume f=1 KHz, C=0.1µf

$f = 1/ 2\prod RC$

$R= 1/2\prod fC$

$R =1/2x3.14x1x10^3x0.1x10^3$

$R= 1.59K\Omega$

To calculate R_1:

$R_1= 10R$

$R_1 =10x1.5K$

$R_1 =15.9K\Omega$

To calculate R_f (Feedback resistor):

$R_f = 2R_1$

$R_f = 2(15.9x10^3) =31.8K\Omega \approx 33K\Omega$

THEORY:

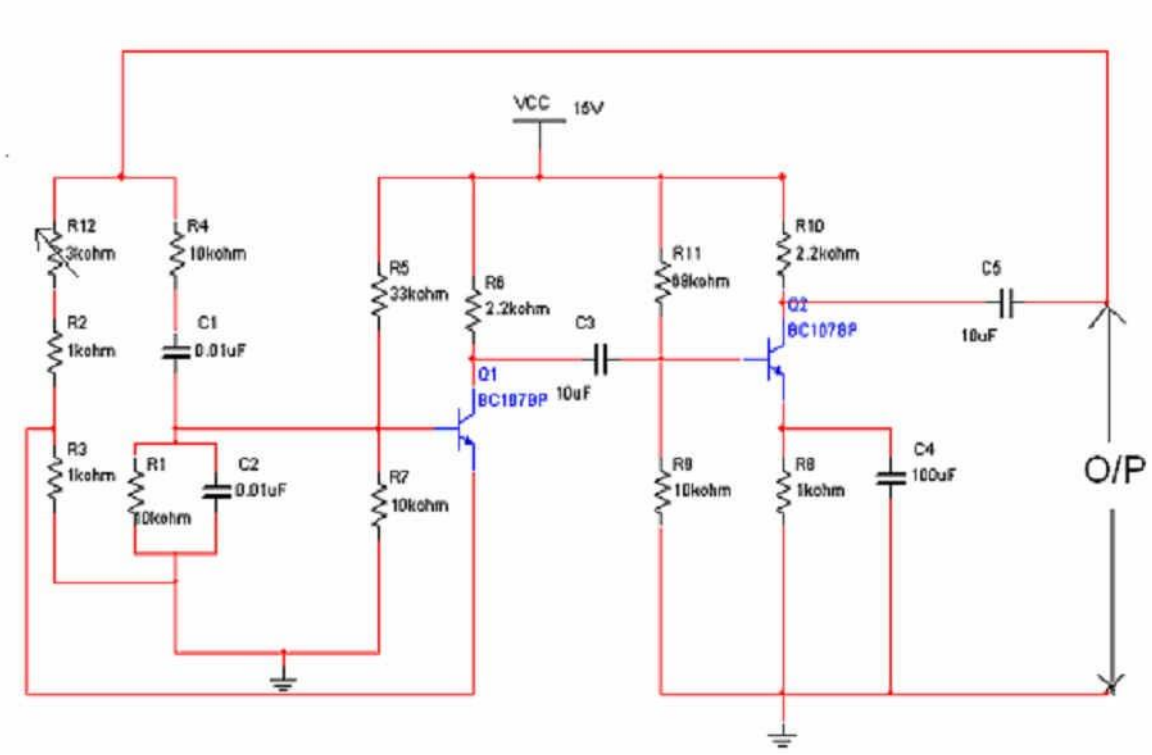
Generally in an oscillator, amplifier stage introduces 180^o phase shift and feedback network introduces additional 180^o phase shift, to obtain a phase shift of 360^o around a loop. This is a condition for any oscillator. But Wein bridge oscillator uses a non-inverting amplifier and hence does not provide any phase shift during amplifier stage. As total phase shift requires is 0^o or $2n\pi$ radians, in Wein bridge type no phase shift is necessary through feedback. Thus the total phase shift around a loop is 0^o. The output of the amplifier is applied between the terminals 1 and 3, which are the input to the feedback network. While the amplifier input is supplied from the diagonal terminals 2 and 4, which is the output from the feedback network. Thus amplifier supplied its own output through the Wein bridge as a feedback network.

The two arms of the bridge, Componentsly R_1, C_1 in series and R_2, C_2 in parallel are called frequency sensitive arms. This is because the components of these two arms decide the frequency of the oscillator. Advantage of Wein bridge oscillator is that by varying the two-capacitor values simultaneously, by mounting them on the common shaft, different frequency ranges can be provided.

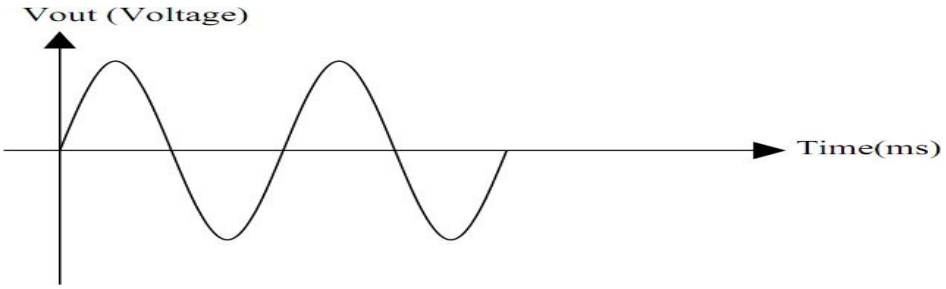
PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Set $V_{CC} = 5V$.
3. For the given supply the amplitude and time period is measured from CRO.
4. Frequency of oscillation is calculated by the formula f=1/T
5. Amplitude Vs time graph is drawn.

CIRCUIT DIAGRAM



MODEL GRAPH:



MODEL TABULATION:

S.NO	Amplitude	Time Period (ms)

RESULT:

Thus the Wein – bridge oscillator is designed for the given frequency of oscillation.

Ex. No.: 3.a Date:	HARTLEY'S OSCILLATOR

AIM:

To design and construct a Hartley oscillator at the given operating frequency.

APPARATUS REQUIRED:

S.No	EQUIPMENTS	RANGE	QUANTITY
1	Resistors		
2	RPS	(0-30)V	1
3	Transistor	BC107	1
4	Capacitors		
5	Inductor	10mH	2
6	CRO	30MHz	1
7	Bread board	-	1

Design Example:

Design of feed back Network:

Given $L_1 = L_2 = 10mH$, f=20 KHz, $V_{CC}=12V$, $I_C=3mA$, S=12

$$f = 1/2\prod\sqrt{(L1+L2)C}$$

C= 3.2nf

Amplifier design:

(i) Selection of R_C:

Gain formula is,

$$A_V = - h_{fe} R_{Leff} / h_{ie}$$

Assume $V_{CE}=V_{CC}/2$ (Transistor active)

$V_{CE}= 12/2= 6V$

$V_E=I_ER_E= V_{CC}/10=1.2V$

$V_{CC}=I_CR_C + V_{CE} + I_ER_E$

$R_C = (V_{CC} - V_{CE} - I_E R_E) / I_C$

Therefore $R_C = 1.6K\Omega = 2\,K\Omega$

(ii) Selection of R_E:

$I_C = I_E = 3mA$

$R_E = V_E / I_E$

$R_E = 1.2 / 3x10^{-3} = 400\ \Omega = 1K\Omega$

(iii) Selection of R_1 & R_2:

Stability factor S=12

$S = 1 + (R_B / R_E)$

$12 = 1 + (R_B / 1x10^3)$

$R_B = 11K$

Using potential divider rule,

$R_B = R_1R_2 / R_1+R_2$ & $V_B = (R2 / R_1+R_2)\ V_{CC}$

$R_B / R_1 = R_2 / R_1+R_2$

Therefore $R_B/R_1 = V_B/V_{CC}$

$V_B = V_{BE} + V_E = 0.7+1.2 = 1.9V = 2V$

$R_1 = (V_{CC} / V_B)R_B$

$R_1 = (12/2)x\ 11x10^3 = 66K\Omega = 100K\Omega$

$V_B/V_{CC} = R_2 / R_1+R_2$

$2 / 12 = R_2 / 100x10^3 + R_2$

$(100x10^3) + R_2 = R_2/0.16 = 19K\Omega$

$R_2 = 19K\Omega = 22\ K\Omega$

(iv)Output capacitance (C_O):

$X_{CO} = R_C/10 = 2x10^3/10 = 200$

$1/2\prod fC_O = 200$

$C_O = 1/2x3.14x20x10^3x200$

C_O=0.039=0.01µf

(v) Input capacitance (C_i):

X_{Cin}= R_B/10=11x10^3/10=1.1x10^3

1/2∏fC_{in}=1.1x10^3

C_{in}=1/2x3.14x20x10^3x1.1x10^3

C_{in}= 0.007=0.01µf

(vi) By pass Capacitance (C_E):

X_{CE}=R_E/10=1x10^3/10=100

1/2∏fC_E=100

C_E= 1/2x3.14x20x10^3x100

C_E =0.079µf = 0.1µf

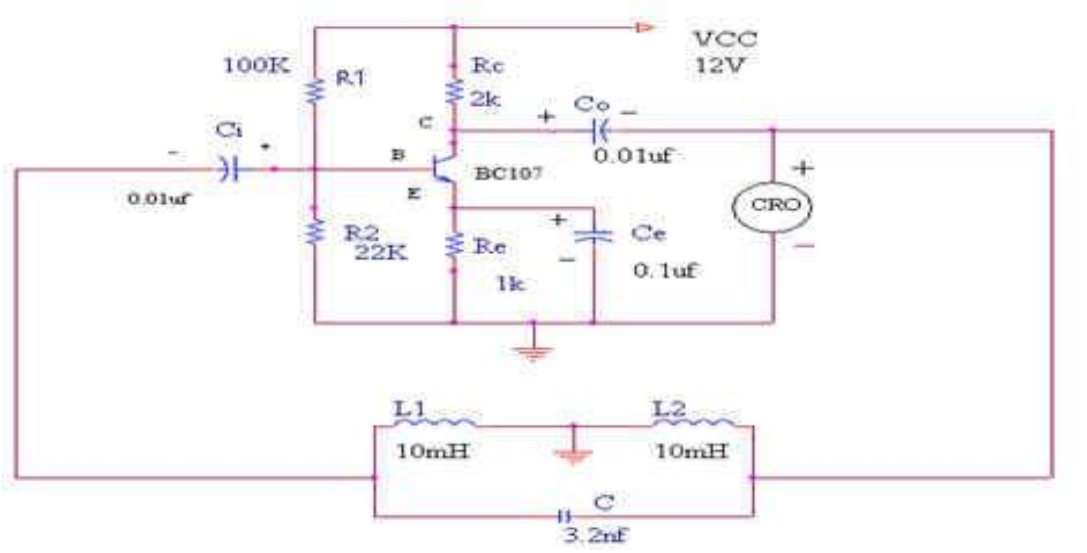
THEORY:

Hartley oscillator is very popular and is commonly used as local oscillator in radio receivers. The collector voltage is applied to the collector through inductor L whose reactance is high compared with X_2 and may therefore be omitted from equivalent circuit, at zero frequency, however capacitor C_b acts as an open circuit.

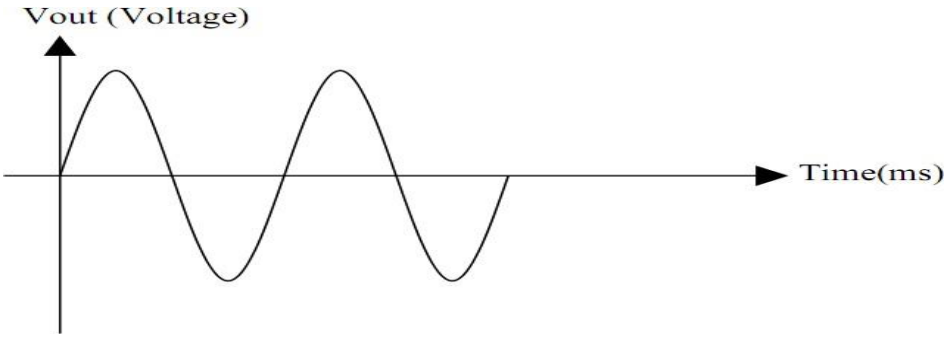
PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Set V_{CC} = 12V.
3. For the given supply the amplitude and time period is measured from CRO.
4. Frequency of oscillation is calculated by the formula f=1/T
5. Verify it with theoretical frequency, f= 1/2∏ ($\sqrt{(L1+L2)C}$) Amplitude Vs time graph is drawn.

CIRCUIT DIAGRAM:



MODEL GRAPH:



MODEL TABULATION:

S.NO	Amplitude	Time Period (ms)

RESULT:

Thus the Hartley oscillator is designed and constructed for the given frequency.

Ex. No.: 3.b. Date:	COLPITT'S OSCILLTOR

AIM:

To design and construct a Colpitt's oscillator at the given operating Frequency.

APPARATUS REQUIRED:

S.No	EQUIPME NTS	RANG E	QUANTI TY
1	Resistors		
2	RPS	(0-30)V	1
3	Transistor	BC107	1
4	Capacitors		
5	Inductor	10mH	1
6	CRO	30MHz	1
7	Bread board	-	1

Design of feedback Network:

Given C_1= 0.1 μF, L=10mH, f=20 KHz, V_{CC}=12V,I_C=3mA, S=12

$$f = 1/2\prod\sqrt{\frac{C1+C2}{LC1C2}}$$, C2= 0.01μF

Amplifier design:

(i)Selection of R_C:

Gain formula is,

$$A_V = - h_{fe} R_{Leff} / h_{ie}$$

Assume $V_{CE}=V_{CC}/2$ (Transistor active)

V_{CE}= 12/2= 6V

$V_E=I_ER_E= V_{CC}/10$=1.2V

$V_{CC}=I_CR_C + V_{CE} + I_ER_E$

$R_C= (V_{CC}- V_{CE} -I_ER_E) / I_C$

Therefore R_C= 1.6KΩ=2 KΩ

(ii) Selection of R_E:

$I_C= I_E$=3mA

$R_E= V_E/I_E$= 1KΩ

(iii) Selection of R_1 & R_2:

Stability factor S=12

$S=1+(R_B/ R_E)$

$12=1+ (R_B/1x10^3)$=11k

Using potential divider rule,

$R_B=R_1R_2$ / R_1+R_2 & V_B= (R2/ R_1+R_2) V_{CC}

R_B /R_1= R_2/ R_1+R_2

Therefore $R_B/R_1= V_B/V_{CC}$

$V_B=V_{BE}+ V_E$= 0.7+1.2=1.9V=2V

R_1= (V_{CC}/ V_B) R_B=66KΩ=100KΩ

V_B/V_{CC} =R_2 / R_1+R_2

2/ 12=R_2 / $100x10^3+R_2$

R_2=19KΩ=22 KΩ

(iv) Output capacitance (C_O):

$X_{CO}=R_C/10=2x10^3/10=200$

$1/2\prod fC_O=200$

$C_O=1/2x3.14x20x10^3x200=0.039=0.01\mu f$

(v) Input capacitance (C_i):

$X_{Cin}= R_B/10=11x10^3/10=1.1x10^3$

$1/2\prod fC_{in}=1.1x10^3$

$C_{in}=1/2x3.14x20x10^3x1.1x10^3=0.0101\mu f$

(vi) By pass Capacitance (C_E):

$X_{CE}=R_E/10=1x10^3/10=100$

$1/2\prod fC_E=100$

C_E= $1/2x3.14x20x10^3x100=0.079\mu f = 0.1\mu f$

THEORY:

Colpitt's oscillator is very popular and is commonly used as local oscillator in radio receivers. The collector voltage is applied to the collector through inductor L whose reactance is high compared with X_2 and may therefore be omitted from equivalent circuit, at zero frequency; The circuit operates as Class C. the tuned circuit determines basically the frequency of oscillation.

PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Set V_{CC} = 12V.
3. For the given supply the amplitude and time period is measured from CRO.
4. Frequency of oscillation is calculated by the formula f=1/T
5. Amplitude Vs time graph is drawn.

CIRCUIT DIAGRAM:

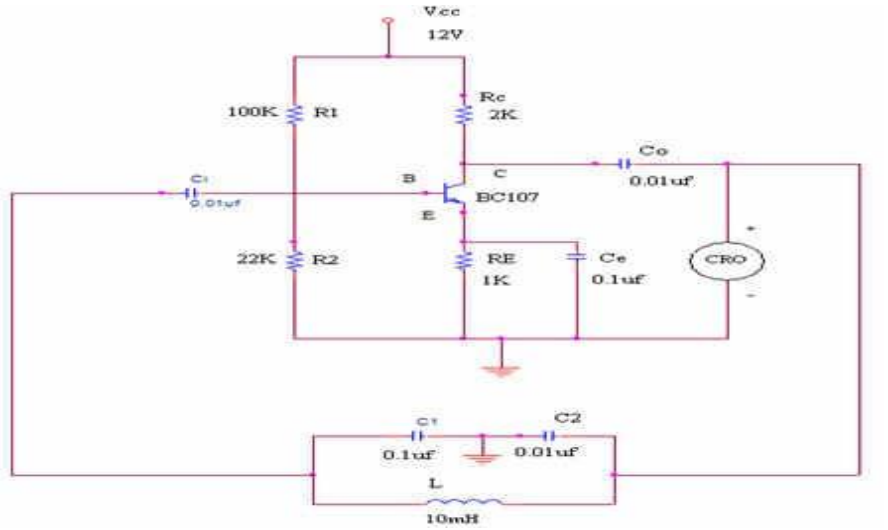
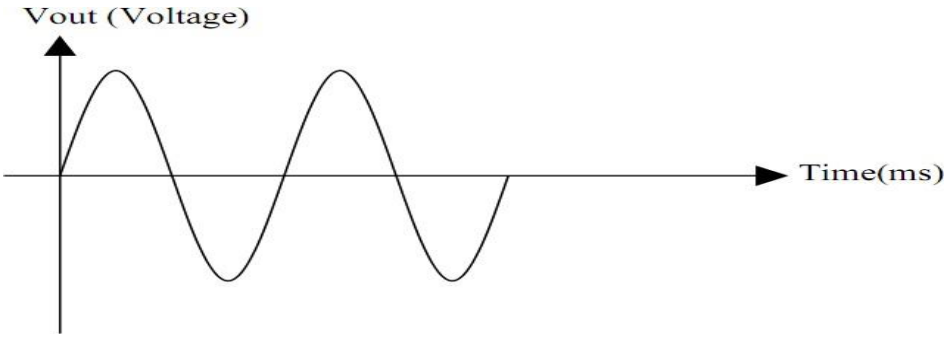


FIG 8.1

MODEL GRAPH:



MODEL TABULATION:

S.NO	Amplitude	Time Period (ms)

RESULT:

Thus the Collipit's oscillator is designed and constructed for the given frequency.

Ex. No.:4 Date:	SINGLE TUNED AMPLIFIER

AIM:

To design a single tuned amplifier and to draw its frequency response.

APPARATUS REQUIRED:

S.No	EQUIPMENTS	RANGE	QUANTITY
1	Resistors		
2	RPS	(0-30)V	1
3	Transistor	BC107	1
4	Capacitors		
5	CRO	(0-30)MHz	1
6	Function generator	(0-10)MHz	1
7	Bread board	-	1

DESIGN EXAMPLE:

Given specifications

Vcc = 12V, β = 100, Ic = 1mA, L=1mH, f=2 KHz, S= [2-10]

Assume, $V_{CE} = V_{CC} / 2 = 6V$

$V_E = V_{CC} / 10 = 1.2V$

To calculate C:

$$F = 1/ 2\prod \sqrt{LC}$$

Therefore C=0 .6μf

To calculate R_E:

$V_E = I_E R_E \quad (I_C = I_E)$

$R_E = V_E / I_E = 1.2 / 1x10^{-3} = 1.2K\Omega$

Assume S= 10, $S = 1 + (R_B / R_E)$

Therefore $R_B = 10K\Omega$

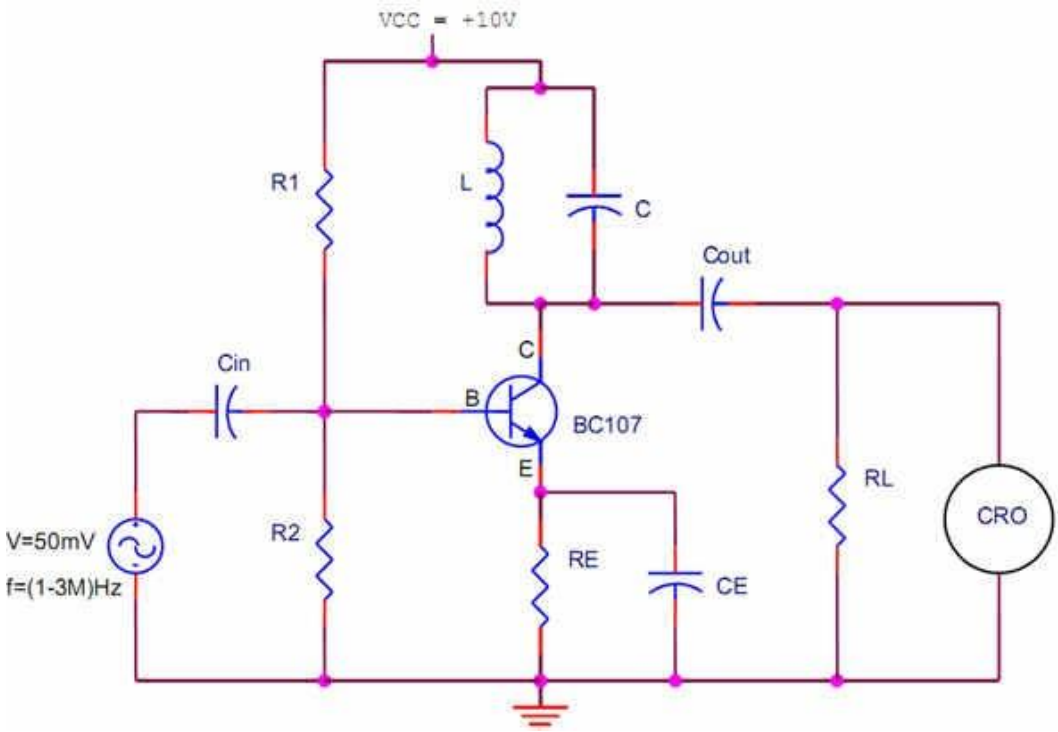
To find R_1 & R_2:

$R_B = R_1 \parallel R_2$

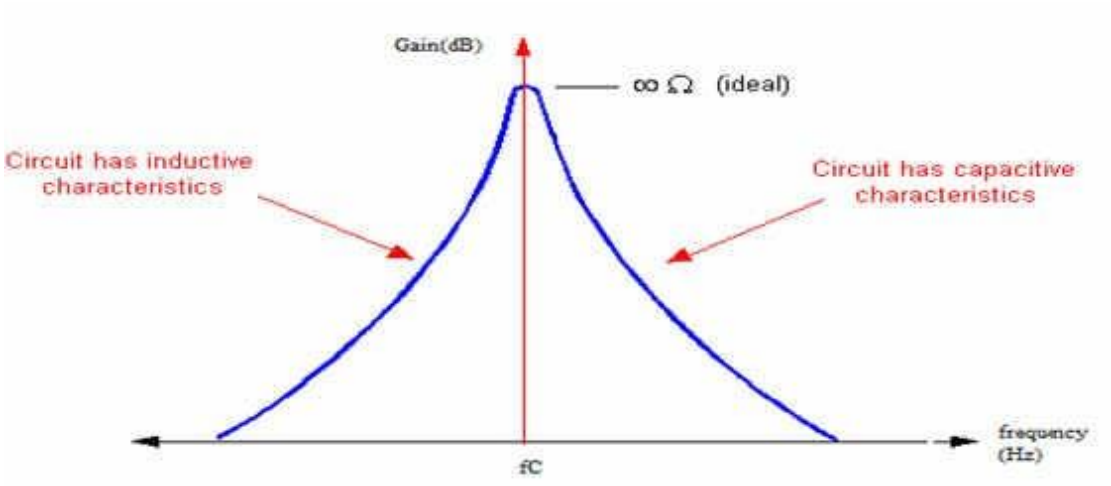
$R_B = R_1 R_2 / R1 + R_2$ ---------- (1)

$V_B = V_{CC} \times (R_2 / R_1 + R_2)$ -------- (2)

CIRCUIT DIAGRAM:



MODEL GRAPH:



TABULATION:

FREQUENCY	V_{in} (V)	OUTPUT V_O(V)	Gain = 20log(V_o/V_{in}) dB

THEORY:

The single tuned amplifier selecting the range of frequency the resistance load replaced by the tank circuit. Tank circuit is nothing but inductors and capacitor in parallel with each other. The tuned amplifier gives the response only at particular frequency at which the output is almost zero. The resistor R_1 and R_2 provide potential diving biasing, R_e and C_e provide the thermal stabilization. This it fixes up the operating point.

PROCEDURE:

1. Connections are given as per the circuit diagram
2. By varying frequency, amplitude is noted down
3. Gain is calculated in dB
4. Frequency response curve is drawn.

RESULT:

Thus the class – c single tuned amplifier is designed and frequency response is plotted.

Ex. No.: 5 Date:	INTEGRATOR AND DIFFERENTIATOR

AIM:

To design and construct a differentiator and integrator circuit.

APPARATUS REQUIRED:

S.No	Components	Range	Quantity
1.	Function generator	(0-30)MHz	1
	CRO	(0-20)V	1
	Regulated Power Supply	(0-30)V	1
2.	Resistor	1 kΩ	1
	Capacitor	1 uf	1
3.	Bread board	-	1
	Connecting Wires	Single strand	As required

THEORY:

Differentiator:

Differentiator is a circuit which differentiates the input signal, it allows high order frequency and blocks low order frequency. If time constant is very low it acts as a differentiator. In this circuit input is continuous pulse with high and low value.

Integrator:

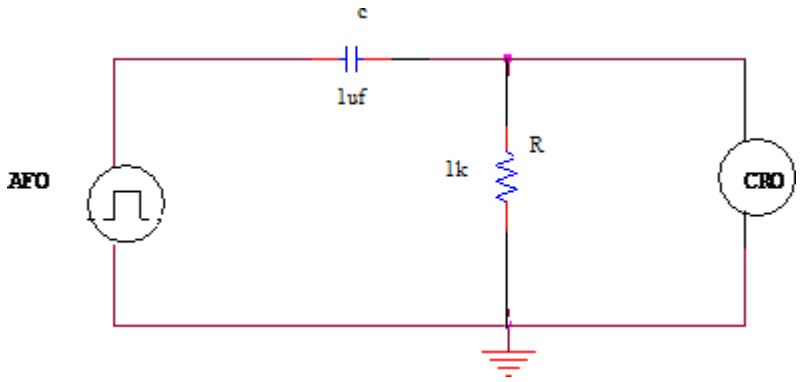
In a low pass filter when the time constant is very large it acts as a integrator. In this the voltage drop across C will be very small in comparison with the drop across resistor R. So total input appears across the R.

PROCEDURE:

1. Connections are given as per the circuit diagram.
2. Set the signal voltage.
3. Observe the output waveform.
4. Sketch the output waveform.

INTEGRATOR:

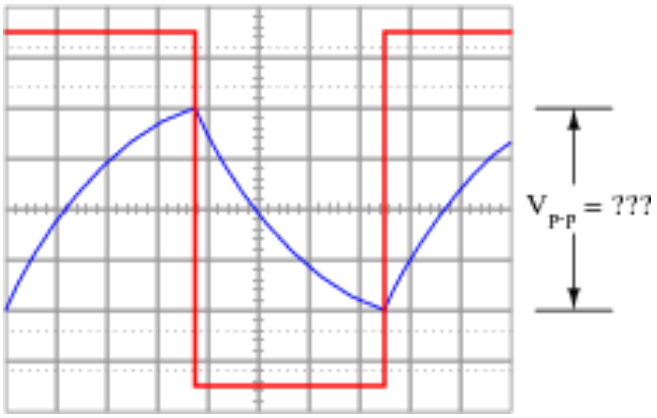
CIRCUIT DIAGRAM:



MODEL TABULATION:

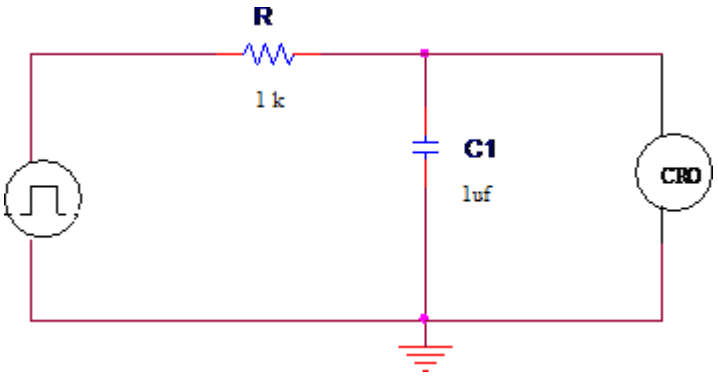
S.NO	Amplitude(V)	Time(ms)

MODEL GRAPH:



DIFFERENTIATOR

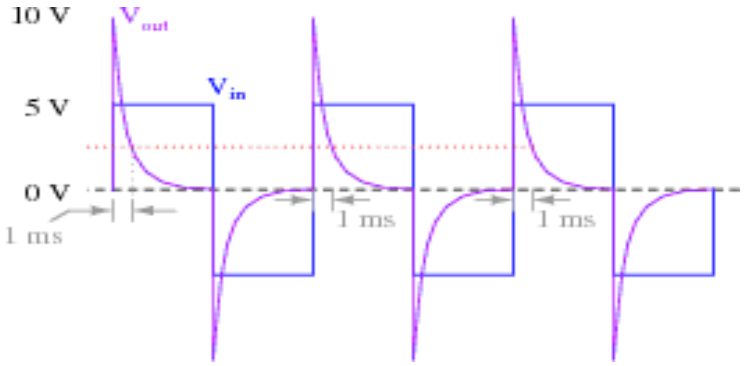
CIRCUIT DIAGRAM:



MODEL TABULATION:

S.NO	Amplitude(V)	Time(ms)

MODEL GRAPH:



RESULT:

Thus the integrator and differentiator are constructed and output waveform observed and readings were tabulated

Ex. No.: 6.a Date:	EMITTER COUPLED ASTABLE MULTIVIBRATOR

AIM:

To design an Emitter coupled Astable multivibrator and study the output waveform.

APPARATUS REQUIRED:

S.No	EQUIPMENTS	RANGE	QUANTITY
1	Resistors		
2	RPS	(0-30)V	1
3	Transistor	BC107	2
4	Capacitors		
5	CRO	(0-30)MHz	1
6	Bread board	-	1

DESIGN EXAMPLE:

Given specifications:

V_{CC}= 10V; hfe = 100; f=1 KHz; I *c* = 2mA; Vce (sat) = 0.2v;

To design R_C:

$R \leq h_{FE} R_C$

$R_C = V_{CC} - V_{C2\ (Sat)} / I_C = 4.9\ k\Omega$

Since $R \leq h_{FE} R_C$

Therefore $R \leq 100 \times 4.7 \times 10^3 = 490\ k\Omega \approx 470\ k\Omega$

To Design C:

Since $T = 1.38RC$

$1 \times 10^{-3} = 1.38 \times 490 \times 10^3 \times C$

Therefore $C = 0.01\mu F$

THEORY:

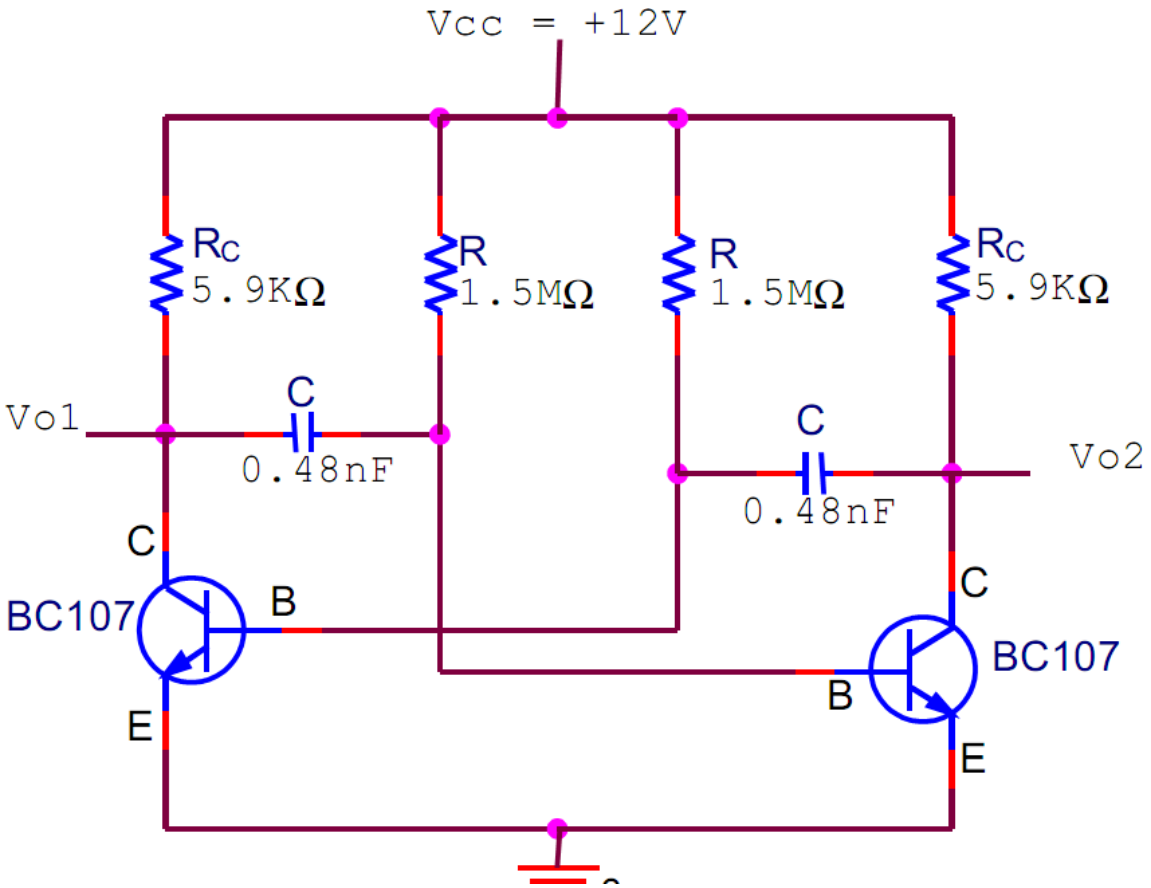
The astable multivibrator generates square wave without any external triggering pulse. It has no stable state, i.e., it has two quasi- Stable states. It switches

back and forth from one stable state to other, remaining in each state for a time depending upon the discharging of a capacitive circuit. When supply voltage + Vcc is applied, one transistor will Conduct more than the other due to some circuit imbalance.

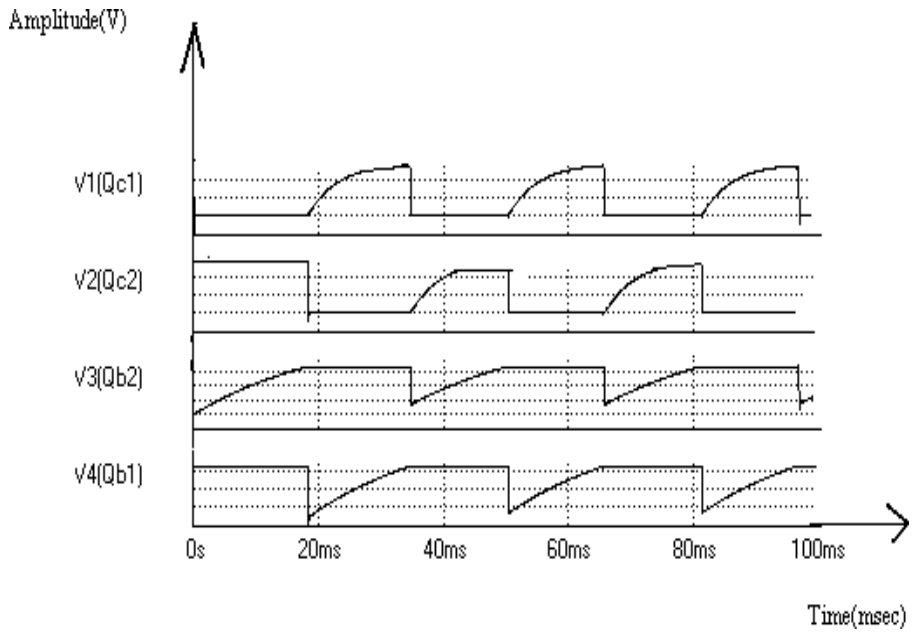
PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Set V_{CC} = 5V.
3. For the given supply the amplitude and time period is measured from CRO.
4. Frequency of oscillation is calculated by the formula f=1/T
5. Amplitude Vs time graph is drawn.

CIRCUIT DIAGRAM



MODEL GRAPH:



TABULATION:

S.NO	Amplitude(V)	Time period(msec)

RESULT:

Thus the astable multivibrator is designed and output waveform is plotted

Ex. No.: 6.b Date:	MONOSTABLE MULTIVIBRATOR

AIM:

To design and test the performance of Monostable multivibrator for the given frequency

APPARATUS REQUIRED:

S.No	EQUIPMENTS	RANGE	QUANTITY
1	Resistors		
2	RPS	(0-30)V	1
3	Transistor	BC107	1
4	CRO	(0-30)MHz	1
5	Capacitor	3.2nf 25pf	1 1
6	Bread board	-	1

DESIGN EXAMPLE:

Given specifications:

V_{CC}= 12V; hfe = 200; f=1 KHz; I *c* = 2mA; Vce (sat) = 0.2v; V_{BB}= - 2V,

(i) **To calculate R_C**:

$R_C = V_{CC}$ - Vce (sat) / I_C

R_C = 12 – 0.2 / $2x10^{-3}$=5.9KΩ

(ii) To calculate R:

$I_{B2(min)}=I_{C2} / h_{fe}= 2x10^{-3} / 200 = 10\mu$ A

Select $I_{B2} > I_{B1(min)}$ (say 25μ A)

Then $R = V_{CC} – V_{BE}$ (sat) / I_{B2}

Therefore R= $12-0.7/25x10^{-6}$=452KΩ

(iii) To calculate C:

T=0.69RC

$1x10^{-3}= 0.69x452x10^{3}$xC

C=3.2nf

To calculate R1 & R2:

V_{B1}= {(V_{BB} R1/ R1 +R2) + ($V_{CE\ (sat)}$ R2 / R1+R2)}

Since Q1 is in off state, $V_{B1} \leq 0$

Then (V_{BB} R1/ R1 +R2) = ($V_{CE\ (sat)}$ R2 / R1+R2)

V_{BB} R1 = $V_{CE\ (sat)}$ R2

2 R1 = 0.2 R2

Assume R1=10KΩ, then R2=100 KΩ

Consider, C_1= 25pf (commutative capacitor)

THEORY:

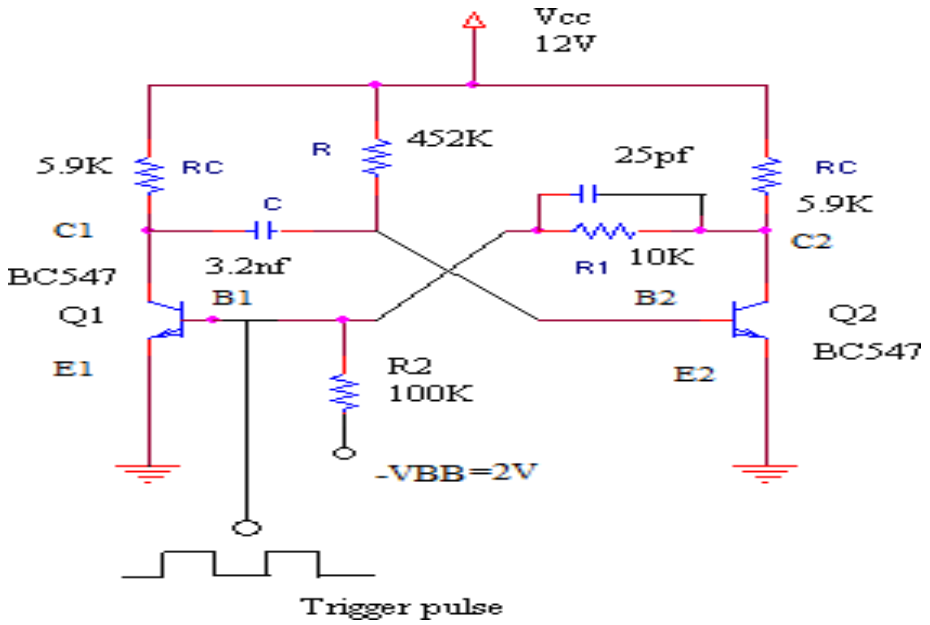
The monostable multivibrator has one stable state when an external trigger input is applied the circuit changes its state from stable quasi stable state. And then automatically after some time interval the circuit returns back to the original normal stable state. The time T is dependent on circuit components.

The capacitor C_1 is a speed-up capacitor coupled to base of Q2 through C. Thus DC coupling in bistable multivibrator is replaced by a capacitor coupling. The resistor R at input of Q2 is returned to $V_{CC.}$ The value of R2, V_{BB} are chosen such that transistor Q1 is off by reverse biasing it. Q2 is on. This is possible by forward biasing Q2 with the help of VCC and resistance R. Thus Q2-ON and Q1-OFF is normal stable state of circuit.

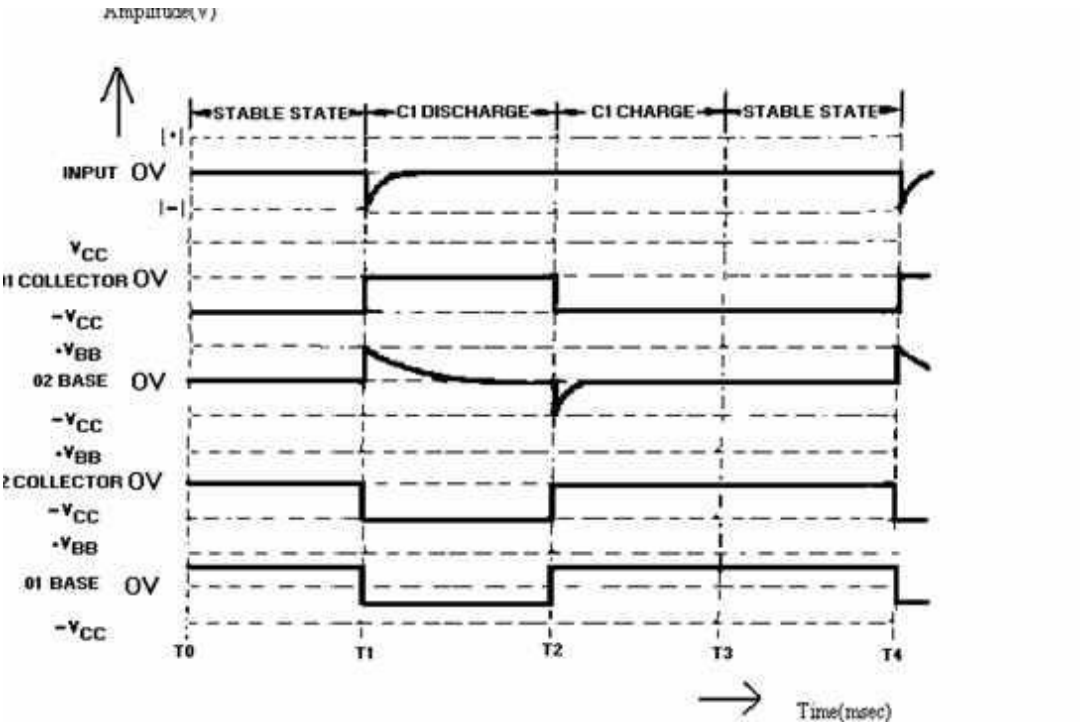
PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Give a negative trigger input to Q2.
3. Note the output of transistor Q2 and Q1.
4. Find the value of T_{on} and T_{off}.

CIRCUIT DIAGRAM:



MODEL GRAPH:



TABULATION:

S.NO	Amplitude(V)	Time period (msec)

RESULT:

Thus the monostable multivibrator is designed and the performance is tested.

Ex. No.: 7 Date:	CLIPPER AND CLAMPER CIRCUITS

AIM:

To construct and design the clipper and clamper circuits using diodes.

APPARATUS REQUIRED:

S.No	Components	Range	Quantity
1.	Function generator	(0-30)MHz	1
	CRO	(0-20)V	1
	Regulated Power Supply	(0-30)V	1
2.	Diode	IN4007	1
	Resistor	1kΩ	1
	Capacitor	1uf	2
3.	Bread board	-	1
	Connecting Wires	Single strand	As required

DESIGN PROCEDURE:

Given f=1 kHz,

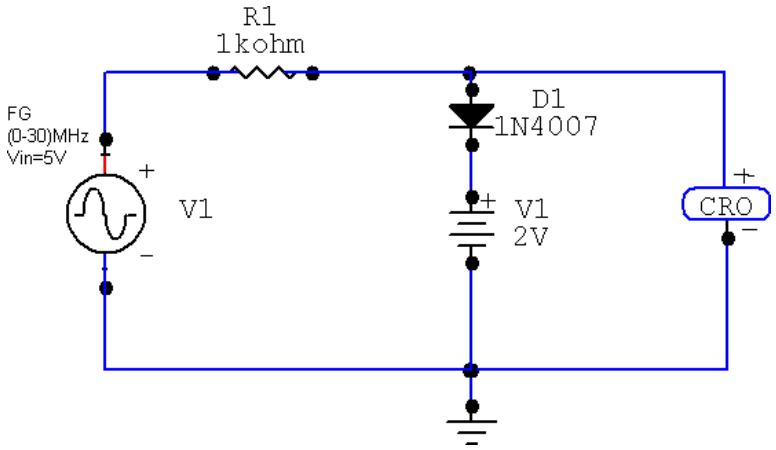
$T=t=1/f=1x10^{-3}$ sec=RC

Assume, C=1uF

Then, R=1KΩ

POSITIVE CLIPPER

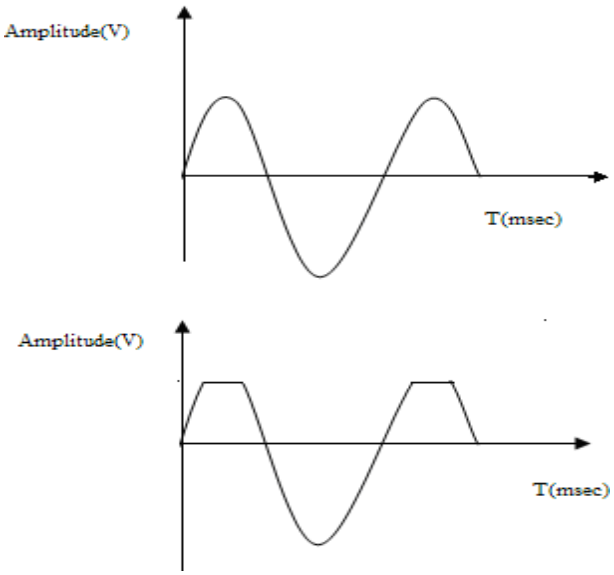
CIRCUIT DIAGRAM:



MODEL TABULATION:

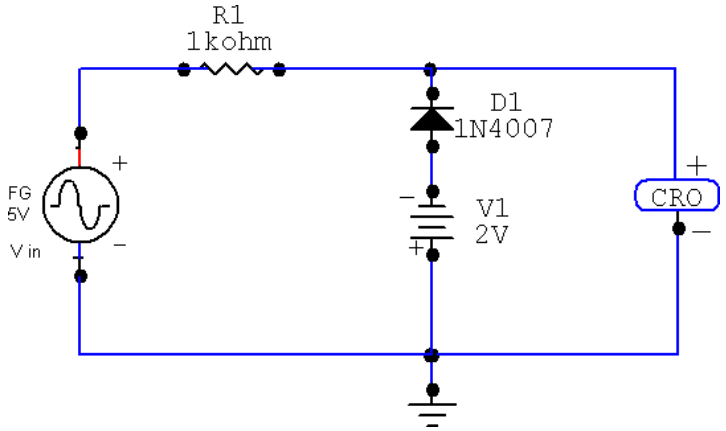
S.NO	SIGNAL	AMPLITUDE	Time (ms)
1	Input		
2	Output		

MODEL GRAPH:



NEGATIVE CLIPPER:

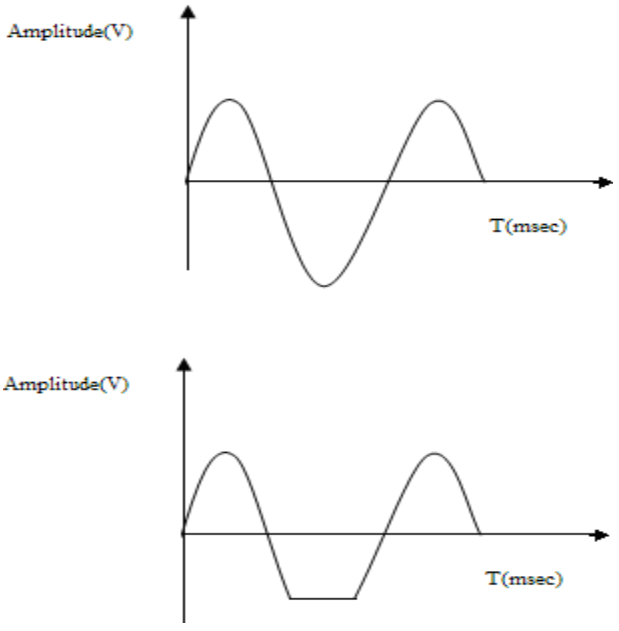
CIRCUIT DIAGRAM:



MODEL TABULATION:

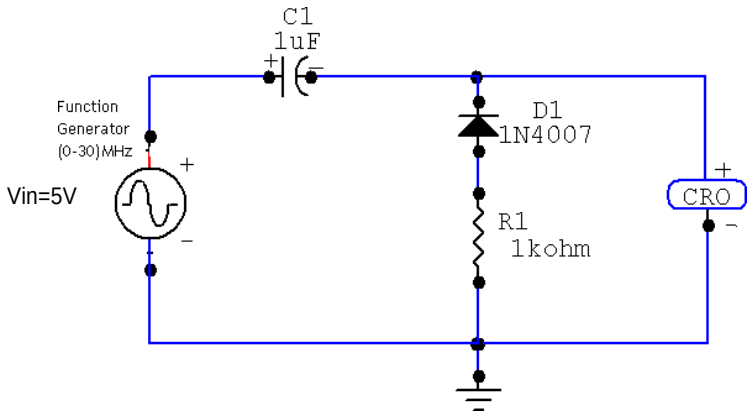
S.NO	SIGNAL	AMPLITUDE	Time (ms)
1	Input		
2	Output		

MODEL GRAPH:



CLAMPER CIRCUIT:

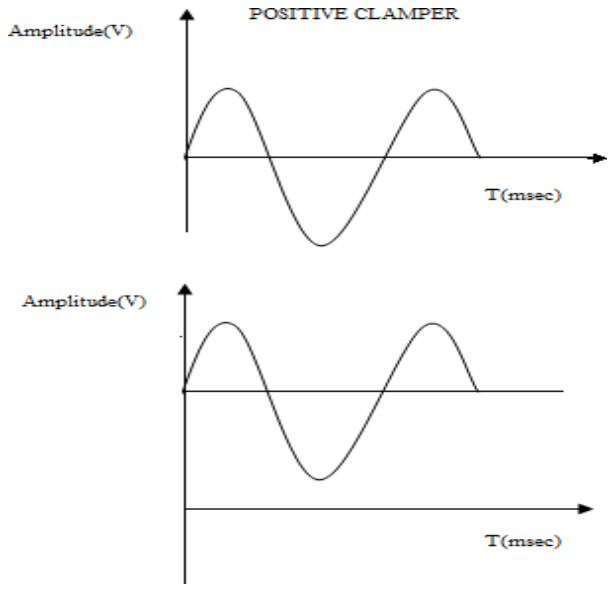
POSITIVE CLAMPER CIRCUIT DIAGRAM:



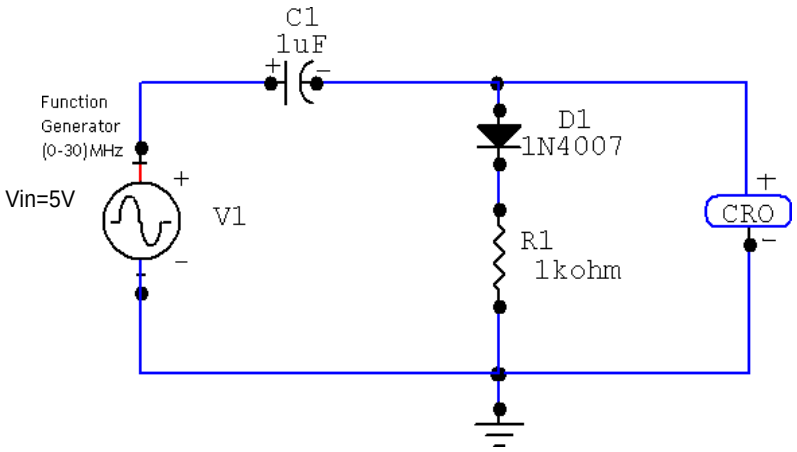
MODEL TABULATION:

S.NO	SIGNAL	AMPLITUDE	Time (ms)
1	Input		
2	Output		

MODEL GRAPH:



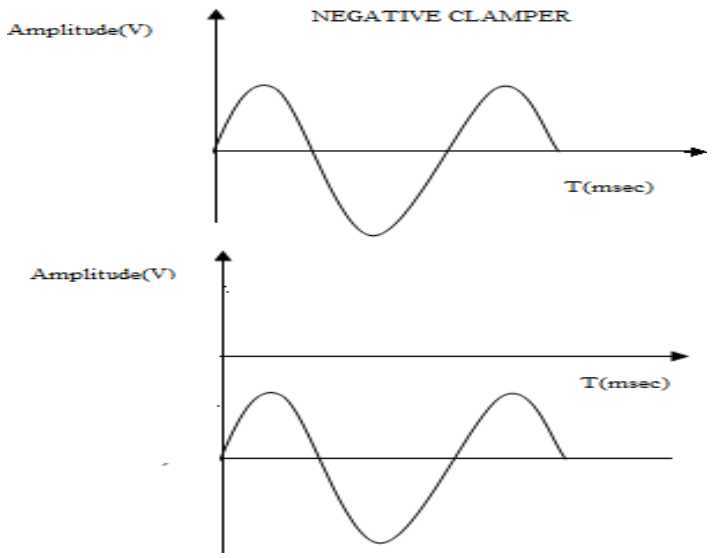
NEGATIVE CLAMPER CIRCUI DIAGRAM:



MODEL TABULATION:

S.NO	SIGNAL	AMPLITUDE	Time (ms)
1	Input		
2	Output		

MODEL GRAPH:



THEORY

CLIPPER:

A Clipper is a circuit that removes either the positive or negative part of a waveform. For a positive clipper only the negative half cycle will appear as output.

CLAMPER:

A Clamper circuit is a circuit that adds a dc voltage to the signal. A positive clamper shifts the ac reference level upto a dc level.

WORKING:

During the positive half cycle, the diode turns on and looks like a short circuit across the output terminals. Ideally, the output voltage is zero. But practically, the diode voltage is 0.7 V while conducting.

On the negative half cycle, the diode is open and hence the negative half cycle appear across the output.

APPLICATION:

- Used for wave shaping
- To protect sensitive circuits

PROCEDURE:

1. Connect as per the circuit diagram.
2. Set the signal voltage (say 5V, 1 KHz) using signal generator.
3. Observe the output waveform using CRO.
4. Sketch the output waveform.

RESULT:

Thus the output waveform for Clipper and clamper was observed and its readings are tabulated.

SIMULATION USING PSPICE

Ex. No.: 9 Date:	TUNED COLLECTOR OSCILLATOR

AIM:

To simulate a tuned collector oscillator using PSPICE**.**

APPARATUS REQUIRED:

1. PC
2. PSPICE software

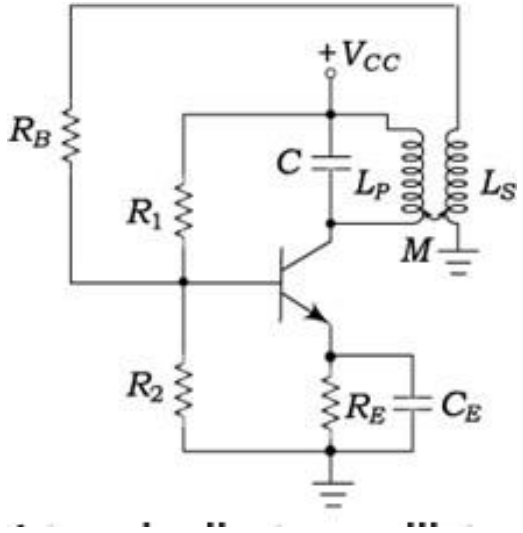
THEORY:

Tuned collector oscillation is a type of transistor LC oscillator where the tuned circuit (tank) consists of a transformer and a capacitor is connected in the collector circuit of the transistor. Tuned collector oscillator is of course the simplest and the basic type of LC oscillators. The tuned circuit connected at the collector circuit behaves like a purely resistive load at resonance and determines the oscillator frequency. The common applications of tuned collector oscillator are RF oscillator circuits, mixers, frequency demodulators, signal generators etc.,

PROCEDURE:

1. Click on the start menu and select the pspice simulation software
2. Select the parts required for the circuit from the parts menu and them in the work space.
3. Connect the parts using wires
4. Save the file and select the appropriate analysis
5. Simulate the circuit and observe the corresponding output waveforms.

CIRCUIT DIAGRAM:



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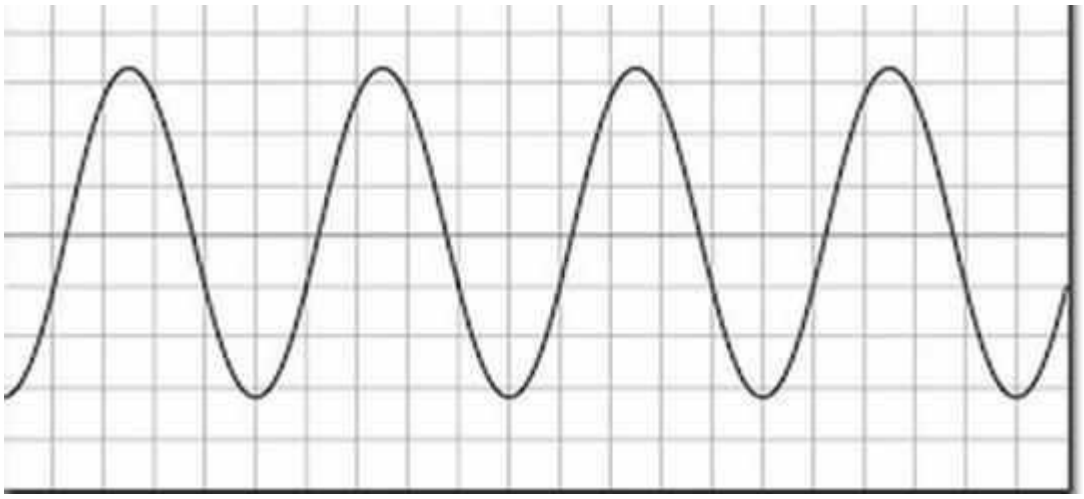
MODEL GRAPH:



RESULT:

Thus the tuned collector oscillator is simulated using PSpice.

Ex. No.: 10 Date:	WEIN BRIGE OSCILLATOR

AIM:

To simulate voltage and current time base circuits by using PSPICE.

APPARATUS REQUIRED:

1. PC
2. PSPICE software

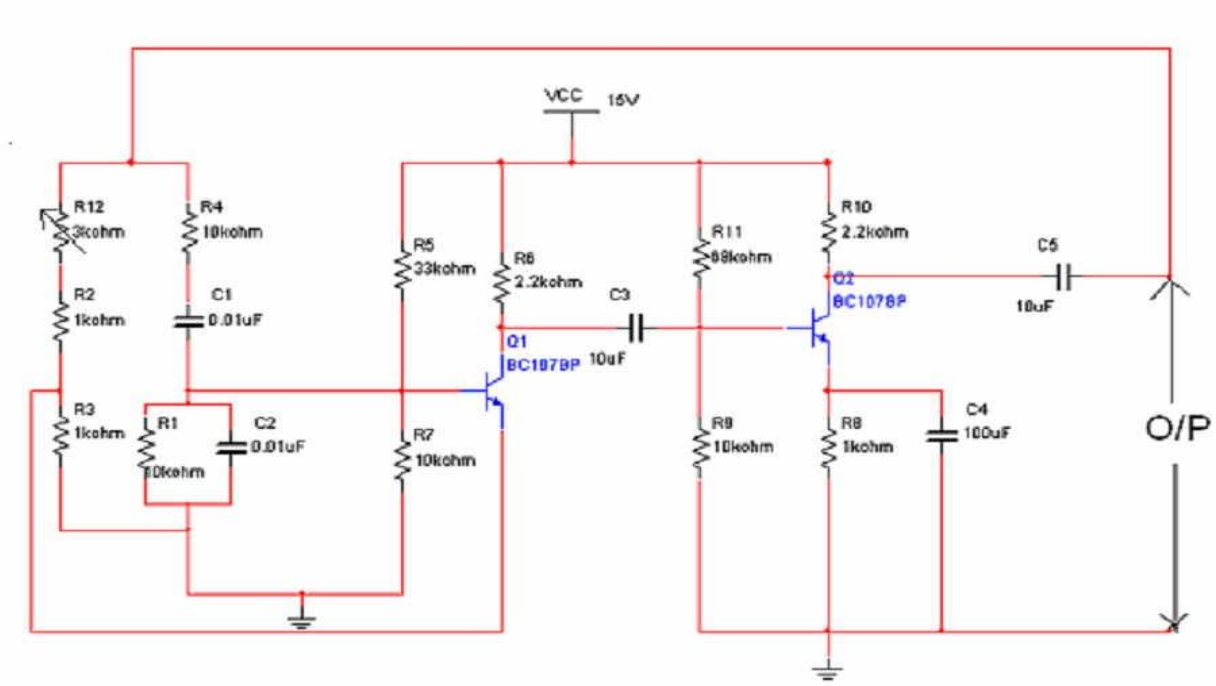
THEORY:

Generally in an oscillator, amplifier stage introduces 180^o phase shift and feedback network introduces additional 180^o phase shift, to obtain a phase shift of 360^o around a loop. This is a condition for any oscillator. But Wein bridge oscillator uses a non-inverting amplifier and hence does not provide any phase shift during amplifier stage. As total phase shift requires is 0^o or $2n\pi$ radians, in Wein bridge type no phase shift is necessary through feedback. Thus the total phase shift around a loop is 0^o. The output of the amplifier is applied between the terminals 1 and 3, which are the input to the feedback network. While the amplifier input is supplied from the diagonal terminals 2 and 4, which is the output from the feedback network. Thus amplifier supplied its own output through the Wein bridge as a feed back network.

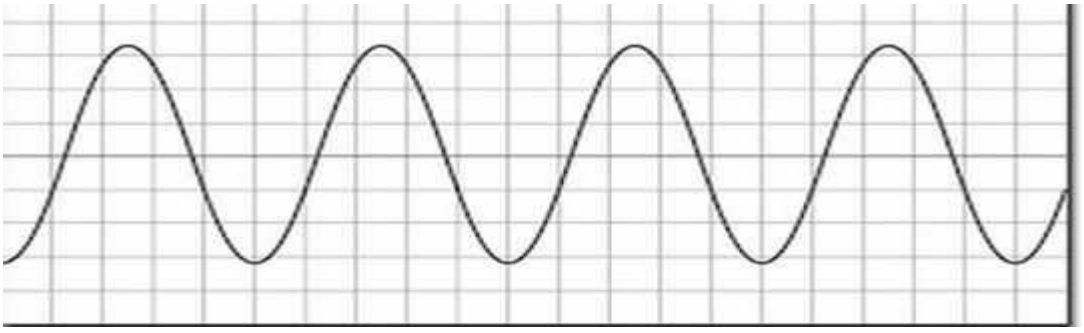
PROCEDURE:

1. Click on the start menu and select the pspice simulation software
2. Select the parts required for the circuit from the parts menu and place them in the work space
3. Connect the parts using wires
4. Save the file and select the appropriate analysis
5. Simulate the circuit and observe the corresponding output waveforms

7.5 CIRCUIT DIAGRAM:



MODEL GRAPH:



RESULT:

Thus the Wein Bridge Oscillator is simulated using Pspice.

Ex. No.: 11 Date:	DOUBLE AND STAGGERED TUNED AMPLIFIER

AIM:

To simulate double and staggered tuned amplifiers.

APPARATUS REQUIRED:

1. PC
2. PSPICE software

THEORY:

A double-tuned amplifier is a tuned amplifier with transformer coupling between the amplifier stages in which the inductances of both the primary and secondary windings are tuned separately with a capacitor across each. The scheme results in a wider bandwidth than a single tuned circuit would achieve. There is a critical value of transformer coupling coefficient at which the frequency response of the amplifier is maximally flat in the pass band and the gain is maximum at the resonant frequency. Designs frequently use a coupling greater than this (over-coupling) in order to achieve an even wider bandwidth at the expense of a small loss of gain in the centre of the pass band. Staggered tuning is a technique used in the design of multi-stage tuned amplifiers whereby each stage is tuned to a slightly different frequency. In comparison to synchronous tuning (where each stage is tuned identically) it produces a wider bandwidth at the expense of reduced gain.

It also produces a sharper transition from the passband to the stopband. Both staggered tuning and synchronous tuning circuits are easier to tune and manufacture than many other filter types. The function of stagger-tuned circuits can be expressed as a rational function and hence they can be designed to any of the major filter responses such as Butterworth and Chebyshev. The poles of the circuit are easy to

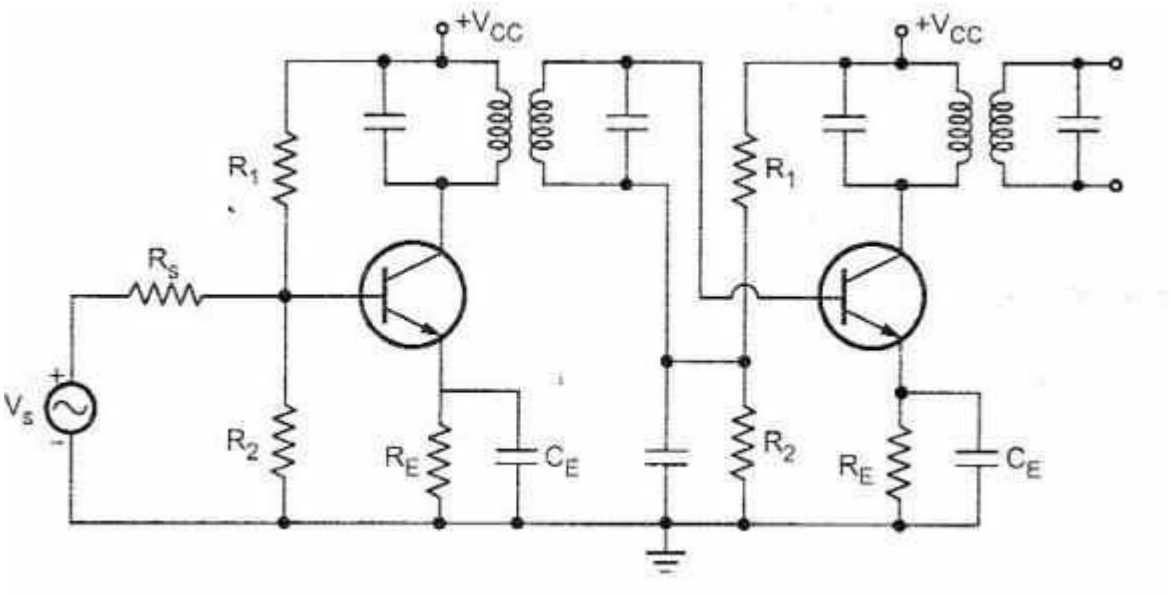
manipulate to achieve the desired response because of the amplifier buffering between stages.

PROCEDURE:

1. Click on the start menu and select the pspice simulation software
2. Select the parts required for the circuit from the parts menu and place them in the work space
3. Connect the parts using wires
4. Save the file and select the appropriate analysis
5. Simulate the circuit and observe the corresponding output waveforms

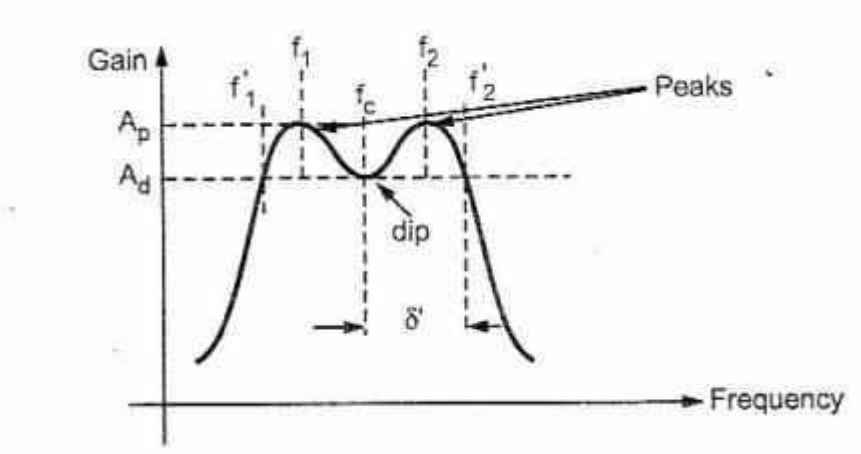
CIRCUIT DIAGRAM:

DOUBLE TUNNED AMPLIFIER



MODEL GRAPH:

DOUBLE TUNNED AMPLIFIER



RESULT:

Thus the double and staggered tuned amplifier is simulated.

Ex. No.: 12 Date:	BI-STABLE MULTIVIBRATOR

AIM:

To simulate an Bi-stable multivibrator using PSPICE.

APPARATUS REQUIRED:

1. PC
2. PSPICE software

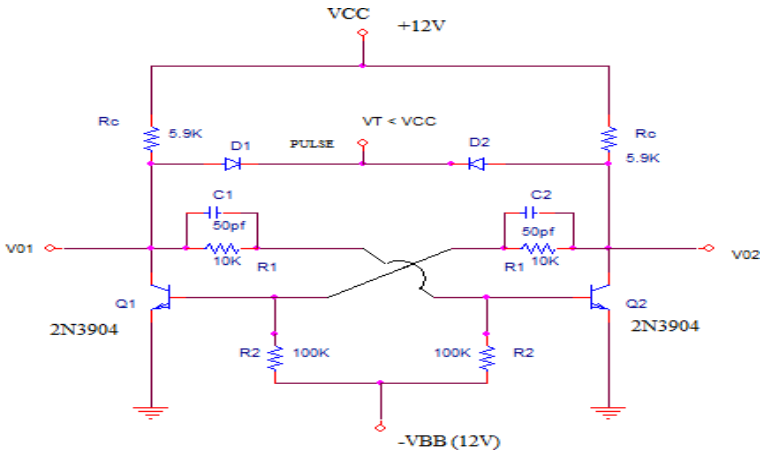
THEORY:

Bi- stable multivibrator contains two stable states and no quasi states. It requires two clock or trigger pulses to change the states. It is also called as flip flop, scale of two toggle circuit, trigger circuit. It is used in digital operations like counting, storing data's in flip flops and production of square waveforms.

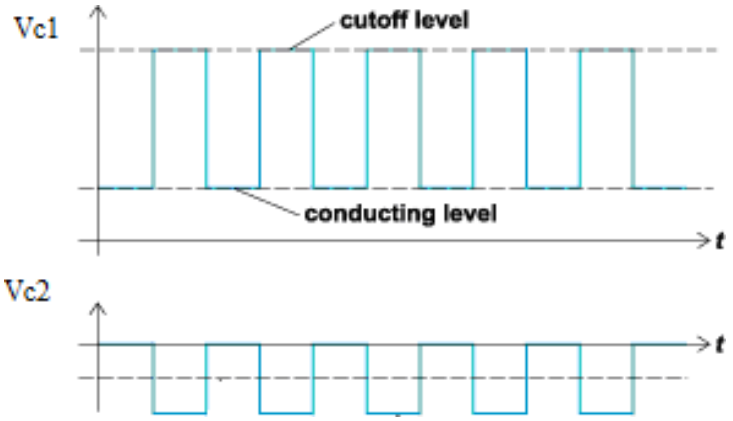
PROCEDURE:

1. Click on the start menu and select the pspice simulation software
2. Select the parts required for the circuit from the parts menu and place them in the work space
3. Connect the parts using wires
4. Save the file and select the appropriate analysis
5. Simulate the circuit and observe the corresponding output waveforms

CIRCUIT DIAGRAM:



MODEL GRAPH:



RESULT:

Thus the Bi-stable multivibrator is simulated using PSpice.

Ex. No.: 13 Date:	SCHMITT TRIGGER CIRCUIT WITH PREDICTABLE HYSTERESIS

AIM:

To simulate Schmitt Trigger circuit with Predictable hysteresis.

APPARATUS REQUIRED:

1. PC
2. PSPICE software

THEORY:

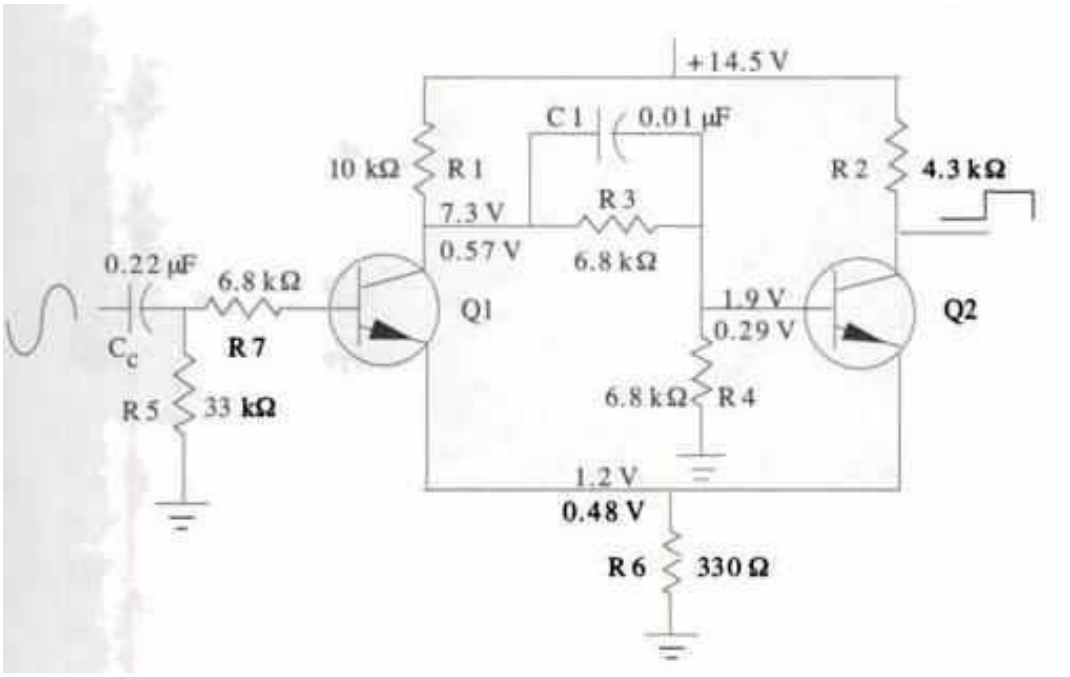
A **Schmitt trigger** is a comparator circuit with hysteresis, implemented by applying positive feedback to the input of an amplifier. It is an active circuit which converts an analog input signal to a digital output signal. The circuit is Componentsd a "trigger" because the output retains its value until the input changes sufficiently to trigger a change. In the non-inverting configuration, when the input is higher than a certain chosen threshold, the output is high. When the input is below a different (lower) chosen threshold, the output is low, and when the input is between the two levels, the output retains its value. This dual threshold action is called *hysteresis* and implies that the Schmitt trigger possesses memory and can act as a bistable circuit (latch or flip-flop). There is a close relation between the two kinds of circuits: a Schmitt trigger can be converted into a latch and a latch can be converted into a Schmitt trigger.

Schmitt trigger devices are typically used in signal conditioning applications to remove noise from signals used in digital circuits, particularly mechanical switch bounce. They are also used in closed loop negative feedback configurations to implement relaxation oscillators, used in function generators and switching power supplies.

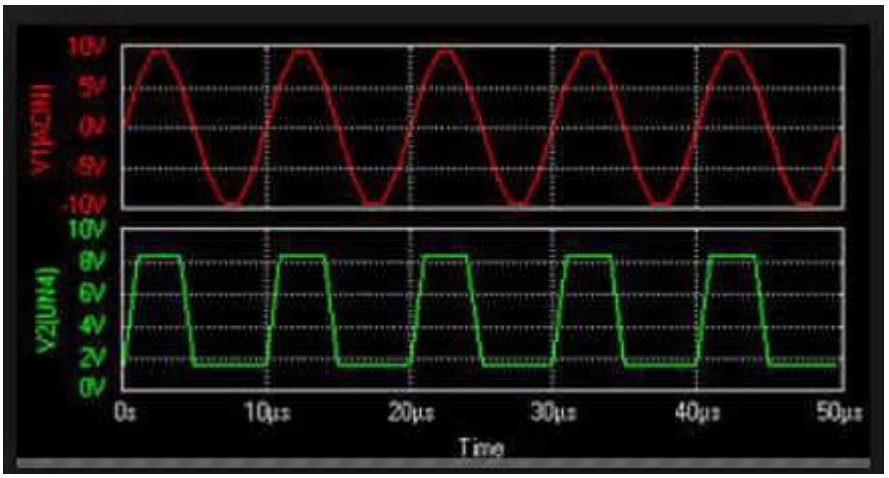
PROCEDURE:

1. Click on the start menu and select the pspice simulation software
2. Select the parts required for the circuit from the parts menu and place them in the work space
3. Connect the parts using wires
4. Save the file and select the appropriate analysis
5. Simulate the circuit and observe the corresponding output waveforms

CIRCUIT DIAGRAM:



MODEL GRAPH:



RESULT:

Thus the Schmitt trigger is simulated using PSpice.

Ex. No.: 14 Date:	ANALYSIS OF POWER AMPLIFIER

AIM:

To design and test the performance of power amplifier.

APPARATUS REQUIRED:

S.No	QUIPMENTS	RANGE	QUANTITY
1	Resistors		
2	RPS	(0-30)V	1
3	Transistor	BC107	1
4	CRO	(0-30)MHz	1
5	Capacitor	3.2nf 25pf	1 1
6	Bread board	-	1

DESIGN EXAMPLE:

Given specifications:

V_{CC}= 12V; hfe = 200; f=1 KHz; I *c* = 2mA; Vce (sat) = 0.2v; V_{BB}= - 2V,

(i) **To calculate R_C**:

$R_C = V_{CC}$ - Vce (sat) / I_C

R_C = 12 – 0.2 / $2x10^{-3}$=5.9KΩ

(ii) To calculate R:

$I_{B2(min)}=I_{C2} / h_{fe}= 2x10^{-3} / 200 = 10\mu$ A

Select $I_{B2} > I_{B1(min)}$ (say 25μ A)

Then $R = V_{CC} – V_{BE}$ (sat) / I_{B2}

Therefore R= $12-0.7/25x10^{-6}$=452KΩ

(iii) To calculate C:

T=0.69RC

$1x10^{-3}= 0.69x452x10^{3}xC$

C=3.2nf

To calculate R1 & R2:

$V_{B1}= \{(V_{BB}\ R1/\ R1 +R2) + (V_{CE\ (sat)}\ R2 / R1+R2)\}$

Since Q1 is in off state ,$V_{B1} \leq 0$

Then $(V_{BB}\ R1/\ R1 +R2) = (V_{CE\ (sat)}\ R2 / R1+R2)$

$V_{BB}\ R1 = V_{CE\ (sat)}\ R2$

$2\ R1 = 0.2\ R2$

Assume R1=10KΩ, then R2=100 KΩ

Consider, C_1= 25pf (commutative capacitor)

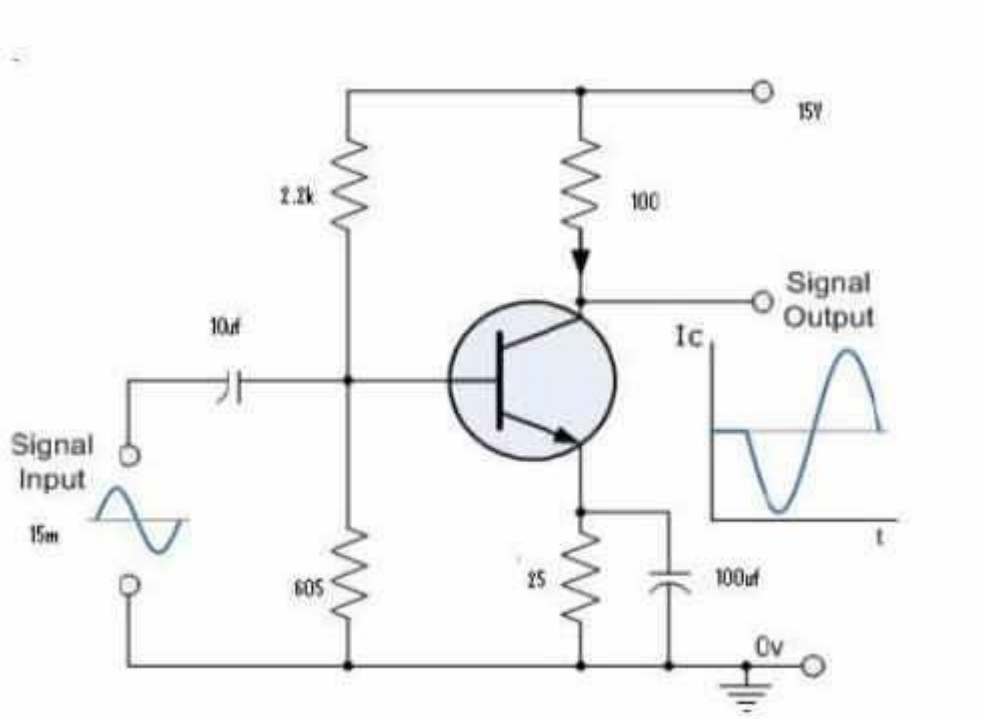
THEORY:

An electronic amplifier is used for increasing the power of a signal. It does this by taking energy from a power supply and controlling the output to match the input signal shape but with a larger amplitude. In this sense, an amplifier may be considered as modulating the output of the power supply.

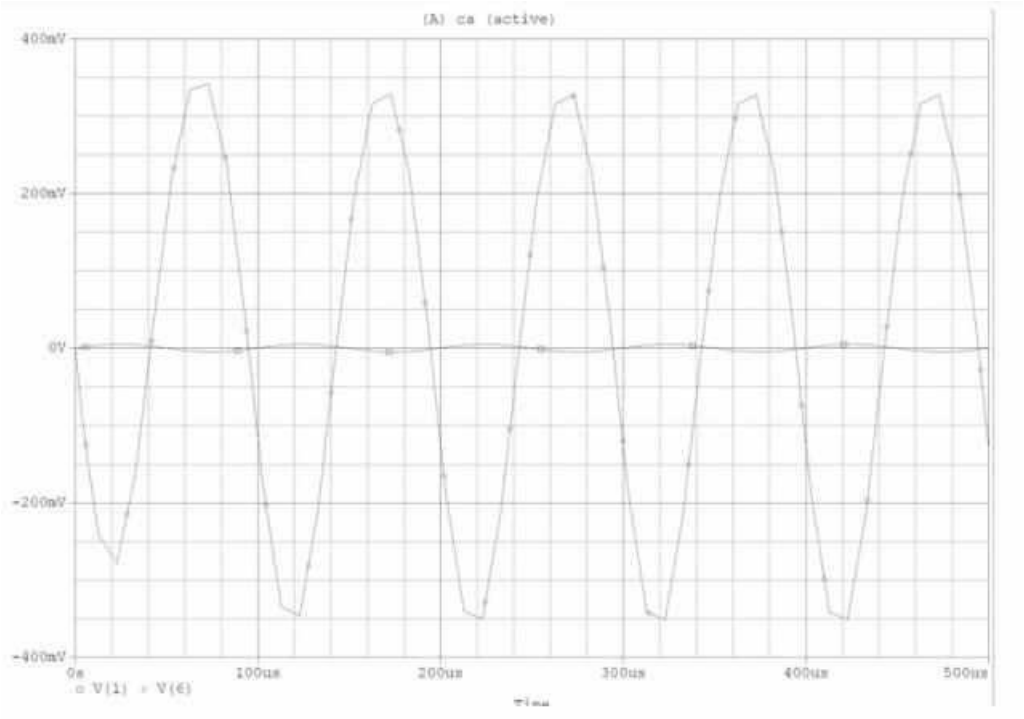
PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Give a negative trigger input to Q2.
3. Note the output of transistor Q2 and Q1.
4. Find the value of Ton and Toff.

CIRCUIT DIAGRAM:



MODEL GRAPH:



TABULATION:

S.NO	Amplitude(V)	Time period(msec)

RESULT:

Thus the Power amplifier is designed and the performance is tested.

Ex. No.: 15 Date:	VOLTAGE AND CURRENT TIME BASE CIRCUITS

AIM:

To simulate voltage and current time base circuits by using PSPICE.

APPARATUS REQUIRED:

1. PC
2. PSPICE software

THEORY:

A **time base generator**, or **timebase**, is a special type of function generator, an electronic circuit that generates a varying voltage to produce a particular waveform. Time base generators produce very high frequency sawtooth waves specifically designed to deflect the beam in cathode ray tube (CRT) smoothly across the face of the tube and then return it to its starting position.

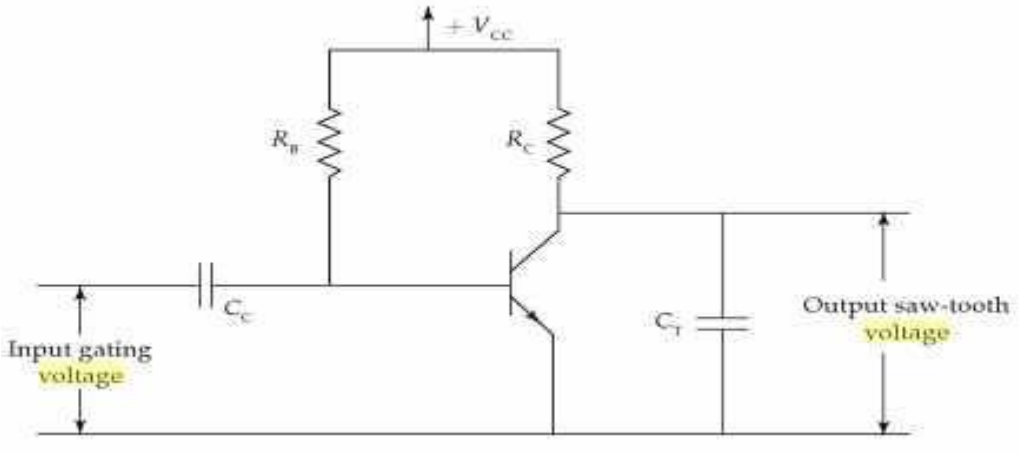
Time bases are used by radar systems to determine range to a target, by comparing the current location along the time base to the time of arrival of radio echoes. Analog television systems using CRTs had two time bases, one for deflecting the beam horizontally in a rapid movement, and another pulling it down the screen 60 times per second.Oscilloscopes often have several time bases, but these may be more flexible function generators able to produce many waveforms as well as a simple time base.

PROCEDURE:

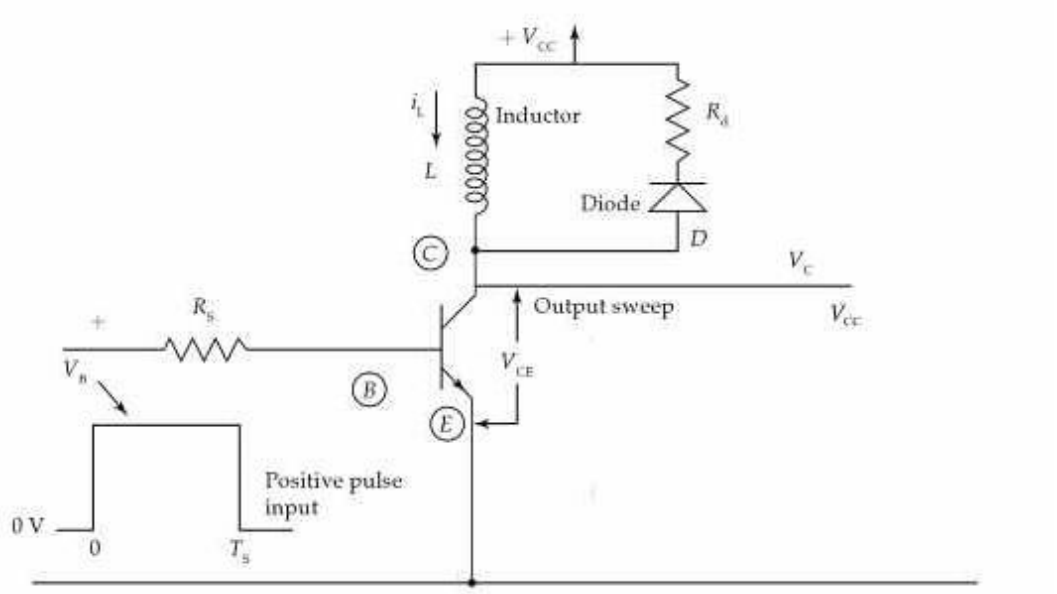
1. Click on the start menu and select the pspice simulation software
2. Select the parts required for the circuit from the parts menu and place them in the work space
3. Connect the parts using wires
4. Save the file and select the appropriate analysis
5. Simulate the circuit and observe the corresponding output waveforms

CIRCUIT DIAGRAM:

VOLTAGE TIME BASE CIRCUIT

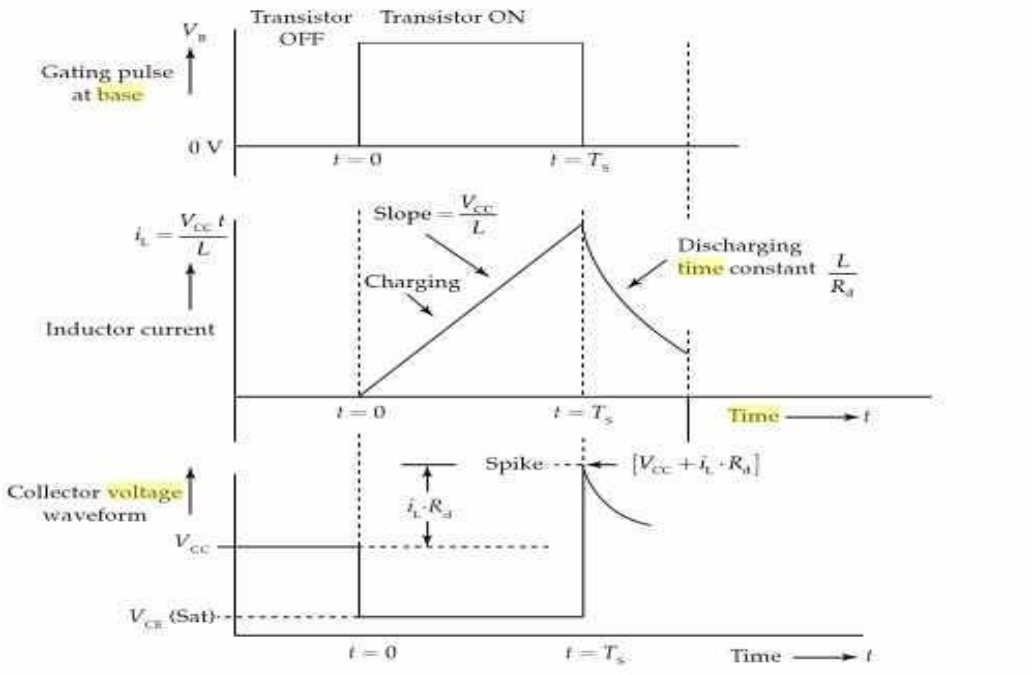


CURRENT TIME BASE CIRCUIT



MODEL GRAPH:

CURRENT TIME BASE CRCUIT



RESULT:

Thus the Voltage and Current time base circuits are simulated using Pspice.

Ex.No: 16	TWIN T OSCILLATOR

AIM:

To simulate the TWIN-T Oscillator using ORCAD PSPICE software.

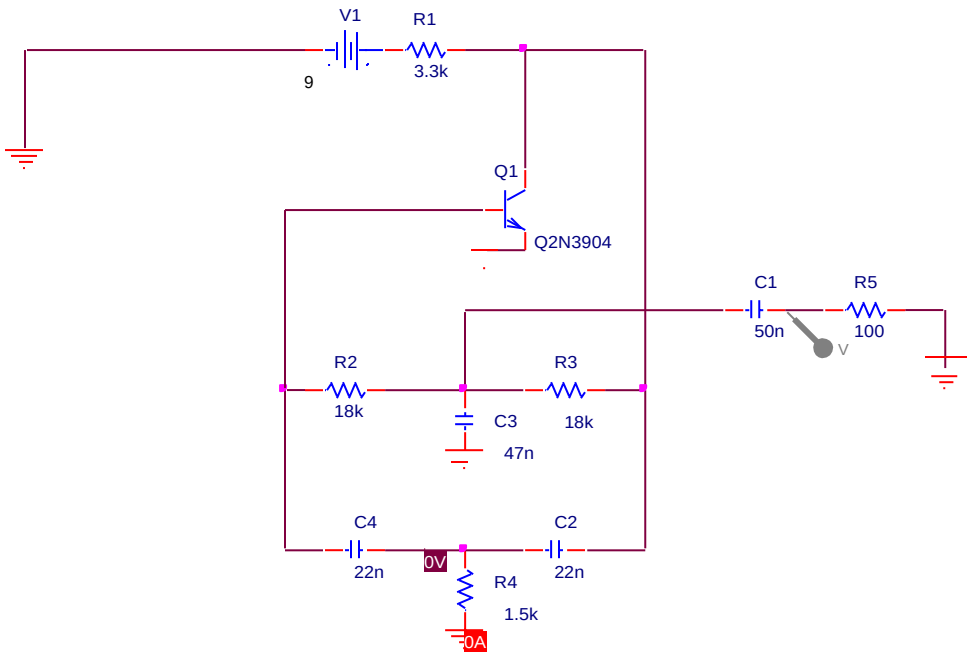
SOFTWARE REQUIRED:

ORCAD PSPICE

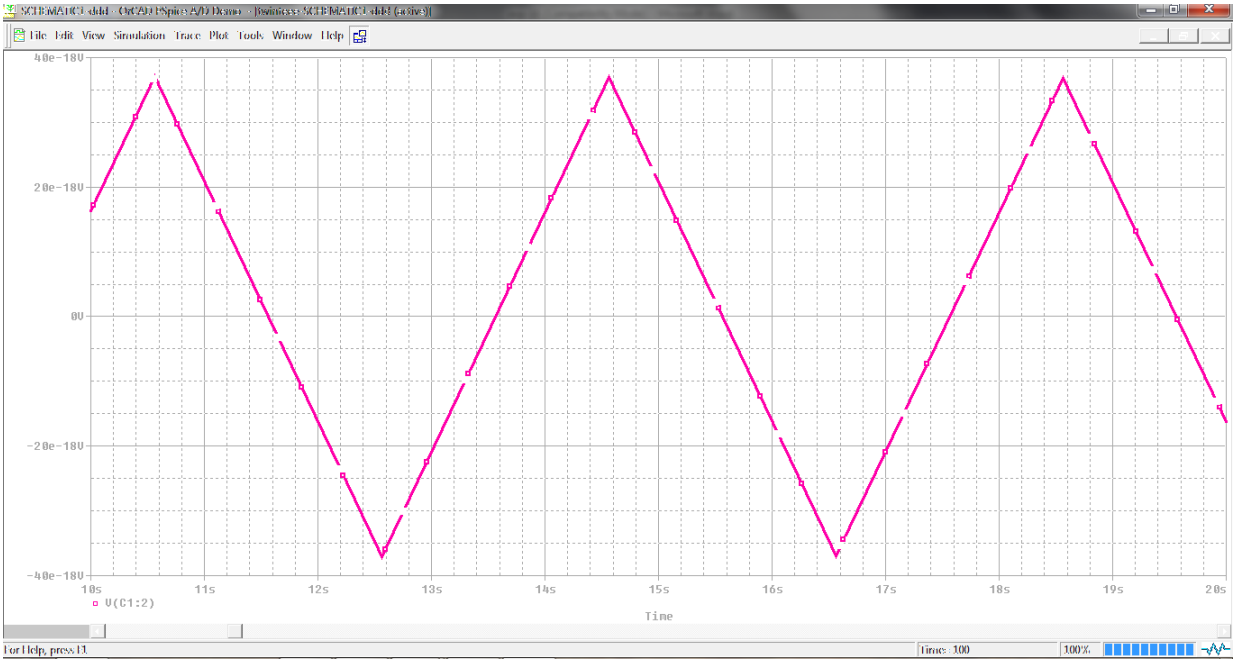
PROCEDURE:

1. Draw the circuit as per the circuit diagram.
2. Create a edit simulation title.
3. Select the type of analysis.
4. Create a new simulation file.
5. Simulate the file.

CIRCUIT DIAGRAM:



OUTPUT:



NETLIST:

*Libraries:

* Local Libraries :

* From [PSPICE NETLIST] section of pspiceev.ini file:

.lib "nom.lib"

*Analysis directives:

.TRAN 0 100s 0

.PROBE

.INC "twinteee-SCHEMATIC1.net"

**** INCLUDING twinteee-SCHEMATIC1.net ****

* source TWINTEEE

Q_Q1 N00024 N00042 0

Q2N3904R_R1 N000051 N00024

3.3k

R_R2 N00042 N00031 18k

R_R3 N00031 N00024 18k

R_R4 0 N00039 1.5k

R_R5 N00292 0 100

C_C1 N00031 N00292 50n

C_C2 N00039 N00024 22n

C_C3 0 N00031 47n

C_C4 N00042 N00039 22n

V_V1 N000051 0 9