SRI SHANMUGHA COLLEGE OF ENGINEERING AND TECHNOLOGY

SANKARI, SALEM

DEPARTMENT OF BIOMEDICAL ENGINEERING

Academic year 2021-2022 Odd Semester

(Regulation 2017)

III SEMESTER - BME

BM8312- DEVICES AND CIRCUITS LABORATORY

LAB MANUAL

PREPARED BY

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AP/ECE

LIST OF EXPERIMENTS

1. Characteristics of PN Junction Diode
2. Zener diode Characteristics & Regulator using Zener diode
3. Common Emitter input-output Characteristics
4. Common Base input-output Characteristics
5. FET Characteristics
6. SCR Characteristics
7. Clipper and Clamper & FWR
8. Verifications of Thevenin & Norton theorem
9. Verifications of KVL & KCL
10. Verifications of Super Position Theorem
11. Verifications of Maximum power transfer &Reciprocity theorem
12. Determination of Resonance Frequency of Series & Parallel RLC Circuits
13. Transient analysis of RL and RC circuits

BEYOND THE SYLLABUS

- Characteristics of UJT

Ex.No.1

CHARACTERISTICS OF PN JUNCTION DIODE

Aim:

To determine the VI characteristics of PN Diode

Apparatus required:

S.No	Name	Range	Type	Qty
1	R.P.S	(0-30)V		1

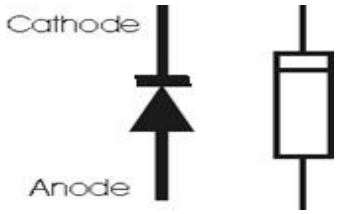
2	Ammeter	(0-5)mA, (0-25)mA		1 1
3	Voltmeter	(0-10)V (0-1)V		1 1
4	Connecting wires	-		As Required
5	Bread Board			1
6	Resistors	1KΩ		1
7	Diode- PN	BY127		1

THEORY:

A diode is a PN junction formed by a layer of P type and layer of N type Semiconductors. Once formed the free electrons in the N region diffuse across the junction and combine with holes in P region and so a depletion Layer is developed. The depletion layer consists of ions, which acts like a barrier for diffusion of charged beyond a certain limit. The difference of potential across the depletion layer is called the barrier potential. At 2.5degree the barrier potential approximately equal 0.7v for silicon diode and 0.3v for germanium diode.

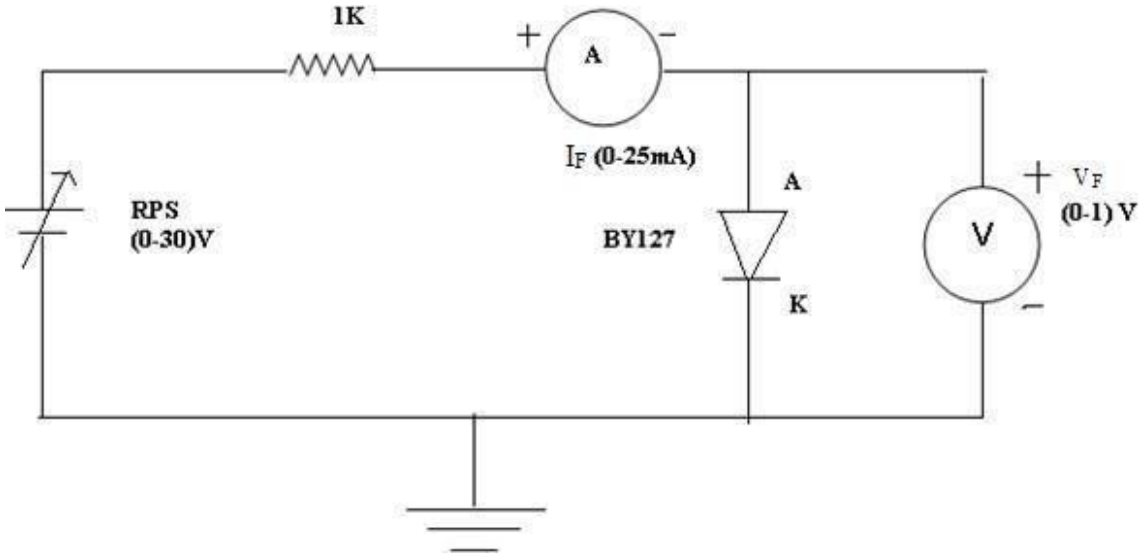
When the junction is forward bias, the majority carrier acquired sufficient energy to overcome the barrier and the diode conducts. When the junction is reverse biased the depletion layer widens and the barrier potential increases. Hence the Majority carriercannot cross the junction and the diode does not conduct. But there will be a leakagecurrent due to minority carrier. When diode is forward biased, resistance offered is zero,and when reverse biased resistance offered is infinity. It acts as a perfect switch.

PIN DIAGRAM:

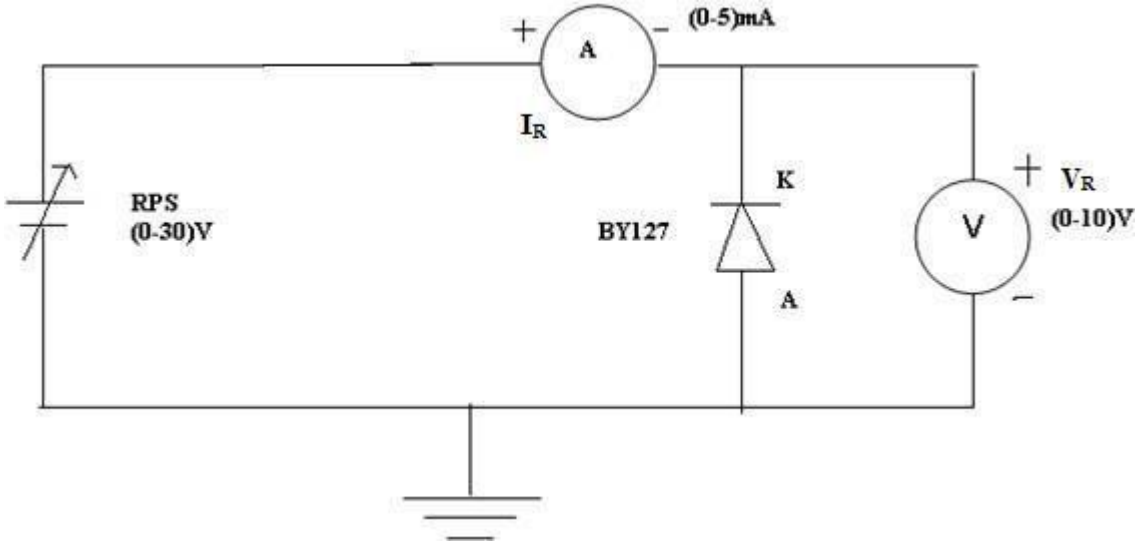


CIRCUIT DIAGRAM:

FORWARD BIAS:



REVERSE BIAS:



PROCEDURE:

FORWARD BIAS:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to anode of the diode and negative terminal to cathode of the diode.
3. Forward voltage V_f across the diode is increased in small steps and the forward current is noted.
4. The readings are tabulated. A graph is drawn between V_f and I_f.

REVERSE BIAS :

1. The connections are made as per the circuit diagram.

2. The positive terminal of power supply is connected to cathode of the diode and negative terminal to anode of the diode.
3. Reverse voltage Vr across the diode is increased in small steps and the Reverse current is noted.
4. The readings are tabulated. A graph is drawn between V_r and I_r.

TABULATION:

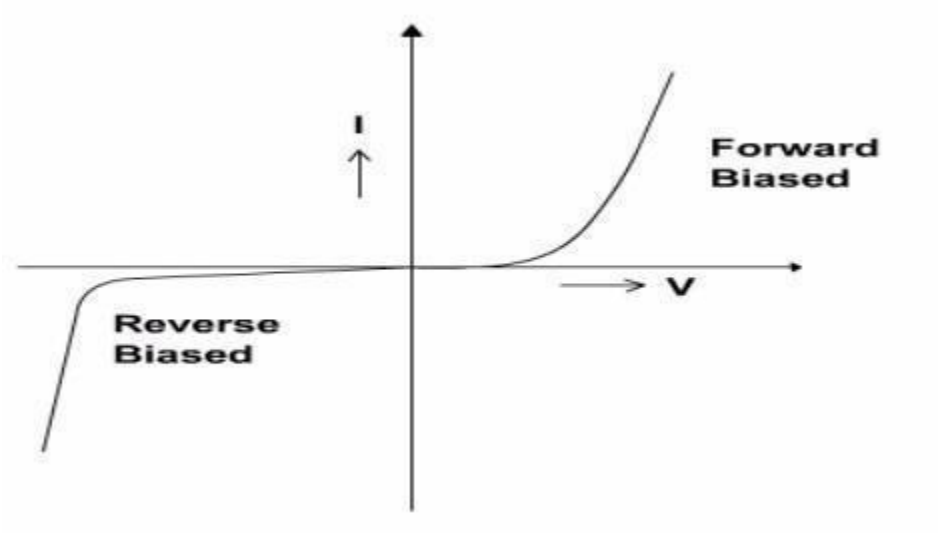
FORWARD BIAS:

V_f(volts)	I_f(mA)

REVERSE BIAS:

V_r(volts)	I_r(mA)

MODEL GRAPH



PRE REQUISITE:

1. What is a semiconductor?
2. Write the Diode current Equation.
3. What is the value of V_t at room temperature
4. What is meant by forward bias
5. What is meant by reverse bias?

REVIEW QUESTIONS:

1. How a PN junction is formed?
2. In what way the width of depletion region can be varied?
3. What is potential barrier?
4. In forward bias condition the current condition is due to _____
5. What is reverse saturation current Ico?

RESULT:

Thus the characteristics of PN-Junction diode were drawn**.**

Ex.No.2a

CHARACTERISTICS OF ZENER DIODE

Aim:

To determine the VI characteristics of Zener Diode

APPARATUS REQUIRED:

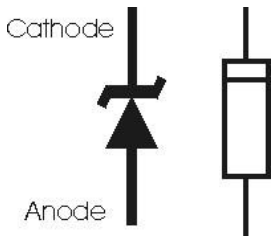
S.No	Name	Range	Type	Qty
1	R.P.S	(0-30)V		1
2	Ammeter	(0-30) mA		1
3	Voltmeter	(0-10)V (0-1)V		1 1
4	Connecting wires	-		As Required
5	Bread Board			1
6	Resistors	1KΩ		1
7	Diode- Zener	FZ 5V6/ FZ 6V2		1

THEORY:

Zener diodes have many of the same basic properties of ordinary semiconductor diodes. When forward biased, they conduct in the forward direction and have the same turn on voltage as ordinary diodes. For silicon this is about 0.6 volts.

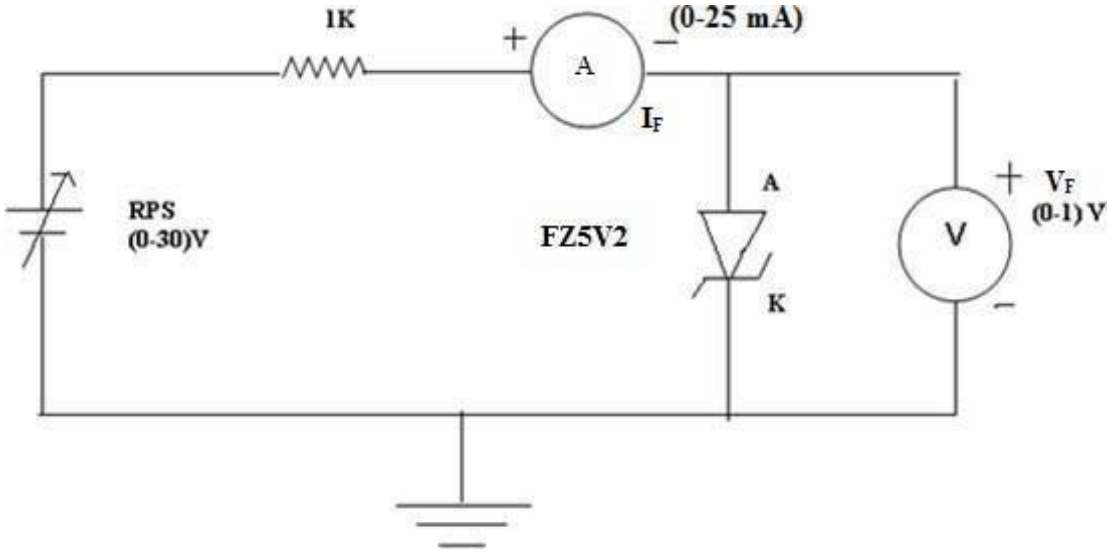
In the reverse direction, the operation of a Zener diode is quite different to an ordinary diode. For low voltages the diodes do not conduct as would be expected. However, once a certain voltage is reached the diode "breaks down" and current flows. Looking at the curves for a Zener diode, it can be seen that the voltage is almost constant regardless of the current carried. This means that a Zener diode provides a stable andknown reference voltage. Hence they are used as Voltage regulators.

PIN DIAGRAM:

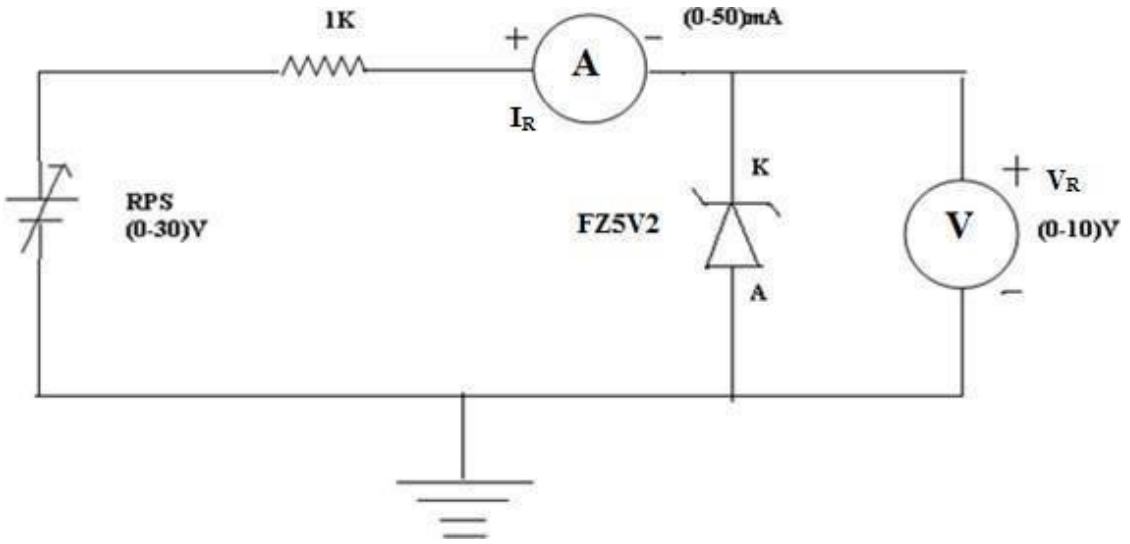


CIRCUIT DIAGRAM:

FORWARD BIAS:



REVERSE BIAS:



PROCEDURE:

FORWARD BIAS:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to anode of the diode and negative terminal to cathode of the diode.
3. Forward voltage V_f across the diode is increased in small steps and the forward current is noted.
4. The readings are tabulated. A graph is drawn between V_f and I_f.

REVERSE BIAS:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to cathode of the diode and negative terminal to anode of the diode.
3. Reverse voltage V_r across the diode is increased in small steps and the Reverse current is noted.
4. The readings are tabulated. A graph is drawn between V_r and I_r.

TABULAR COLUMN:

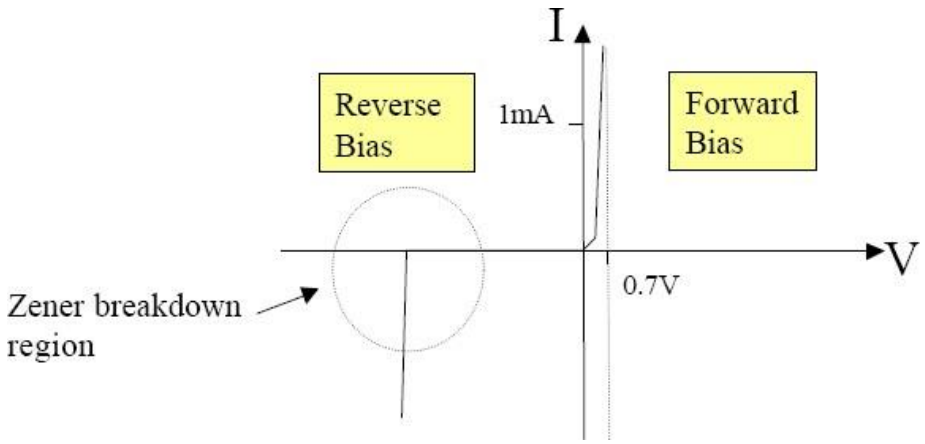
FORWARD BIAS:

V_f(volts)	I_f(mA)

REVERSE BIAS:

V_r(volts)	I_r(mA)

MODEL GRAPH



PRE REQUISITE:

1. How the name of the Zener came?
2. What is cause of reverse breakdown?
3. What is Zener voltage?
4. Write the Symbol for the Zener diode.
5. What are the different types of breakdowns in semiconductor junctions?

REVIEW QUESTIONS:

1. What is the difference between p-n Junction diode and Zener diode
2. Can we use Zener diode as a switch?
3. Explain working of a Zener Diode
4. What is the max value of voltage of Zener breakdown devices
5. What is cause of reverse breakdown

RESULT:

Thus the characteristics of Zener diode were drawn**.**

Ex.No.2b

ZENER DIODE AS A VOLTAGE REGULATOR

Aim:

To study the Zener Diode as Voltage Regulator.

APPARATUS REQUIRED:

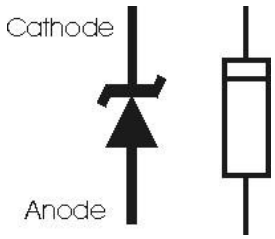
S.No	Name	Range	Type	Qty
1	R.P.S	(0-30)V		1
2	Ammeter	(0-30) mA		1
3	Voltmeter	(0-10)V (0-1)V		1 1
4	Connecting wires			As Required
5	Bread Board			1
6	Resistors	1KΩ		1
7	Diode- Zener	FZ 5V6/ FZ 6V2		1

THEORY:

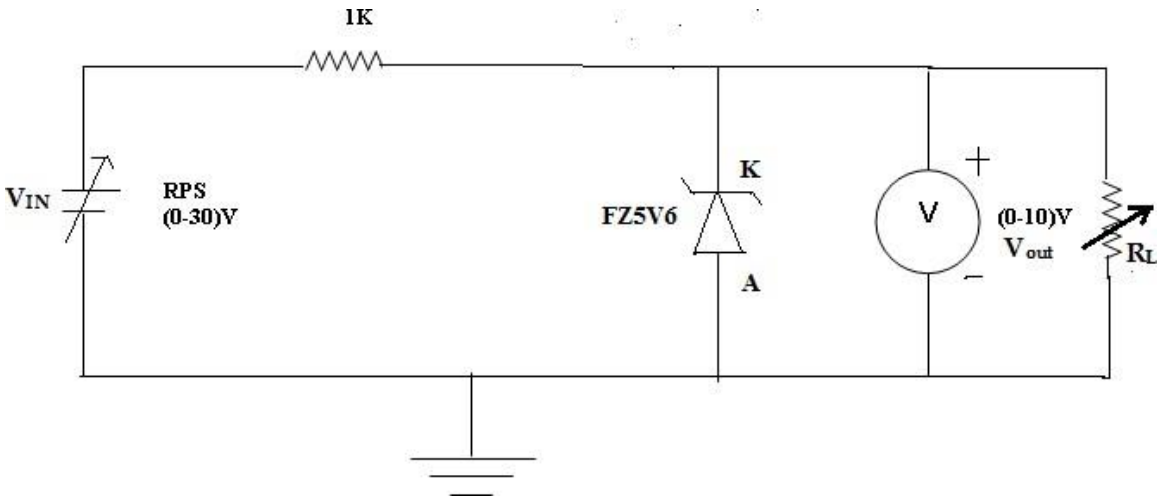
Zener diodes have many of the same basic properties of ordinary semiconductor diodes. When forward biased, they conduct in the forward direction and have the same turn on voltage as ordinary diodes. For silicon this is about 0.6 volts.

In the reverse direction, the operation of a Zener diode is quite different to an ordinary diode. For low voltages the diodes do not conduct as would be expected. However, once a certain voltage is reached the diode "breaks down" and current flows. Looking at the curves for a Zener diode, it can be seen that the voltage is almost constant regardless of the current carried. This means that a Zener diode provides a stable andknown reference voltage. Hence they are used as Voltage regulators.

PIN DIAGRAM:



CIRCUIT DIAGRAM:



PROCEDURE:

1. The connections are made as per the circuit diagram.
2. Keep Load resistance R_L constant.
3. Vary the Input voltage and note down the corresponding output voltage.
4. Now keep voltage constant vary the R_L and note down the voltmeter corresponding reading.
5. Plot the respective regulations graph.

TABULAR COLUMN:

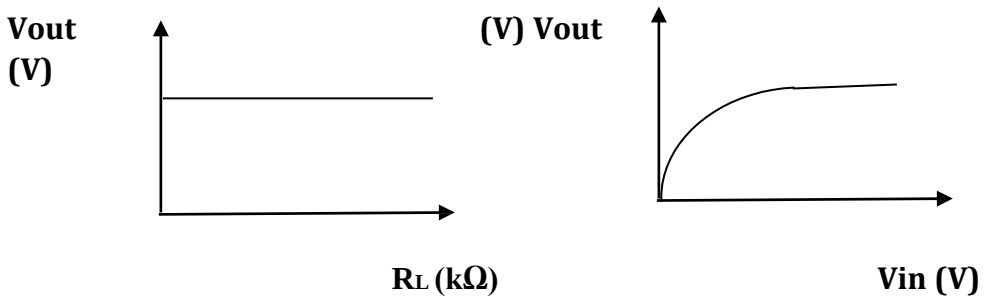
LOAD REGULATION:

R_L (kΩ)	Vout (V)

LINE REGULATION:

Vin (V)	Vout (V)

MODEL GRAPH



LOAD REGULATION **LINE REGULATION**

PREREQUISITE

1. How Zener diode acts as a voltage regulator.
2. Explain working of a Zener Diode
3. Compare Zener and avalanche Breakdown.

REVIEW QUESTIONS:

1. What are the applications of Zener diode?
2. What is voltage regulator?
3. What is cut-in-voltage?
4. What is break down voltage?
5. Draw characteristics of Zener Diode under Forward & Reverse Bias Conditions

RESULT:

Thus the Zener diode as a Voltage Regulator were studied**.**

Ex.No:3 CHARACTERISTICS OF CE CONFIGURATION

AIM:

To plot the transistor characteristics (INPUT & OUTPUT) of CE configuration.

APPARATUS REQUIRED:

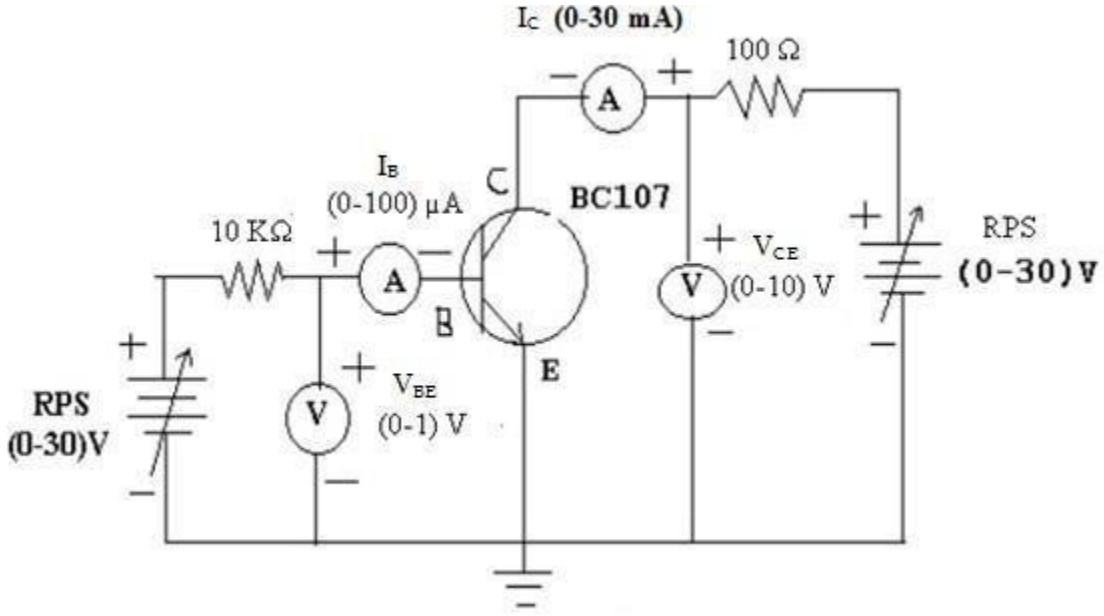
S.No.	COMPONENTS	SPECIFICATION	QTY
1	Transistor BC 107	Max Rating : 50V 1A, 3W	1
2	Resistors	10KΩ,100Ω	2
3	Regulated power supply	(0-30) V	1
4	Voltmeters	Mc (0-10) V Mc (0-1) V	1 1
5	Ammeters	Mc (0-30) mA Mc (0-100)μA	1 1
6	Bread board & connecting wires		As Required

THEORY:

A NPN function transistor consist of a silicon (or germanium) crystal in which a layer of p – type silicon is sandwiched between two layers of N – type silicon. The arrow on emitter lead specifies the direction of the current flow when the emitter – base functionis biased in the forward direction since the conductivity of the BJT depends on both the majority and minority carriers it is called bipolar device. In CE configuration, Emitter is common to both the Emitter and Base.

PIN DIAGRAM OF BC107

CIRCUIT DIAGRAM:



DESCRIPTION:

Input Characteristics:

Voltage across Base Emitter junction V_{BE} vs I_B, where V_{CE} constant

Output Characteristics:

Voltage across Collector Emitter junction V_{CE} vs I_C where I_B constant

PROCEDURE:

Input Characteristics:

1. Connections are made as per the circuit diagram.
2. V_{CE} is kept constant (say 2v), V_{BE} is varied insteps of 0.1v and the corresponding I_B values are tabulated. The above procedure is repeated for 1V etc.
3. Graph is plotted between V_{BE} vs I_B, where V_{CE} constant.

Output Characteristics:

1. Connection are made as per the circuit diagram
2. I_B is kept constant, V_{CE} is varied in step IV the corresponding I_C values are tabulated. The above procedure is repeated for different constant values.
3. Graph is plotted between V_{CE} and Ic for a constant I_B.

TABULATION:

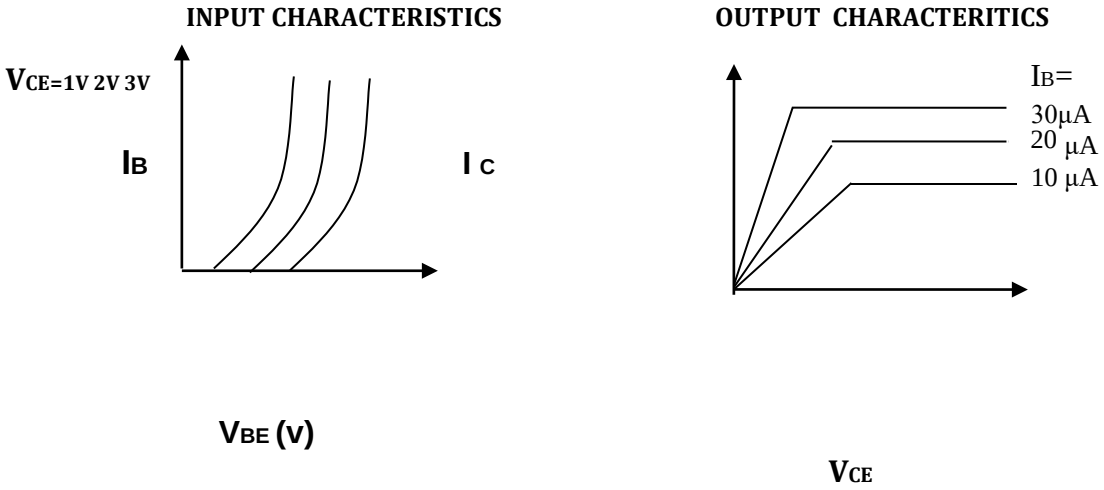
Input Characteristics:

V_{CE} = V		V_{CE} = V	
V_{BE}(V)	I_B (µA)	V_{BE}(V)	I_B(µA)

Output characteristics:

I_B = µA		I_B = µA	
V_{CE}(V)	I_C (mA)	V_{CE}(V)	I_C(mA)

MODEL GRAPH:



PRE REQUISITE:

1. List the current components of BJT in CE configuration
2. What is Early Effect?
3. Why the doping of collector is less compared to emitter?
4. What do you mean by "reverse active"?
5. What is the difference between CE and Emitter follower circuit?

REVIEW QUESTIONS:

1. Explain the operation of CE configuration
2. Determine the output resistance and input resistance
3. Define current gain in CE configuration?
4. Why CE configuration is preferred for amplification

RESULT:

Thus the input and output characteristic of BJT in Common Emitter mode is drawn.

Ex.No:4

CHARACTERISTICS OF CB CONFIGURATION

AIM:

To plot the transistor characteristics (INPUT & OUTPUT) of CB configuration.

APPARATUS REQUIRED:

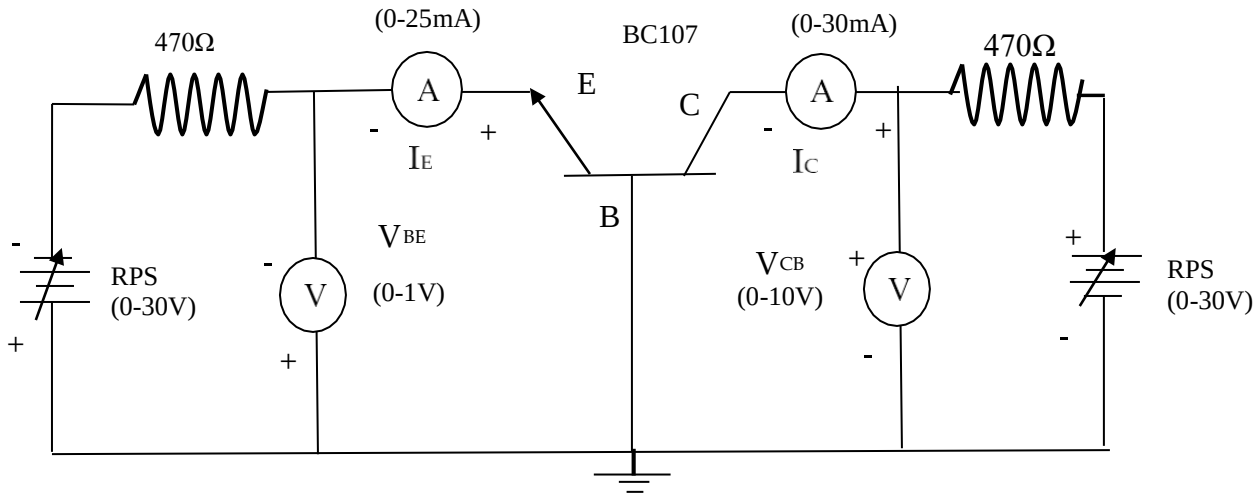
S.No.	COMPONENTS	SPECIFICATION	QTY
1	Transistor BC 107	Max Rating : 50V 1A, 3W	1
2	Resistors	470Ω	2
3	Regulated power supply	(0-30) V	1
4	Voltmeters	Mc (0-10) V Mc (0-1) V	1 1
5	Ammeters	Mc (0-30) m A	2
6	Bread board & connecting wires	-	1

THEORY:

A NPN function transistor consist of a silicon (or germanium) crystal in which a layer of p – type silicon is sandwiched between two layers of N – type silicon. The arrow on emitter lead specifies the direction of the current flow when the emitter – base functionis biased in the forward direction since the conductivity of the BJT depends on both the majority and minority carriers it is called bipolar device. In CB configuration, base is common to both the emitter and collector.

PIN DIAGRAM OF BC107

CIRCUIT DIAGRAM:



DESCRIPTION:

Input Characteristics:

Voltage across Base Emitter junction V_{BE} vs I_E, where V_{CB} constant

Output characteristics:

Voltage across Collector Emitter junction V_{BC} vs I_C where I_E constant

PROCEDURE:

Input Characteristics:

1. Connections are made as per the circuit diagram.
2. V_{CB} is kept constant (say 2v), V_{BE} is varied insteps of 0.1v and the corresponding I_E values are tabulated. The above procedure is repeated for 1V etc.
3. Graph is plotted between V_{BE} vs I_E, where V_{CB} constant.

Output Characteristics:

1. Connection are made as per the circuit diagram
2. I_E is kept constant, V_{BC} is varied in step IV the corresponding I_C values are tabulated. The above procedure is repeated for different constant values.
3. Graph is plotted between V_{BC} and Ic for a constant I_E.

TABULATION:

Input Characteristics:

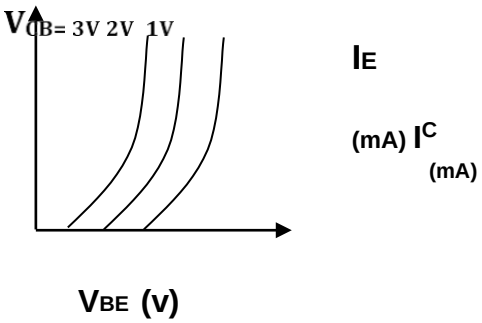
V_{CB} = V		**V_{CB} = V**	
V_{BE} (V)	**I_E (mA)**	**V_{BE} (V)**	**I_E (mA)**

Output Characteristics:

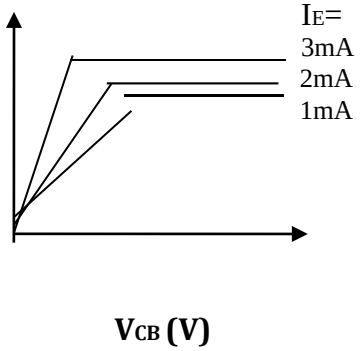
I_E= mA		**IE= mA**	
V_{BE} (V)	**I_C (mA)**	**V_{BE} (V)**	**I_c (mA)**

MODEL GRAPH:

INPUT CHARACTERISTICS



OUTPUT CHARACTERITICS



PRE REQUISITE:

1. Explain the operation of CB configuration
2. Determine the output resistance
3. Determine input resistance
4. Explain input characteristics
5. Explain output characteristics

REVIEW QUESTIONS:

1. Bring out the comparison of CC and CB transistor parameters
2. Give the relation of Ebers moll equation.
3. Bring out the comparison of CEand CB transistor parameters

4. Draw input and output characteristics of CB?
5. Explain Gummen poll model

RESULT:

Thus the input and output characteristic of BJT in Common Base mode is drawn.

EX .NO-5

CHARACTERISTICS OF JFET.

AIM:

To plot the drain and transfer characteristics of JFET & to find drain resistance, trans conductance, amplification factor, drain saturation current I_{DSS} and Pinch off voltage.

APPARATUS REQUIRED:

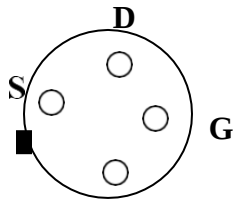
S.No.	Components	Specification	Qty
1	FET	BFW10 I_{dss}> 8 mA, Vp<8V	1
2	Resistors	1KΩ	1
3	Regulated dual power supply	MC (0-30)V	1
4	Voltmeters	MC (0-10)V MC (0-25)V	1 1
5	Ammeters	MC (0-25) mA	1
6	Bread board & connecting wires		

THEORY:

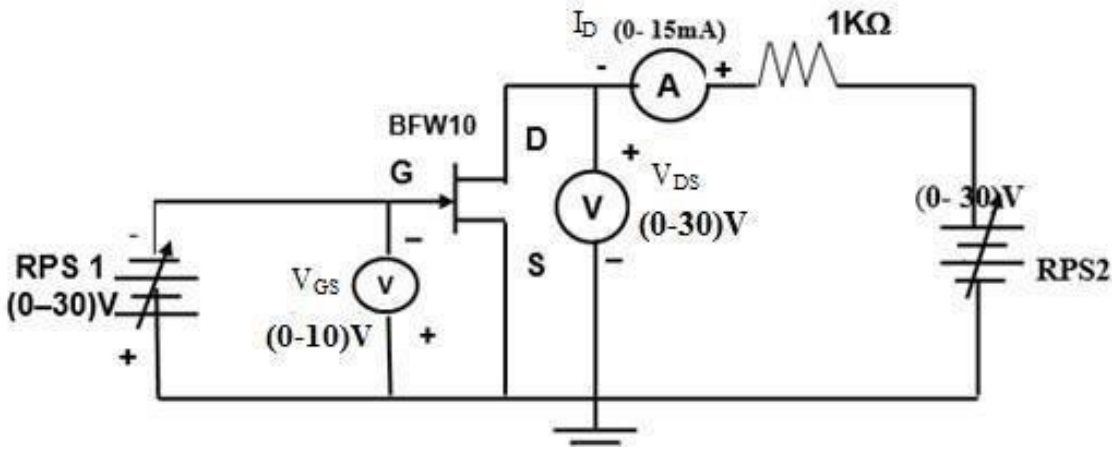
Field effect transistor is a semiconductor device that depends for its operation on the control of current by an electric field. It's operation depends on the flow of majority carriers only. It is therefore a unipolar device. It exhibits a high input resistance. An N- channel JFET

consists of a N-type bar is sandwiched between two heavily doped Persians. Due to the concentration gradient, the depletion region formed. On both sides of the semiconductor bar the ohmic contacts are made. One terminal is called source & other is called drain. Both the p-type regions are connected together.

PIN DIAGRAM OF BFW10



CIRCUIT DIAGRAM



DESCRIPTION:

DRAIN CHARACTERISTICS

INPUT: Drain voltage V_{DS} is varied insteps of 1V, VGS is kept constant OUTPUT:

Drain current I_D

TRANSFER CHARACTERISTICS

INPUT: Gate – source voltage V_{GS} is varied, Drain –source voltage V_{DS} is kept constant OUTPUT**:**

Drain current I_D

PROCEDURE:

Drain Characteristics:

1. Connections are made as per the circuit diagram.
2. Gate –source voltage V_{GS} is kept constant (say –1v), drain voltage V_{DS} is varied insteps of 1v and the corresponding drain current I_D values are tabulated.
3. The above procedure is repeated for V_{GS}= -2v, 0v.
4. The graph is plotted V_{DS} and I_D for a constant V_{GS}. 5. The drain resistance is found from the graph

$$r_d = \Delta V_{DS} / \Delta I_D$$

Transfer Characteristics:

1. Connections are made as per the circuit diagram.
2. Drain –source voltage V_{DS} is kept constant (say 5v), the gate – source voltage V_{GS} is varied insteps of 1v (-VE voltage) and the corresponding drain current I_D values are tabulated.
3. The above procedure is repeated for V_{DS} = 10v, 15v, 4. Graph is plotted between V_{GS} and I_D for a constant V_{DS}.
5. The trans conductance is found from the graph

$$g_m = \Delta I_D / \Delta V_G$$

TABULAR COLUMN:

Drain characteristics

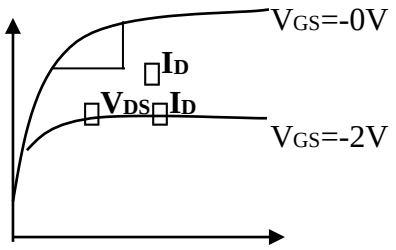
V_{GS} = V		**V_{GS} = V**	
V_{DS} (V)	**I_D (mA)**	**V_{DS} (V)**	**I_D (mA)**

Transfer characteristics

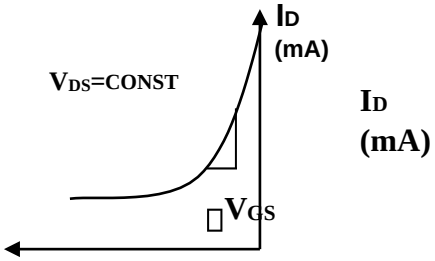
V_{DS} = V		**V_{DS}** =V	
V_{GS} (V)	**I_D (mA)**	**V_{GS} (V)**	**I_D (mA)**

MODEL GRAPH:

DRAIN CHARACTERISTICS



TRANSFER CHARACTERISTICS



CALCULATION

Transconductance $g_m = \Delta I_D/\Delta V_G$

Drain resistance $r_d = \Delta V_{DS} / \Delta I_D$ Amplification factor

$\mu = g_m r_d$

PRE REQUISITE:

1. Why it is called by name “field effect transistor”?
2. What are the advantage of FET OVER BJT?
3. What are the disadvantages of FET?
4. What is the significance of arrowhead in FET symbol?
5. Why FET is called unipolar device

REVIEW QUESTIONS:

1. Define VVR.
2. Why MOSFET is preferred than FET?
3. What are the differences between FET & MOSFET?
4. What are the applications of FET?
5. Why FET is called us voltage controlled device?

RESULT:

Thus the drain and transfer for characteristics of JFET is drawn.

Drain resistance r_d =

Trans conductance g_m =

Amplification factor =

EX NO: 6

CHARACTERISTICS OF SCR

AIM:

To construct a circuit using SCR to draw its Firing Characteristics.

APPARATUS REQUIRED:

S.No	Components	Specification	Quantity
1	SCR	TYN410	1
2	Dual RPS	(0-30)V	1
3	Resistor	560 Ω, 470Ω (0.5W)	1 each
4	Ammeter	(0-25)mA (0-100)mA	1 1
5	Voltmeter	(0-30)V	1
6	Bread board		1

THEORY:

The SCR consists of four layers of semiconductor material alternatively P type and N type. It can be brought of as an ordinary rectifier with a control element .The control element is called GATE. The gate current determines the anode to cathode voltage at which the device starts to conduct.

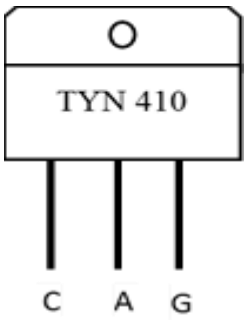
It means that gate terminal of the SCR is controlled by the applied voltage. Once switched ON the gate has no further control. To switch the SCR the anode currenthas to be reduced below a certain level called HOLDING CURRENT.

The SCR can be triggered ON with the gate or amplitude triggering, pulse triggering methods. The terms ON & OFF are used to represent the conduction andblocking mode of

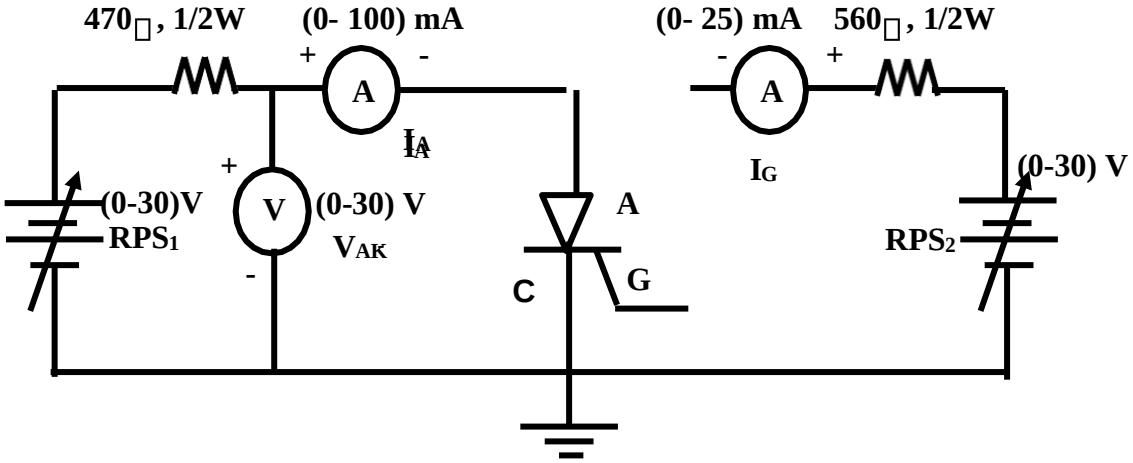
SCR respectively open circuited with the anode to cathode voltage made large enough .In conduction state the SCR behaves as an ordinary diode.

The anode to cathode voltage at which the SCR conducts is called BREAK OVER VOLTAGE or FORWARD BLOCKING VOLTAGE. It has great switching speed than other devices.

PIN DIAGRAM:



CIRCUIT DIAGRAM:



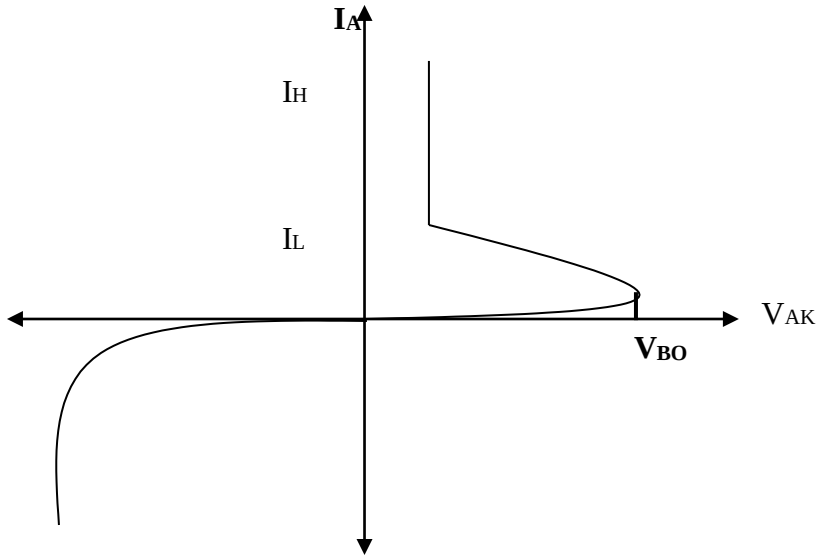
PROCEDURE:

1. Give the circuit connections as per the diagram.
2. Set V_{AK} to 10V using RPS_1
3. Increase Gate Current using RPS_2till the VAK suddenly drops down. Note the gate current at this point. This is known as firing current.
4. Set the firing current in I_G.
5. Increase the Anode voltage using RPS_1 in steps so that both I_A increases. Note down change in V_{AK}.
6. Note the maximum I_A. This is known as Holding current (I_H).
7. Remove the Gate terminal (ie). Make the gate open.
8. Anode current drops now and reaches minimum which is called Latching current (I_L).

TABULAR COLUMN:

	V_{AK}= v	I_A (mA)	I_G (mA)
Before Firirng At Firing After Firirng			

MODEL GRAPH:



PRE REQUISITE:

1. What is an SCR?
2. What are the methods to trigger ON SCR?
3. What is meant by break over voltage of SCR?
4. What is meant by holding current and latching current in SCR?
5. SCR a unidirectional or bidirectional device.

REVIEW QUESTIONS:

1. What is meant by Valley Point and Peak point
2. After triggering an SCR, the gate pulse is removed. What is the state (ON or OFF) of the device at this condition? Justify our answer
3. Why is Peak Reverse Voltage Important?

4. What is asymmetrical SCR?
5. What is the difference between SCR and TRIAC?

RESULT:

Thus the characteristics of the SCR is drawn.

Forward break over voltage =
Latching Current =
Holding Current =

Ex.No:7

CLIPPER AND CLAMPER

AIM:

To construct and study the operation of clipper and clamper circuits.

APPARATUS REQUIRED:

S.No	COMPONENTS	RANGE/SPECIFICATION	QUANTITY
1.	Resistor	4.7KΩ,100KΩ	1each
2.	Capacitor	0.1μf	1
3.	Diode	IN4001	1
4.	AFG	1MHz	1
5.	CRO	30MHz	1
6.	Bread Board		1
7.	Regulated power supply	(0 – 30)V	1

THEORY:

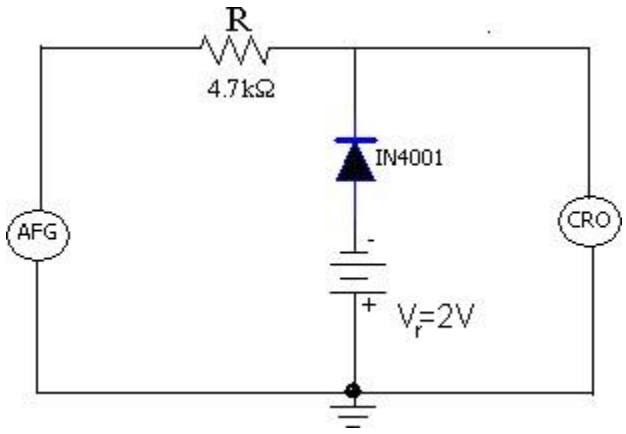
The basic action of a clipper circuit is to remove certain portions of the waveform, above or below certain levels as per the requirements. Thus the circuits which are used to clip off unwanted portion of the waveform, without distorting the remaining part of the waveform are called clipper circuits or Clippers. The half wave rectifier is the best and simplest type of clipper circuit which clips off the positive/negative portion of the input signal. The clipper circuits are also called limiters or slicers.

PROCEDURE

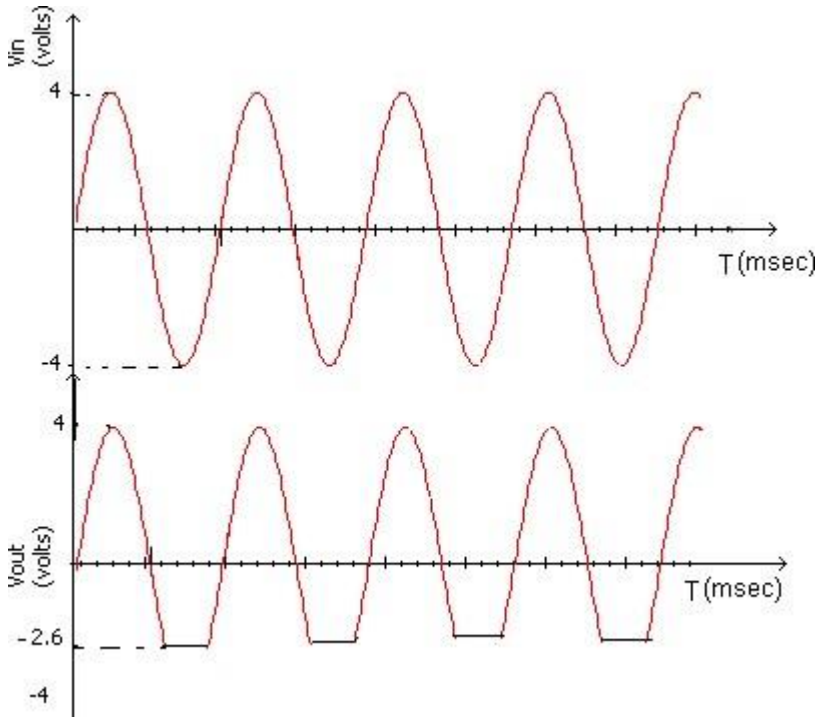
Clipper Circuit

1. Connect the components and apparatus as shown in the circuit diagram.
2. Set input, sinusoidal signal of 8Vp-p and 1 kHz frequency and the reference voltage as 2V using RPS.
3. Observe the output across the diode using CRO.
4. Plot the input and output signal in a linear graph.

NEGATIVE PEAK CLIPPER



MODEL GRAPH



Theoretical calculations:

Vr=2v, Vγ=0.6v

When the diode is forward biased Vo =-(Vr+ Vγ) = -(2v+0.6v)= -2.6v

When the diode is reverse biased the Vo=Vi

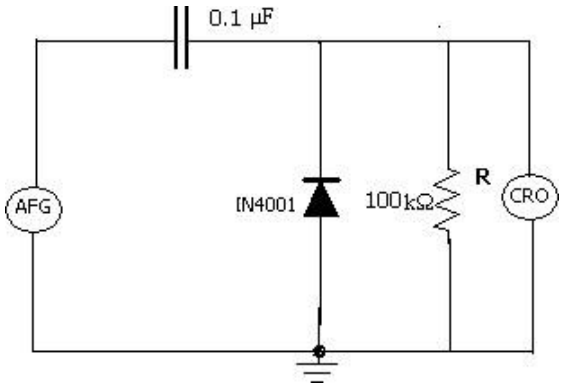
PROCEDURE

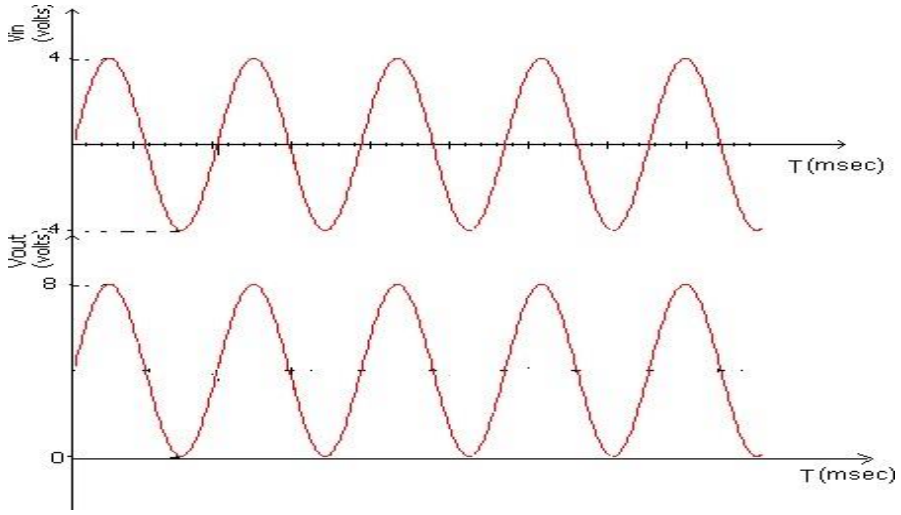
Clamper Circuit

1. Connect the components and apparatus as shown in the circuit diagram.
2. Set input, sinusoidal signal of 8Vp-p and 1kHz frequency
3. Observe the output across the load resistance using CRO.
4. Plot the input and output signal in a linear graph.

CIRCUIT DIAGRAM

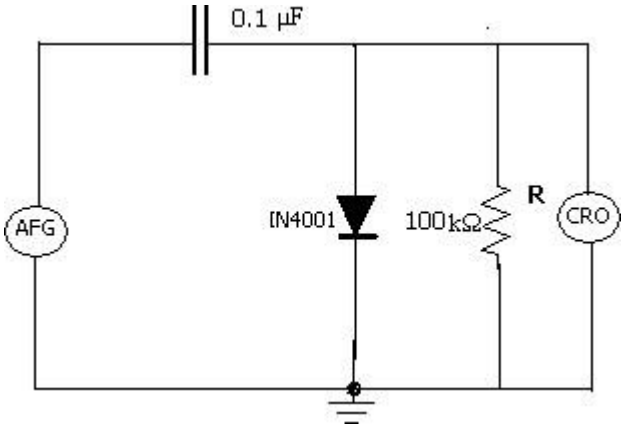
POSITIVE CLAMPER

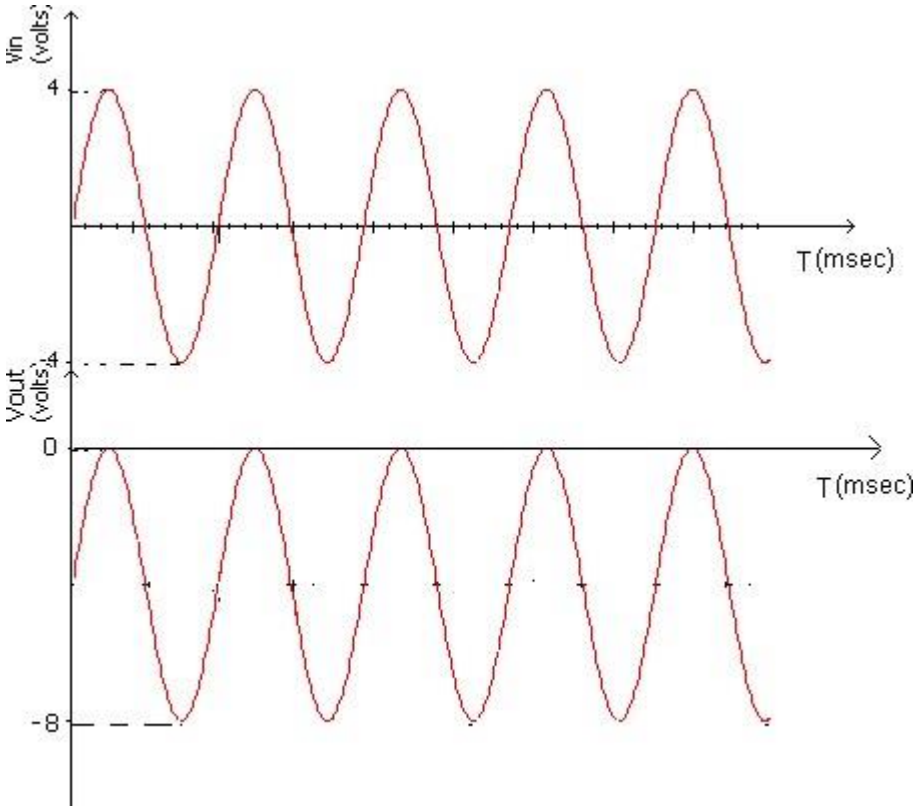




CIRCUIT DIAGRAM

NEGATIVECLAMPER





PRE REQUISITE

1. What is clipper?
2. What is clamper?
3. Difference between clipper and clamper?
4. What are different types of clampers?
5. Positive base and negative base clippers means

REVIEW QUESTIONS:

1. How does a clamper circuit add a dc level to the output voltage?
2. What I do you mean by biased and combinational clipper?
3. What are the classifications of a clipper circuit?
4. Why capacitors are used in clampers?
5. What happens in the output waveform if the polarity of capacitor is changed in the clampers

RESULT:

Thus the clipper and clamper circuits are designed and the output waveforms are observed.

Ex.No:8

VERIFICATION OF THEVENIN'S & NORTON'STHEOREM

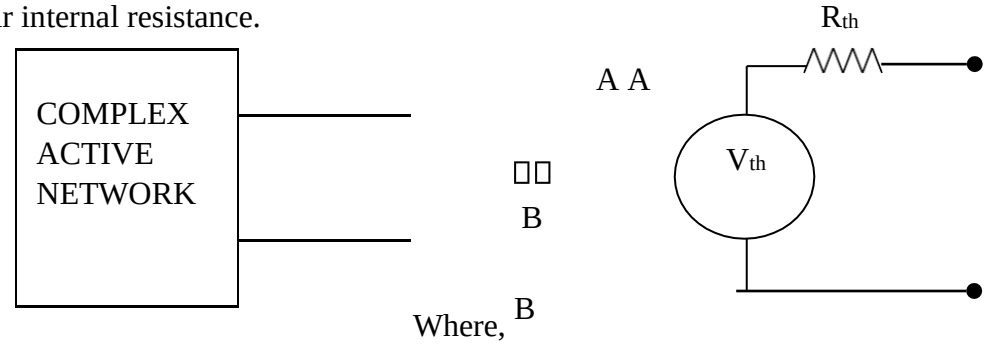
AIM:

a. To verify the Thevenin's theorem for the given electric circuit.
b. To verify the Norton's theorem for the given circuit.

THEVENIN'S THEOREM

STATEMENT:

A one port linear, active, resistive network which contains one or more voltage or current sources can be replaced by a single voltage source V_{th} in series with a single resistance R_{th}. V_{th} is equal to the open circuit voltage across the port terminals of the network & the resistance R_{th} is measured between the port terminals with all the energy sources replaced by their internal resistance.



Where,

R_{th} - Thevenin's resistance. V_{th} -Thevenin's voltage.

APPARATUS REQUIRED:

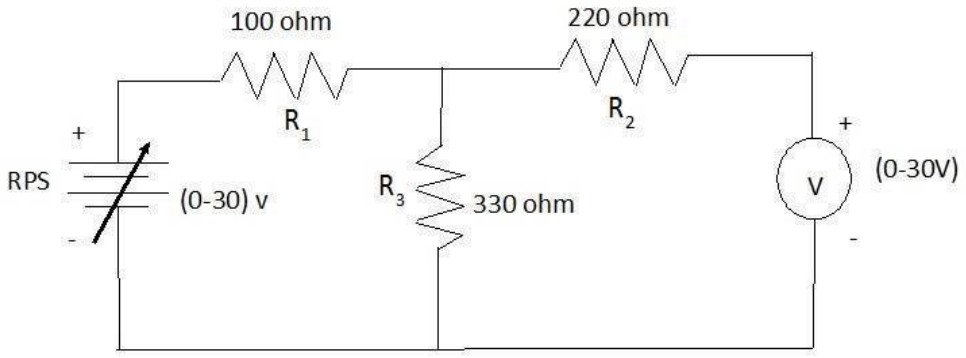
S.No	Name	Range	Qty
1	R.P.S	(0-30) V	1
2	Ammeter	0-50 mA	2
3	Voltmeter	0 – 25V	2
4	Connecting wires		
5	Resistors	1K, 2.2K3.3K,4.7K,6.8K,10K	Each 2
6	Breadboard		1

PROCEDURE:

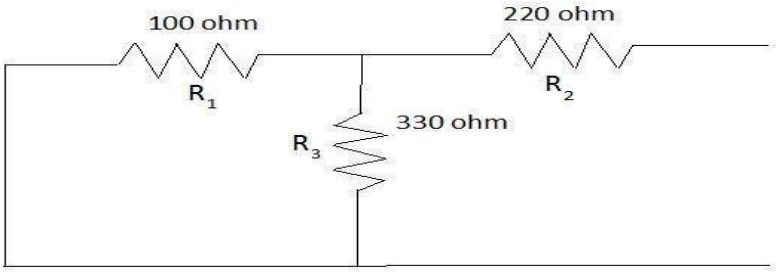
1. To Find Vth :(Under open circuit the load resistance)
    a) Connections are made as per the circuit diagram.
    b) Switch on the power supply and note down the voltmeter readings Vth.

2. To Find Rth (Under short circuit Voltage source)
    a) Connections are given as per the circuit diagram.
    b) Switch ON the Power supply.
    c) Vary the R.P.S to fixed voltage, note down the ammeter and voltmeter readings.
    d) Repeat the step (ii) for various R.P.S voltage and tabulate the readings.
3. To Find I_L
    a) Connections are given as per the circuit diagram.
    b) Switch ON the power supply.
    c) Vary the R.P.S. to the given voltage and note down the ammeter reading (I_L).

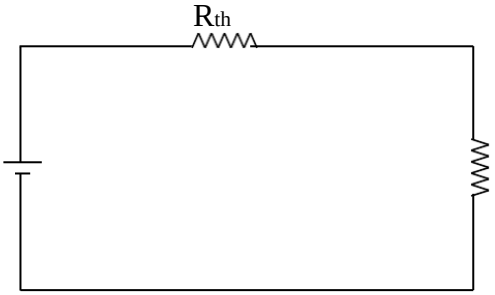
CIRCUIT DIAGRAM: I



To find R_{th}:



Thevinin's Equivalent Circuit:



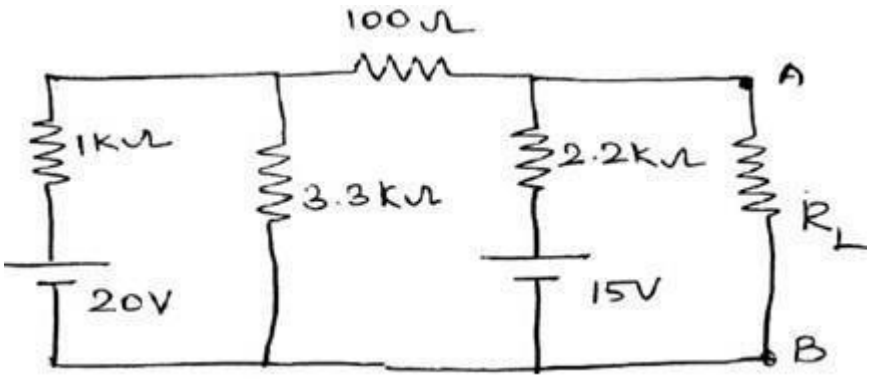
V_{th}

$$I_L = \frac{V_{th} R_L}{R_{TH} + R_L}$$

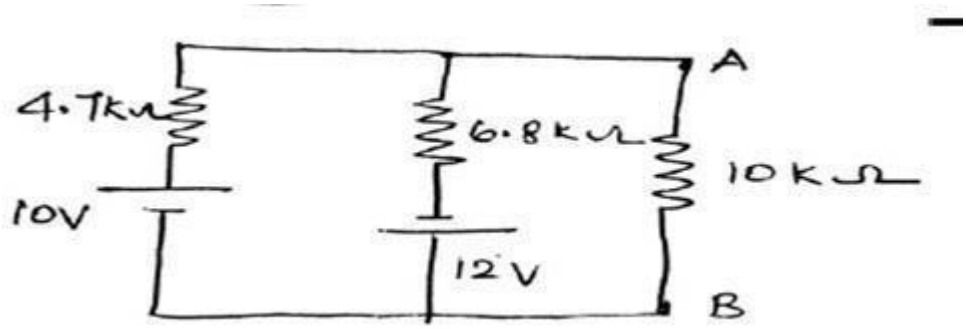
TABULATION:

S.No	Specified voltage (Volts)	Theoritical			Practical		
		Vth	Rth	IL	Vth	Rth	IL

CIRCUIT DIAGRAM: II



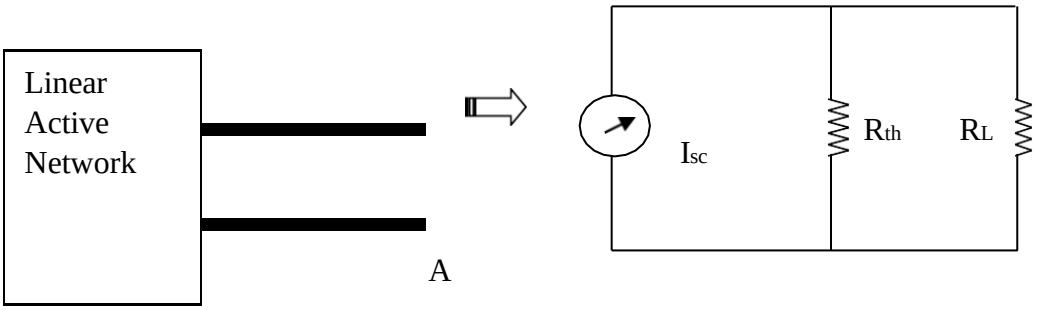
CIRCUIT DIAGRAM: III



B. NORTON'S THEOREM

Statement:

A one port linear, active, resistive network which contains one or more voltage or current sources can be replaced by a single current source I_{SC} in parallel with a single resistance R_{th}. I_{SC} is equal to the short circuit current across the port terminals of the network & the resistance R_{th} is measured between the port terminals with all the energy sources replaced by their internal resistance.



Where,

I_{SC} – Short circuit current at terminals A & B R_{th}– Thevenin's equivalent Resistance.

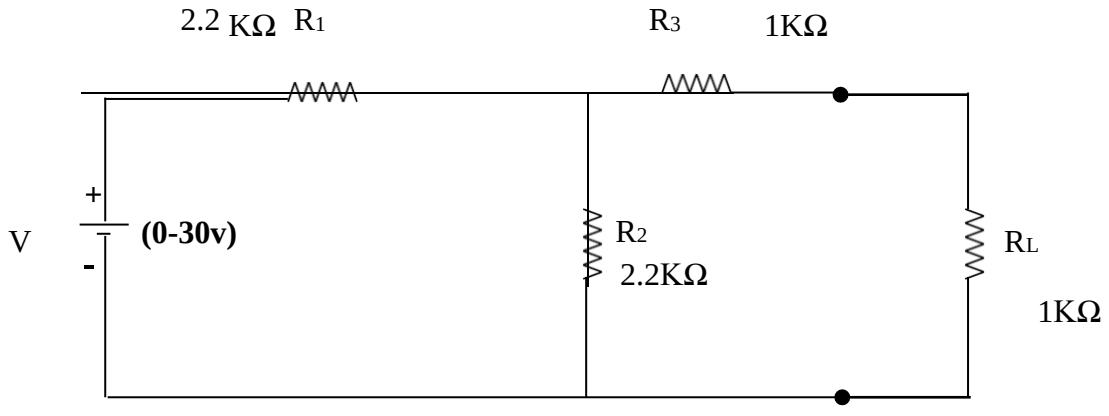
Apparatus Required:

S.No	Name	Range	Qty
1	R.P.S	(0-30) V	1
2	Ammeter	0 – 50mA	2
3	Voltmeter	0-25 V	2
4	Connecting wires		
5	Resistors	1K, 2.2K,4.7K,6.8K	Each 2
6	Breadboard		1

Procedure:

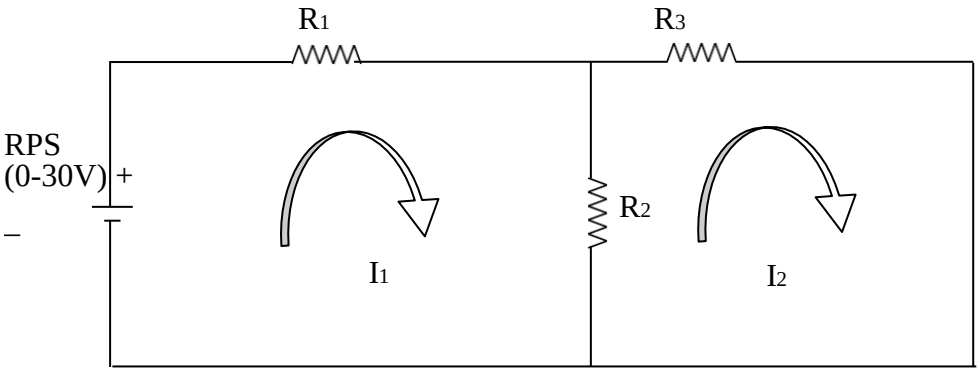
1. To find I_{SC}(short circuit the load resistance)
   a) Connections are made as per the circuit diagram.
   b) Note down the ammeter reading (I_{SC})
2. To find R_{th}(short circuit the voltage source)
   a) Connections are made as per the circuit diagrams
   b) Supply is switched 'ON'
   c) Vary the R.P.S to the specified voltage, note down the ammeter and voltmeter readings.
   d) Repeat the step 3 for various R.P.S voltage and the readings are tabulated.
   e) Calculate the R_{Th} using the tabulation.
3. To Find I_L
   a) Connections are given as per the circuit diagram.
   b) Switch ON the power supply.
   c) Vary the R.P.S. to the specified voltage and note down the ammeter reading (I_L).

Circuit diagram:



Theoretical Verification:

To Find I_{SC}:

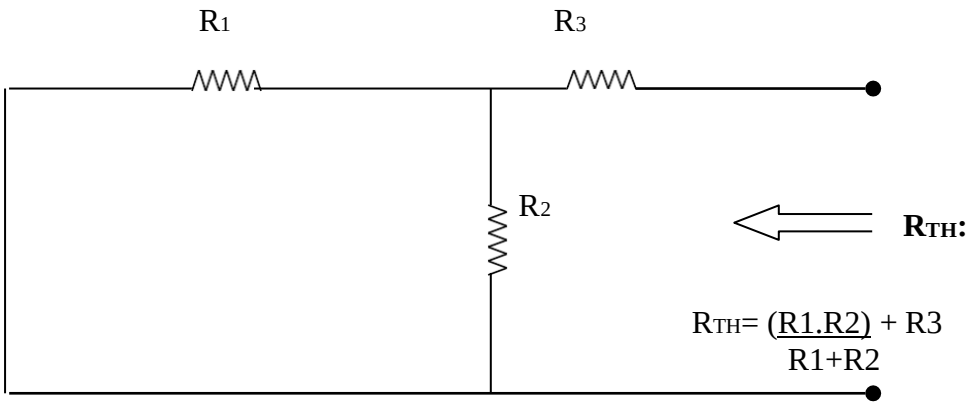


35

□1	$R_1 + R_2$	$- R_2$	$R_2 + R_3$
		$= - R_2$	
□2	$R_1 + R_2$	$- R_2$	0
		$= - R_2$	

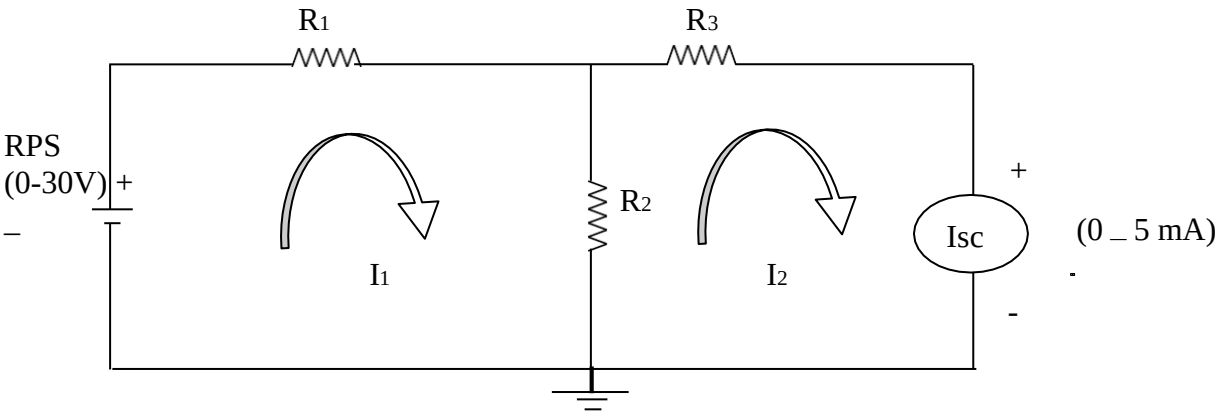
$I_{SC} = I_2 = □2 / □□$

To Find R_{TH}:

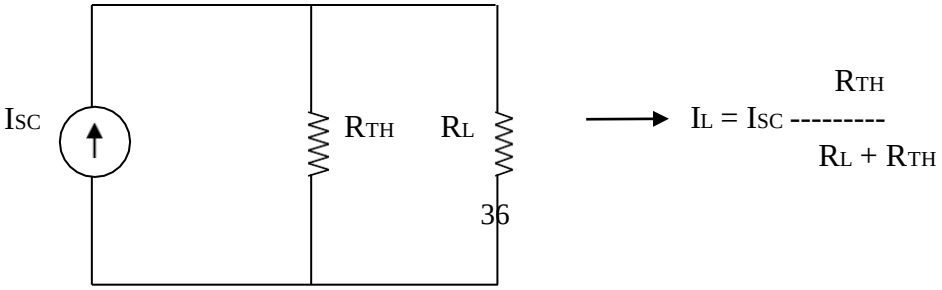


$R_{TH} = \frac{(R1.R2)}{R1+R2} + R3$

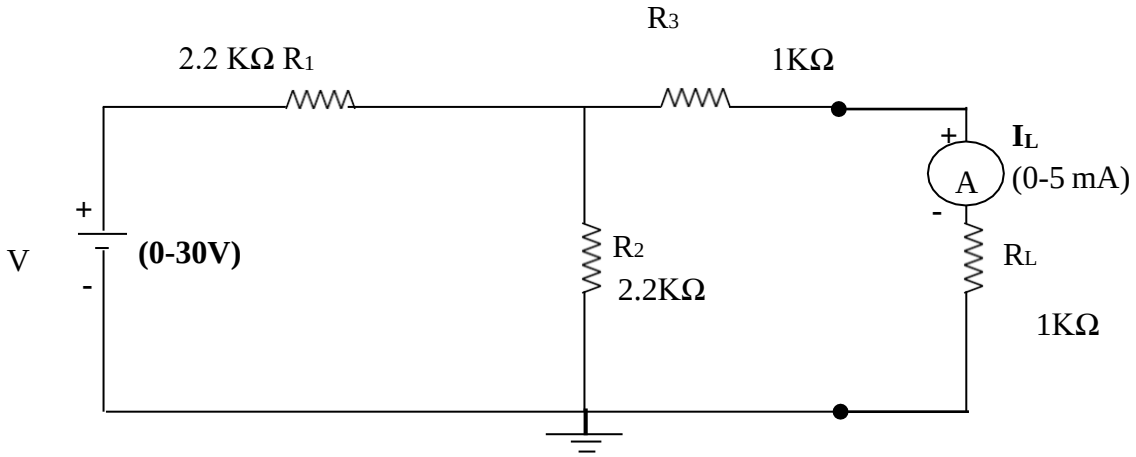
To Find Isc:



To Find I_L:



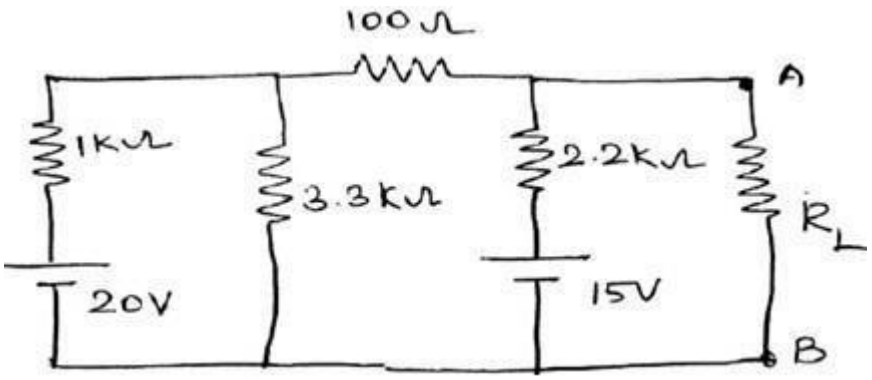
To Find I_L:



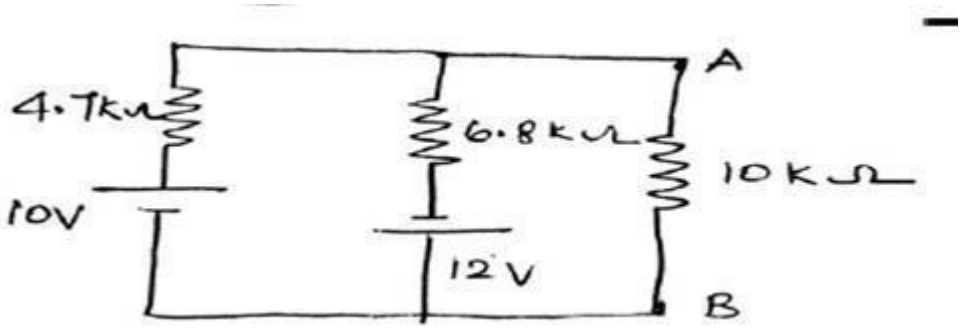
Tabulation:

S.No	Specified voltage (Volts)	Theoritical			Practical		
		Isc	Rth	IL	Isc	Rth	IL

CIRCUIT DIAGRAM: II



CIRCUIT DIAGRAM: III



PRE REQUISITE

1. How Rth is obtained in any circuit for applying Thevenin's and Norton's theorem?
2. What is Vth or Thevenin's voltage?
3. How Vth is obtained in any circuit for applying Thevenin's theorem?
4. What is IN or Norton's current?
5. How IN is obtained?

Review Questions:

1. State Thevenin's & Norton's theorem.
2. Draw the Thevenin's & Norton's equivalent circuit for 3. What is duality theorem?
4. Explain dependent sources and sources transformation.
5. Explain Star-Delta conversion

RESULT:

Thus the Thevenin's & Norton's theorems are verified.

Ex.No.9

VERIFICATION OF KIRCHOFFS CURRENT LAW AND KIRCHOFF'S VOLTAGE LAW.

Aim:

(a) To verify the Kirchoff's current law.
(b) To verify the Kirchoff's voltage law.

Statement:

Kirchhoff's Current Law:

The algebraic sum of all the currents at any junction in an electric circuit is zero. In other words, the sum of the current flowing towards a junction is equal to the sum of the currents flowing away from it.

Kirchhoff's Voltage Law:

In any closed circuit, the algebraic sum of all the electromotive forces and the potential drops is equal to zero. In other words, for any closed path in a network, the algebraic sum of voltages is zero.

(i.e) sum of voltage drops = sum of voltage rises.

Apparatus Required:

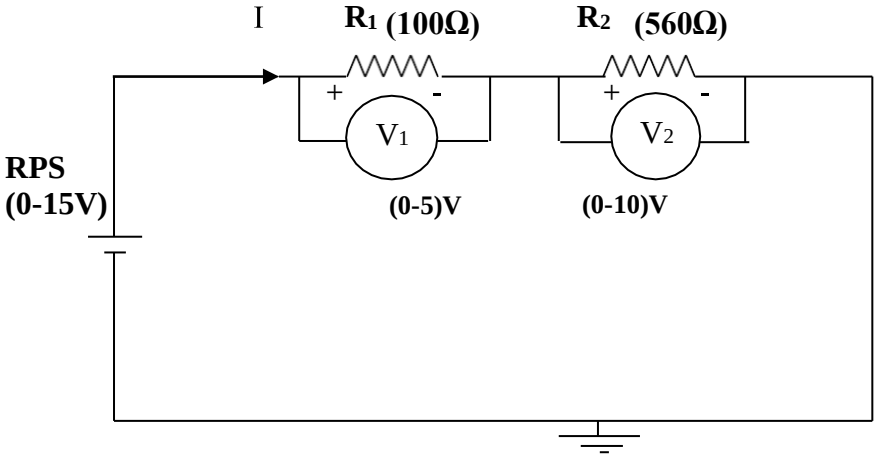
S.No	Name	Specification	Qty
1	R.P.S	(0-30V)	
2	Ammeter	0 – 50mA	1
3	Voltmeter	0 – 25V	1
4	Connecting wires		
5	Bread Board		
6	Resistors	100Ω, 560Ω, 470Ω, 2.2K,3.3K,4.7K	Each 2

PROCEDURE (Both KCL & KVL)

1. Connections are made as per the circuit diagram.
2. Switch on the power supply.

3. Vary the R.P.S to a specified voltage and note down the corresponding ammeter and voltmeter readings.
4. Repeat the step 3 for various R.P.S voltage and tabulate the readings.
5. Switch off the power supply and remove the connections.

Model circuit of KVL:



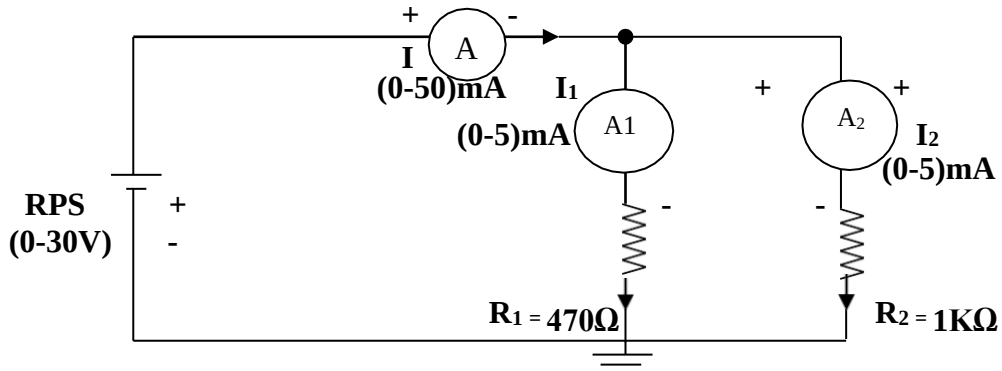
$V = IR_1 + IR_2$

$V = V_1 + V_2$

TABULATION:

S.No	Vs(Volts)	V1(Volts)	V2(Volts)	Vt=V1+V2(Volts)

Model Circuit of KCL:



$V = I_1R_1 = I_2R_2$

At the Junction A:

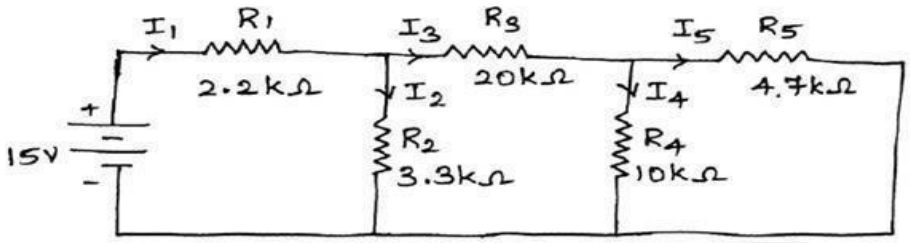
$I = I_1 + I_2$

TABULATION:

S.No	Vs(volts)	I(A)	I_1(A)	I_2(A)	$I = I_1 + I_2$(A)

Practical circuit Diagrams:

1. Forthecircuit shownin figure, computethe valueofcurrentsI1, I2, I3, I4, and I5 byusing KVLand KCL. Verifytheresults experimentally.



TABULATION:

KVL :

S.No	Vs(Volts)	V1(Volts)	V2(Volts)	V3(Volts)	V4(Volts)	V5(Volts)

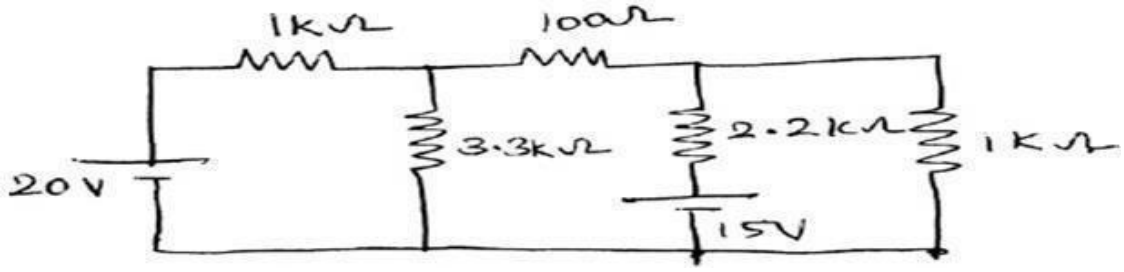
Loop1: 15 =V1+V2
Loop2: V2=V3+V4
Loop3: V3=V5

KCL:

S.No	Vs(Volts)	I_1(A)	I_2(A)	I_3(A)	I_4(A)	I_5(A)

I1= I2+I3
I3=I4+I5

2. .Forthecircuit given, findthevaluesofcurrentsI1, I2, and I3 using KVLand KCL.



TABULATION:

KVL:

S.No	Vs(Volts)	V1(Volts)	V2(Volts)	V3(Volts)	V4(Volts)	V5(Volts)

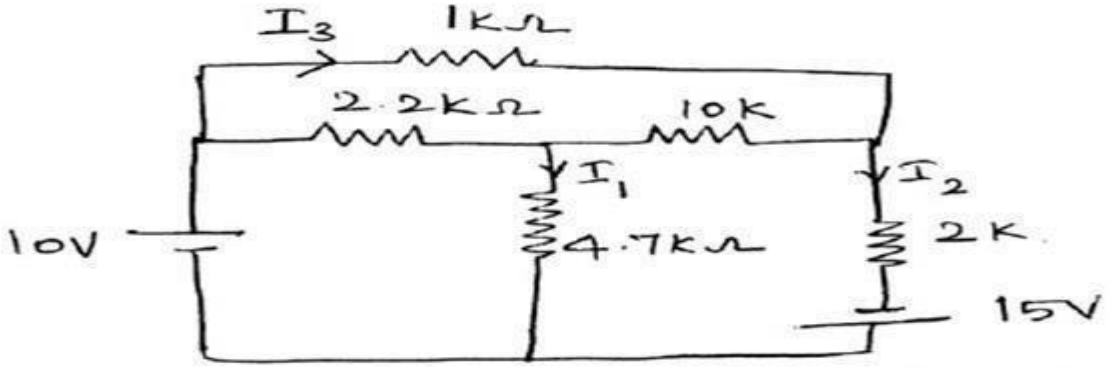
LOOP1:20=V1+V2; LOOP2: V2=V3+V4+15; LOOP3: 15+V4=V5

KCL:

S.No	Vs(Volts)	I_1(A)	I_2(A)	I_3(A)	I_4(A)	I_5(A)

$I_1=I_2+I_3$; $I_3=I_4+I_5$

3. .Forthecircuit shownin thefiguredeterminethevaluesofcurrentsI1, I2and I3using KVLand KCL



TABULATION:

S.No	Vs(Volts)	V1(Volts)	V2(Volts)	V3(Volts)	V4(Volts)	V5(Volts)

KVL:

Loop1:10=V1+V2; Loop2:V2=V3+V4-15; Loop:3 V5=V1+V3

S.No	Vs	I_1	I_2	I_3	I_4	I_5

Preparatory Questions

1. State KCL and KVL.
2. What is meant by short circuit and open circuit?
3. Two resistances with the value of R1, R2 are connected in i) series and ii) parallel. What is the equivalent resistance?
4. Two inductors with the value of L1, L2 are connected in i) series and ii) parallel. What is the equivalent inductance?
5. Two capacitors with the value of C1, C2 are connected in i) series and ii) parallel. What is the equivalent capacitance?

REVIEW QUESTIONS:

1. Define Resistance, Inductance and capacitance.
2. Color coding of resistor.
3. Define active and passive elements 4. Define Unilateral and Bilateral elements.
5. Define linear and Non-Linear elements.

RESULT:

Thus the Kirchoff's current law and Kirchoff's voltage law are verified.

Ex.No:10

VERIFICATION OF SUPERPOSITION THEOREM

Aim:

To verify the superposition theorem for the given electric circuit.

Statement:

In a linear lumped element, bilateral electric circuit energized by two or more sources, the current in any resistor is equal to the algebraic sum of the separate currents in each resistor when each source act, separately.

The Voltage sources are short-circuited and the current sources are open circuited in order to replace the other sources by their respective internal resistances.

Apparatus Required:

S.No	Name	Range	Qty
1	R.P.S	(0-30) V	1
2	Ammeter	0 -50 mA	1
3	Voltmeter	0 – 25 V	1
4	Connecting wires		
5	Resistors	10K, 22K,5.8K	Each 2
6	Breadboard		1

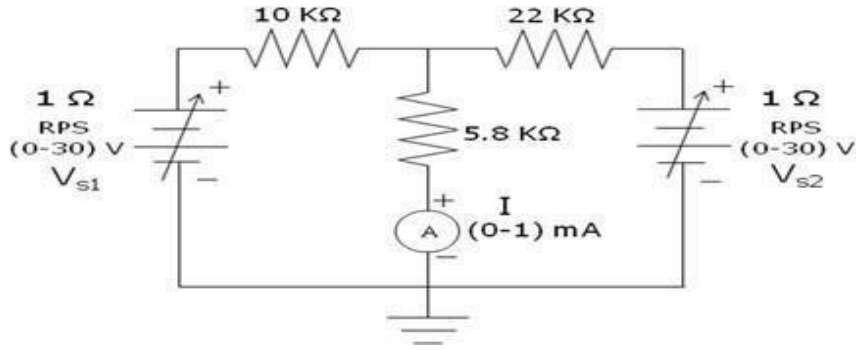
Procedure:

To Find I, I_1 & I_2:

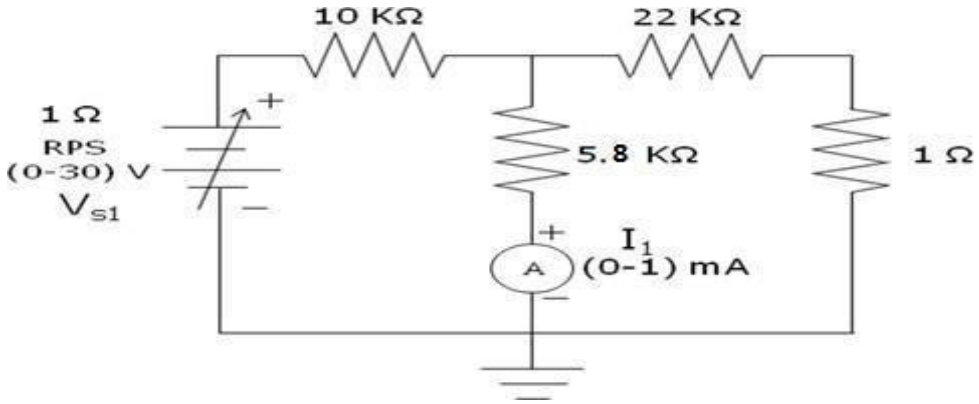
1. Connections are given as per the circuit diagram.
2. Switch on the power supply.

3. Vary the RPS to the given voltage and note down the ammeter readings for fig (1), fig (2) & fig (3).

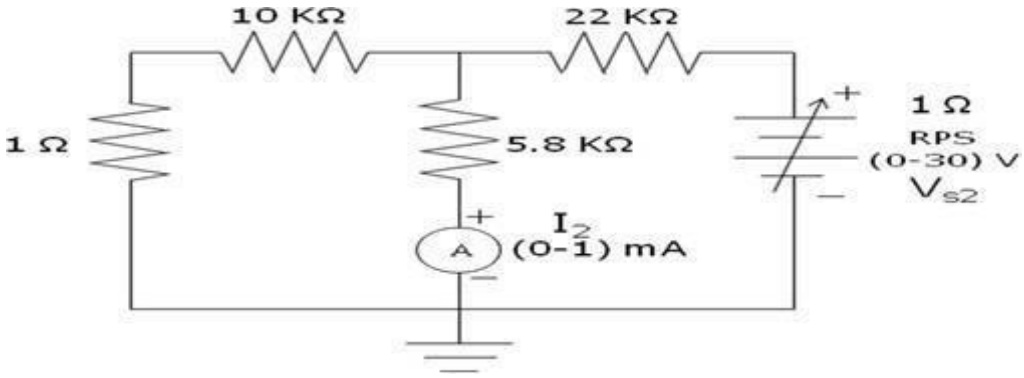
(a) When both V_{S1}& V_{S2} are active



(b) When V_{S1} acts alone



(c) When V_{S2} acts alone

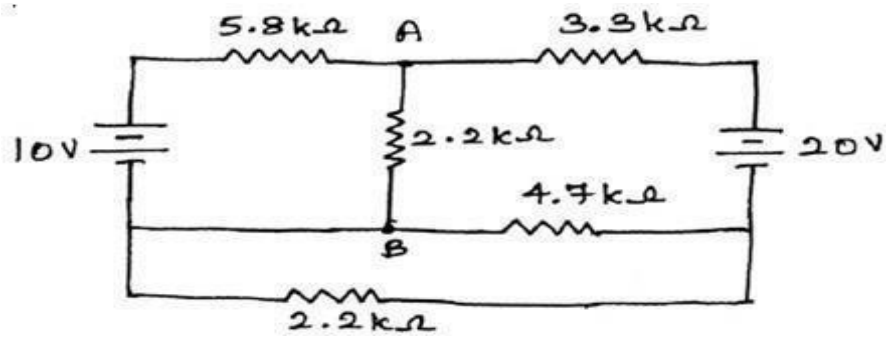


TABULAR COLUMN:

V_{S1} (volts)	V_{S2} (volts)	Theoritical				Practical			
		I (mA)	I_1 (mA)	I_2 (mA)	$I = I_1 + I_2$ (mA)	I (mA)	I_1 (mA)	I_2 (mA)	$I = I_1 + I_2$ (mA)

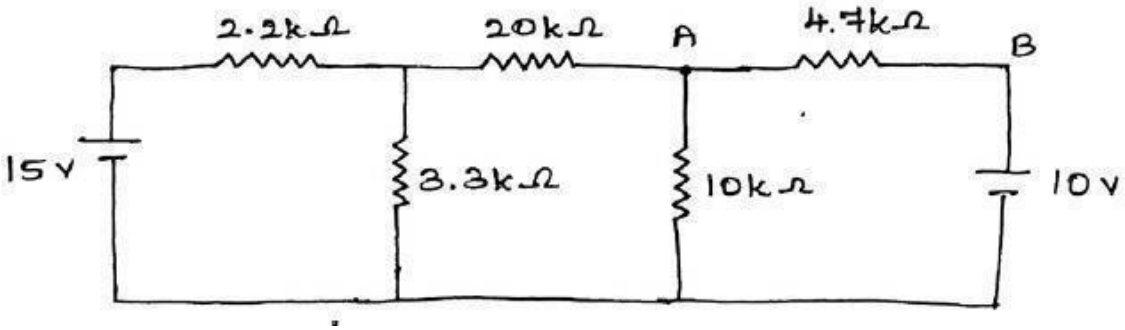
PRACTICALCIRCUITII:

Findthecurrent in the 2.2k Ω resistorbetweenA& B forthenetworkusingsuperpositiontheorem. Verify theresults experimental



PRACTICALCIRCUITIII:

Findthecurrent in the 4.7 k ΩresistorbetweenAand Bforthe networkusingsuperpositiontheorem.



PREREQUISITE

1. Define Lumped and distributed elements
2. Define ohm's law
3. What is the equivalent resistance for the resistor if it is connected in series and parallel
4. What is the equivalent Capacitance for the capacitor if it is connected in series and Parallel
5. What is the equivalent Inductance for the Inductor if it is connected in series and parallel

Review Questions:

1. State superposition theorem.
2. What is duality theorem?
3. Explain dependent sources and sources transformation.
4. Explain Star-Delta conversion
5. State voltage division rule & State current division rule.

Result:

Thus the superposition theorem is verified.

Ex.No:11

VERIFICATION OF MAXIMUM POWER TRASNFER AND RECIPROCITY THEOREM

Aim:

a. To practically verify the maximum power transfer theorem for the network with the theoretical value.

b. To practically verify the reciprocity theorem for the network with the theoretical calculation.

THEORY:

Maximum power transfer theorem:

This theorem states that maximum power will be delivered from a voltage source to a load when the load resistance is equal to the internal resistance of the source.

$$\text{Max. Power transferred} = \frac{V_{2th}}{4\,R_{th}}$$

Apparatus Required:

S.No	Name	Range	Qty
1	R.P.S	(0-30) V	1
2	Ammeter	0 – 50 mA	
3	Voltmeter	0 – 25V	
4	Connecting wires		
5	Resistors	1K, 2.2K,4.7K,6.8K	Each 2

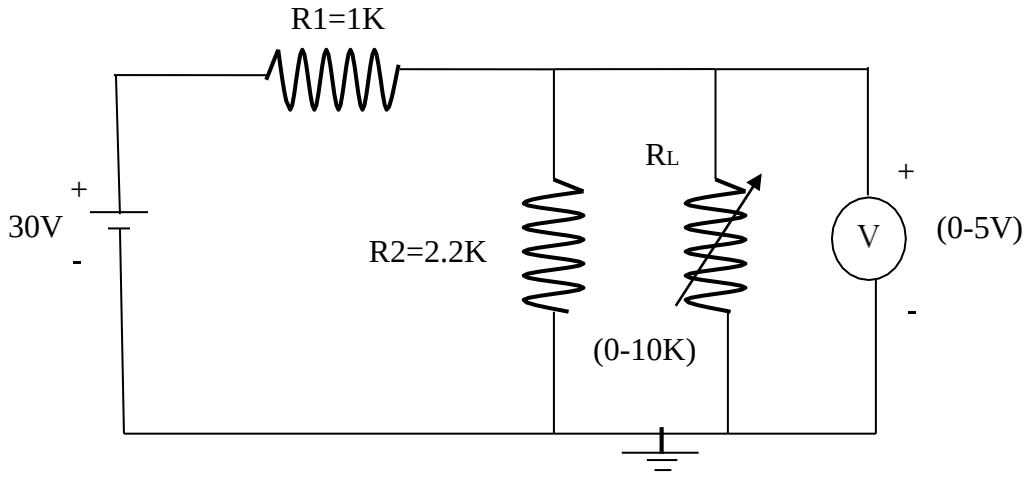
6	Breadboard		1

a. MAXIMUM POWER TRANSFER THEOREM:

PROCEDURE:

1. Remove the portion of network through which power has to be transferred.
2. Name those terminals as A and B.
3. Calculate R_{th} by substituting all sources with internal resistance working back at network
4. Give the connections as per the circuit diagram.
5. By varying the DRB (R_L) for values of R_L, measure the current through R_L.
6. Calculate the power delivered to R_L.
7. Verify resistance (R_L) at $P_{L\,(max)}$ is equal to R_{th}.

CIRCUIT DIAGRAM:



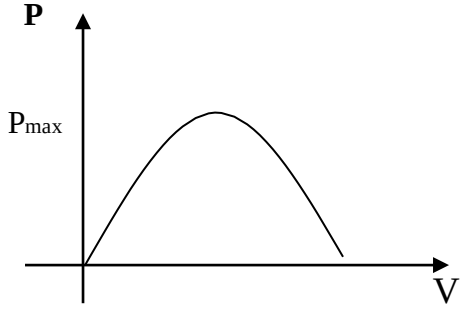
TABULATION

Experimental values:

P=V$_L$^{2}/4R$_{th}$

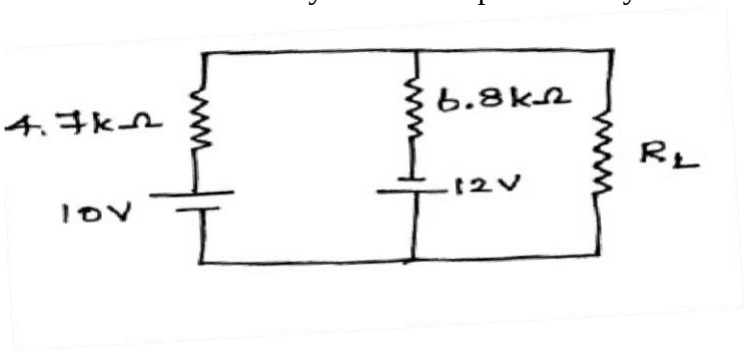
$R_L\Omega$	**V_{th}(v)**	**P_L (w)**

Model Graph:



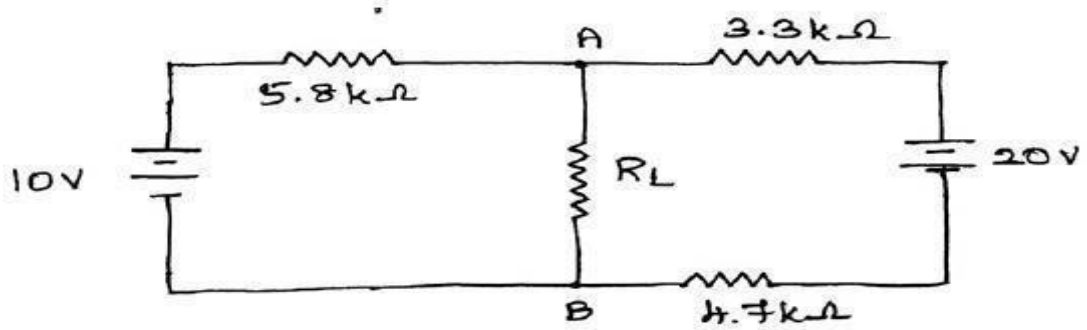
Practical circuit II:

DeterminethevalueofR$_L$ usingmaximumpowertransfertheoremandalso findthepowertransferredto the load. Verifytheresultsexperimentally.



Practical circuit III:

DeterminethevalueofRL usingmaximumpowertransfertheoremandalso findthepowertransferredto the load.



Reciprocity Theorem:

In any linear bilateral network the ratio of voltage to current response, in any element to the input is constant even when the position of the input and output areinterchanged.

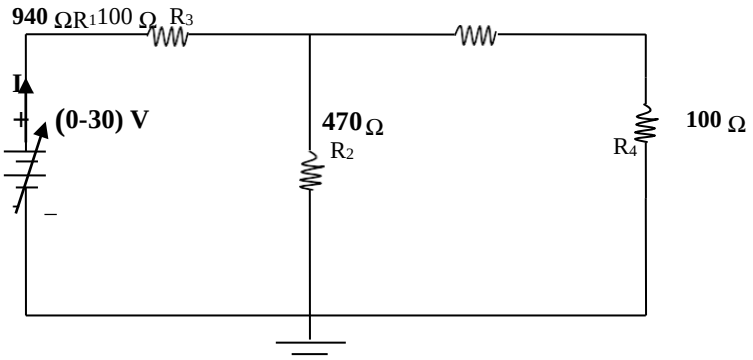
Apparatus Required:

S.No	Name	Range	Qty
1	R.P.S	(0-30) V	1
2	Ammeter	0 – 50 mA	1
3	Voltmeter	0 – 25V	1
4	Connecting wires		
5	Resistors	1K, 2.2K,4.7K,6.8K	Each 2
6	Breadboard		1

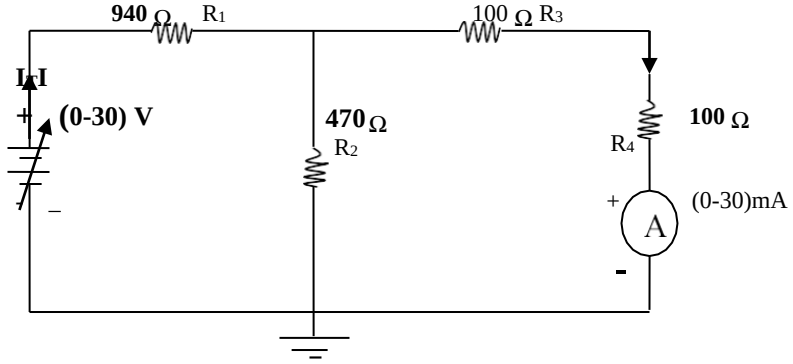
Procedure:

1. Connections are given as per the circuit diagram.
2. Note down the ammeter reading and find the ratio of the output current and input voltage.
3. Interchange the position of ammeter and the voltage source.
4. Note down the ammeter reading and find the ratio of the output and input voltage.
5. Compare this value with the value obtained in step 2.

CIRCUIT DIAGRAM: ORIGINAL NETWORKS



Circuit 1: To Measure the Load Current



$R_{eq} = (R_3+R_4)* R_2$

---------- $+ R_1$

$(R_3+R_4) + R_2$

$I_T = V/ R_{eq}$

$I = I_T * R_2$

$((R_3+R_4) + R_2)$

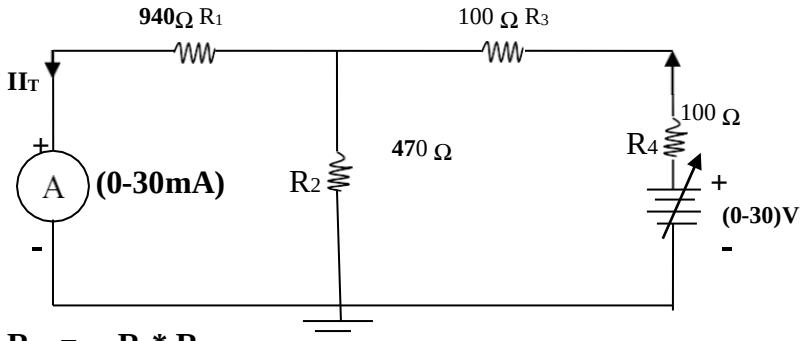
TABULATION

Experimental values: Theoretical values:

V (Volts)	I (mA)	Z = V/I
0		
2		
4		
6		

V (Volts)	I (mA)	Z = V/I
0		
2		
4		
6		

Circuit 2: After Interchanging Positions of V and I



$$R_{eq} = \frac{R_1 * R_2}{R_1+R_2} + R_3+R_4$$

$$I_T = V / R_{eq}$$

$$I = \frac{I_T * R_2}{R_1+R_2}$$

TABULATION

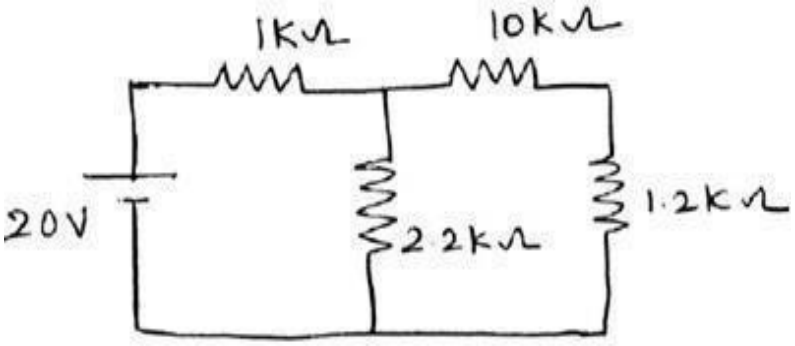
Experimental values: Theoretical Values

V (Volts)	I (mA)	Z = V/I
0		
2		
4		
6		

V (Volts)	I (mA)	Z = V/I
0		
2		
4		
6		

PRACTICAL CIRCUIT II:

Obtaincurrent flowingthroughthe 1.2 k Ωin thecircuit andverifythereciprocitytheorem.



PRE REQUISITE

1. Define duality
2. What is transient state?
3. What is transient time?
4. What is natural response?
5. What is transient response?

Review Questions:

1. State Maximum Power transfer theorem.
2. State reciprocity theorem?
3. What is duality theorem?
4. Explain dependent sources and sources transformation.
5. Explain Star-Delta conversion

RESULT:

Hence the maximum power transfer and reciprocity theorem for the given networks are practically verified.

Ex.No:12

FREQUENCY RESPONSE OF SERIES AND PARALLEL RESONANCE CIRCUITS

Aim:

To plot the current vs frequency graph of series and parallel resonance circuits and hence measure the bandwidth, resonant frequency.

Apparatus Required:

Sl. No	Name	Range	Qty
1.	Signal Generator	2MHz	1
2.	CRO	30MHz	1
3.	Connecting Wires		
4.	Resistors	1K, 470Ω,100Ω	1 each
5.	Capacitors	0.01uF, 0.1μf	2
6.	Inductors	99mH, 300mH	1
7.	Bread Board		1

Circuit Description For RLC Series Circuit:

A circuit is said to be in resonance when applied voltage V and current I are in phase with each other. Thus at resonance condition, the equivalent complex impedance of the circuit consists of only resistance (R). So current is maximum. Since V and I are in phase, the power factor is unity.

When the frequency is equal to complex impedance V

$= R + j (X_L – X_C)$

Where

$X_L = \square L$

$X_C = 1/\omega C$

Resonance Curve:

The curve between current and frequency is known as resonance curve. The shapes of such curve for of R as shown in fig(1). For smaller values of R, current Vs frequency wave is sharply peak, but for larger values of R, it is flat.

Bandwidth of a Resonance Circuit:

Bandwidth of a circuit is given by the band of frequencies which lies between two points on either side of resonance frequency, where current falls through 1/1.414 of the maximum value of resonance. Narrow is the bandwidth, higher the selectivity of the circuit. As shown in fig, the bandwidth AB is given by $F_2 – F_1$. F_1 is the lower cut off frequency and F_2 is the upper cut off frequency.

Q - Factor:

In the case of a RLC series circuit, it is defined as equal to the voltage magnification in the circuit at resonance. At resonance, current is maximum. $I_o = V/R$.

The applied voltage $V = I_oR$
Voltage magnification = $V_L/V = I_oX_L$

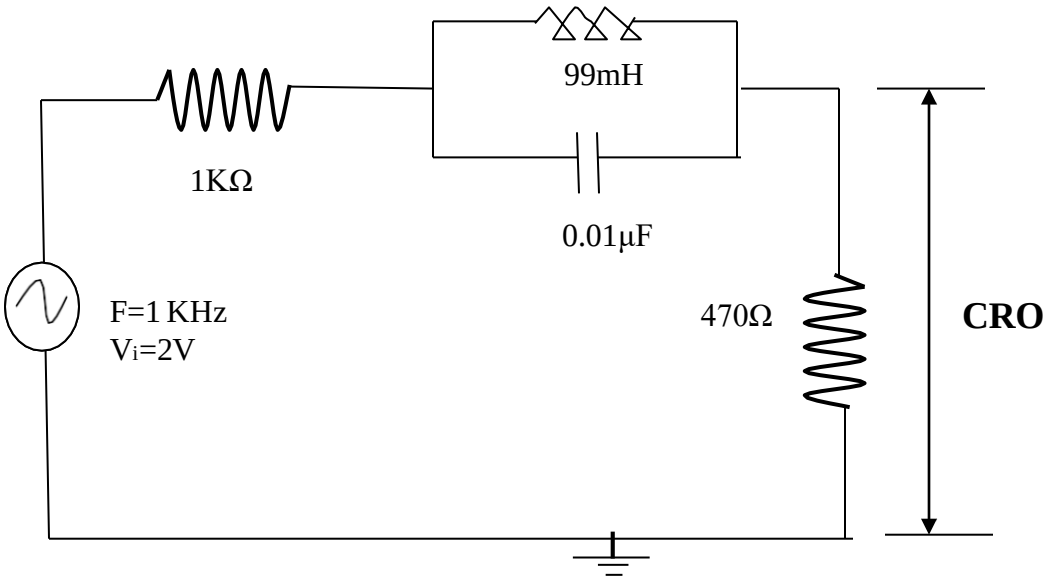
In the case of resonance, high Q factor means not only high voltage, but also higher sensitivity of tuning circuit. Q factor can be increased by having a coil of large inductance, not of smaller ohmic resistance.

$Q = \omega L / R$

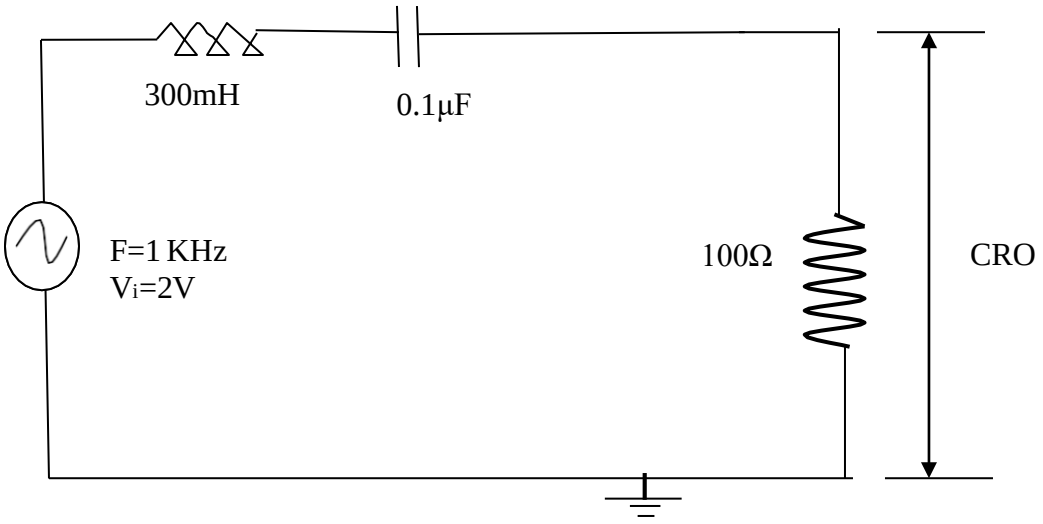
Procedure:

1. Connections are made as per the circuit diagram.
2. By varying the frequency and note down the corresponding meter reading.
3. Draw the current V_S frequency curve and measure the bandwidth, resonance frequency and Q factor.

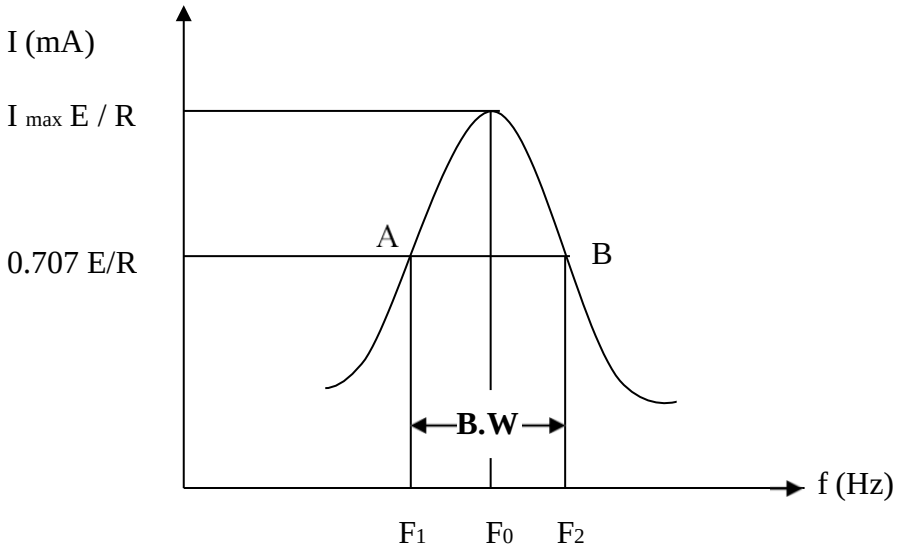
RLC Parallel Resonance Circuit:



RLC Series Resonance Circuit:

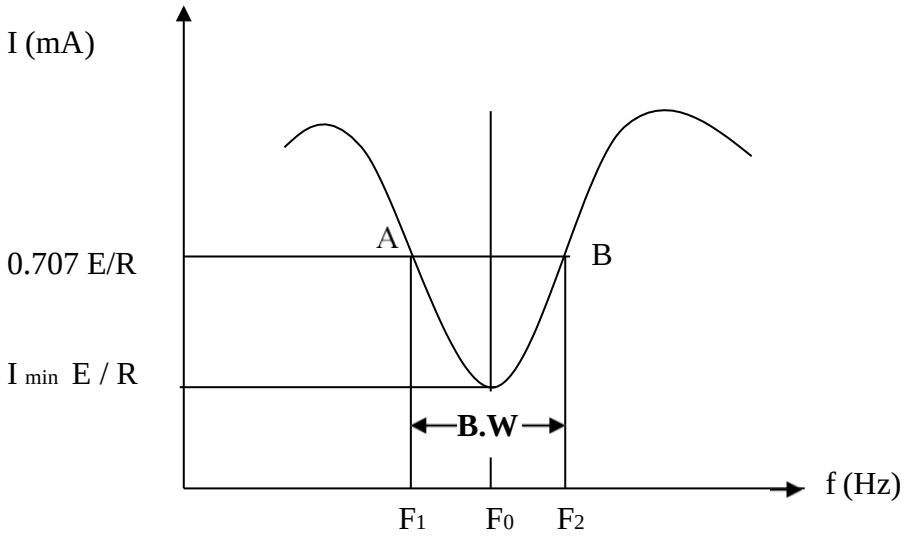


Series Resonance Curve:



Bandwidth B. W = $F_2 - F_1$
Resonant Frequency = F_0

Parallel Resonance Curve:



Tabulation:

Series circuit:

Input Voltage: V

Parallel circuit:

Input Voltage: V

S.No	Frequency (Hertz)	Output Voltage (V)	Current (mA)

S.No	Frequency (Hertz)	Output Voltage (V)	Current (mA)

PRE REQUISITE

1. What is a parallel resonant circuit?
2. What is a series resonant circuit?
3. What are tuned circuits?
4. When the circuit is said to be in resonance?
5. What is resonant frequency?

Review Questions:

1. Explain series resonance.
2. Define Q factor.
3. What is coefficient of coupling?
4. What is transient response?
5. Briefly explain the series & parallel connection of independent source.

Result:

Thus the frequency curve of series and parallel circuits are drawn.

Ex.No:13

TRANSIENT ANALYSIS OF RL & RC CIRCUITS

AIM: To construct and verify the output waveforms of differentiator and integrator circuit

APPARATUS REQUIRED:

S.No	COMPONENTS	RANGE	QUANTITY
1	Resistor	10kΩ	1
2	Capacitor	0.01μF	1
3	AFG	(0-1)MHz	1
4	CRO	(0 – 30)MHz	1
5	Bread Board		1

THEORY:

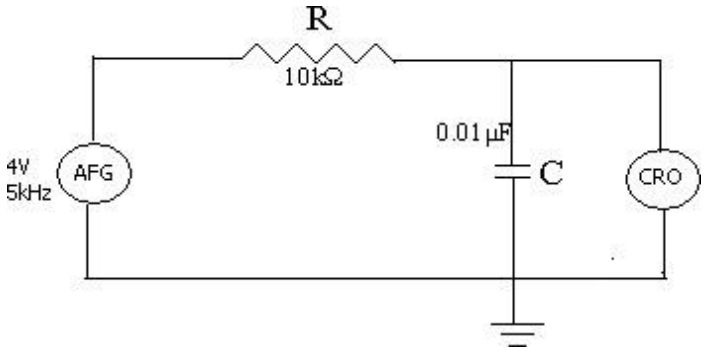
The RC linear network used for wave shaping circuit based on input frequency is divided as High Pass Filter and Low Pass Filter. The High pass filter acts as differentiator when the time constant is very low. The Low pass filter circuit with a very high time constant acts as an integrator.

PROCEDURE:

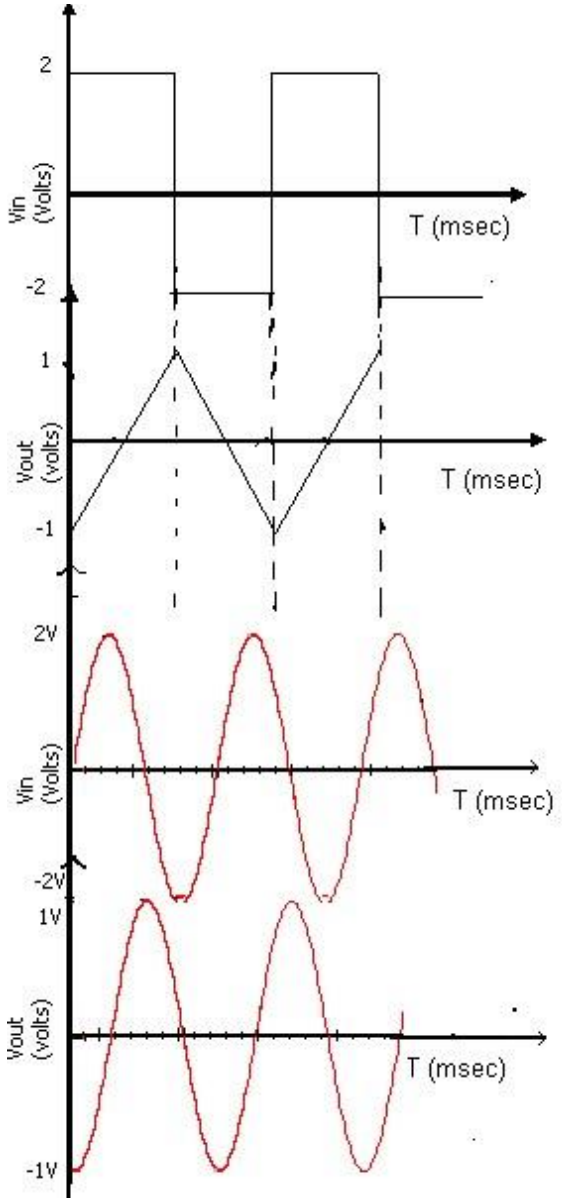
1. Connect the components and apparatus as shown in the circuit diagram.
2. For ***Differentiator*** set sinusoidal input of 4 volts and 200Hz and verify the output using CRO. Repeat it with square waveform as an input.
3. For ***Integrator*** set sinusoidal input of 4 volts and 5 kHz and verify the output using CRO. Repeat it with square waveform as an input. 4. Plot the input and output waveform for differentiator and integrator in linear graph.

CIRCUIT DIAGRAM

INTEGRATOR

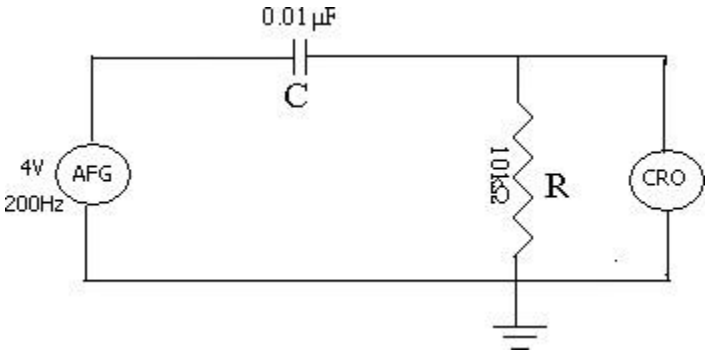


MODEL GRAPH

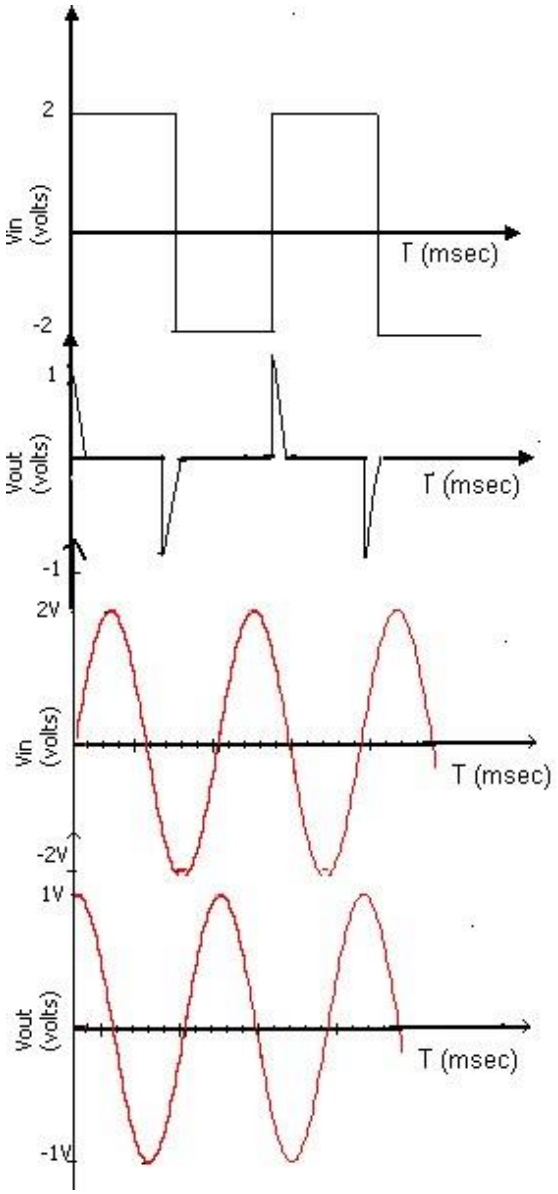


CIRCUIT DIAGRAM

DIFFERENTIATOR



MODEL GRAPH



PRE REQUISITE

1. Give the expression for quality factor of series RLC Circuit.
2. Give the expression for quality factor of parallel RLC Circuit.

3. What is the formula to find the power factor in a three phase circuits.
4. What is the formula to find the reactive power in three phase circuits?
5. What is the advantage of using three phase rather than using three single phase circuits?

REVIEW QUESTIONS:

1. How high pass RC circuit is used as a differentiator?
2. How low pass RC circuit is used as an integrator?
3. What should be the input for an integrator circuit to obtain the ramp signal in the output?
4. What will be time constant of an integrator to obtain saw tooth waveform in the output?
5. What is the formula to verify the output of an integrator and a differentiator circuit?

RESULT:

Thus the integrator and the differentiator circuit operation are verified for the square and sine wave input.