SRI SHANMUGHA COLLEGE OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Communication Engineering

EC8361 – ANALOG AND DIGITAL CIRCUITS LAB MANUAL

COURSE OBJECTIVES

- To study the Frequency response of CE, CB and CC Amplifier
- To learn the frequency response of CS Amplifiers
- To study the Transfer characteristics of differential amplifier
- To perform experiment to obtain the bandwidth of single stage and multistage amplifiers
- To perform SPICE simulation of Electronic Circuits
- To design and implement the Combinational and sequential logic circuits

LIST OF ANALOG EXPERIMENTS:

1. Design of Regulated Power supplies
2. Frequency Response of CE, CB, CC and CS amplifiers
3. Darlington Amplifier
4. Differential Amplifiers - Transfer characteristics, CMRR Measurement
5. Cascode and Cascade amplifiers
6. Determination of bandwidth of single stage and multistage amplifiers
7. Analysis of BJT with Fixed bias and Voltage divider bias using Spice
8. Analysis of FET, MOSFET with fixed bias, self-bias and voltage divider bias using simulation software like Spice
9. Analysis of Cascode and Cascade amplifiers using Spice
10. Analysis of Frequency Response of BJT and FET using Spice

LIST OF DIGITAL EXPERIMENTS

1. Design and implementation of code converters using logic gates
   (i) BCD to excess-3 code and vice versa
   (ii) Binary to gray and vice-versa
2. Design and implementation of 4 bit binary Adder/ Subtractor and BCD adder using IC 7483
3. Design and implementation of Multiplexer and De-multiplexer using logic gates
4. Design and implementation of encoder and decoder using logic gates
5. Construction and verification of 4 bit ripple counter and Mod-10 / Mod-12 Ripple counters
6. Design and implementation of 3-bit synchronous up/down counter

COURSE OUTCOMES

- Differentiate cascode and cascade amplifier.
- Analyze the limitation in bandwidth of single stage and multi stage amplifier
- Simulate amplifiers using PSpice
- Measure CMRR in differential amplifier

Expt. No. 1 COMMON EMITTER AMPLIFIER

Aim:

To construct a Common Emitter amplifier circuit and plot the frequency response

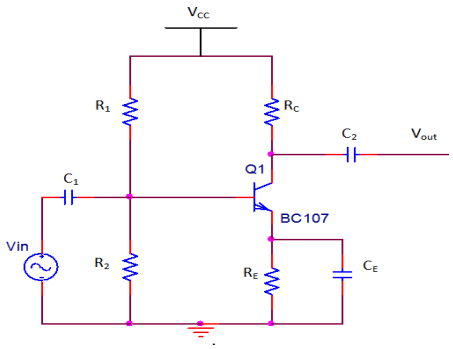
Apparatus Required:

S. No.	Apparatus	Range	Quantity
1	Transistor	BC107	1
2	Resistor	As per design	4
3	Capacitor	As per design	3
4	Power Supply	(0 - 30)V	1
5	Function Generator	(0 - 3)MHz	1
6	CRO	(0 - 30)MHz	1
7	Bread Board	-	1
8	Connecting wires	-	few

Theory:

The CE amplifier provides high gain and wide frequency response. The emitter lead is common to both input & output circuits and is grounded. The emitter-base circuit is forward biased. The collector current is controlled by the base current rather than the emitter current. The input signal is applied to base terminal of the transistor and amplifier output is taken across the collector terminal. A very small change in base current produces a much larger change in collector current. When positive half-cycle is fed to the input circuit, it opposes the forward bias of the circuit which causes the collector current to decrease, it decreases the voltage further more negative. Thus when input cycle varies through a negative half-cycle, it increases the forward bias of the circuit, which causes the collector current to increases thus the output signal in common emitter amplifier is out of phase with the input signal.

Circuit Diagram:



Design:

Given:

V_{cc} = 10 V; I_c = 10mA

To find V_E:

$V_E = \frac{V_{CC}}{10}$ =

To find R_E:

$R_E = \frac{V_E}{I_E}$ =

Find β from given transistor.

To find R_2:

Condition to be3 satisfied: $R_2 \leq 0.1\beta R_E$

R_2 =

To find V_{BE}:

$V_{BE} = V_B - V_E$

$V_B = V_{BE} + V_E$

V_{BE} =

To find R_1:

$$R_1 = \frac{R_2 V_{CC}}{V_B} - R_2$$

R_1 =

To find R_C:

$V_{CC} = I_C R_C + V_{CE} + I_E R_E$

$$\frac{V_{CC} - V_{CE} - I_E R_E}{I_C} = R_C$$

R_c =

Procedure:

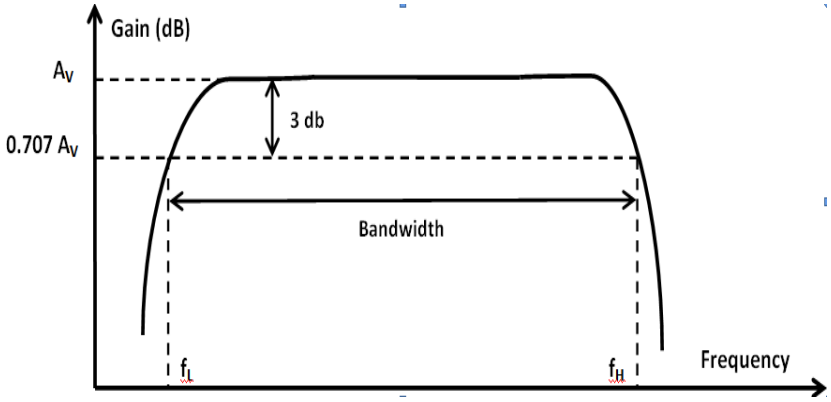
1. Connect the circuit as per the circuit diagram.
2. Set the input voltage to a constant value.
3. Vary the input frequency 0 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph (Gain (dB) Vs Frequency (Hz)).

Tabulation:

Input voltage, V_{in} (V) =

Frequency (Hz)	Output Voltage (volts) V_o	Gain= 20 log(V_o/V_{in}) (dB)

Model Graph:



Bandwidth Calculation:

f_L (Hz) =

f_H (Hz) =

Bandwidth (Hz) = f_H - f_L

Bandwidth (Hz) =

Result:

Thus the common emitter amplifier circuit has been designed and the frequency response is obtained.

Outcome:

Able to design and construct a common emitter amplifier circuit and determine the frequency response of the amplifier.

Practical Applications

1. Common-emitter amplifiers are used as Low frequency voltage amplifier.
2. Common-emitter amplifiers are also used in radio frequency transceiver circuits. (Radio)
3. Common emitter configuration commonly used in low-noise amplifiers.
4. Common emitter amplifiers have both voltage and current gain, hence they are used as driving stages of many audio amplifiers. It can amplify headphone audio, condenser mic audio.
5. Common emitter amplifiers are also used in output drive stages of a large LED circuit or in a circuit with multiple loads like LED, Buzzer, Resistor, coils, etc.

Viva – voce

1. What is an Amplifier?
2. What is meant by Self Bias & fixed Bias circuits, which one is preferred and why?
3. What is quiescent point? What are the various parameters of the transistor that cause drift in Q-point?
4. What is meant Band width, Lower cut-off and Upper cut-off frequency?
5. How the junctions of Transistor are biased in ON state and OFF state?
6. What is meant by single stage amplifier?
7. Who invented the transistor?
8. What is meant by thermal runaway?
9. For faithful amplification, in what region the transistor operates?
10. What is the need for biasing?
11. List out the types of biasing methods in BJT.
12. List out the advantages of common emitter amplifier.
13. What is the function of input capacitor C_{in} ?
14. What is the function of output capacitor C_{out}?
15. What is meant by d.c. load line?
16. Define - Operating Point
17. What will happen to the output signal if the operating point locates nearer to the cut-off region?
18. What will happen to the output signal if the operating point locates nearer to the saturation region?
19. What is meant by a.c. load line?
20. What is meant by Beta?
21. Give the relationship between Alpha and Beta.
22. What is the phase difference between the output and input voltages of a CE amplifier?
23. What is the purpose of capacitors in a transistor amplifier?
24. To obtain highest power gain, which transistor configuration is used?
25. What is the other name CE amplifier?

Expt. No. 2 COMMON COLLECTOR AMPLIFIER

Aim:

To construct a common collector amplifier circuit and plot the frequency response

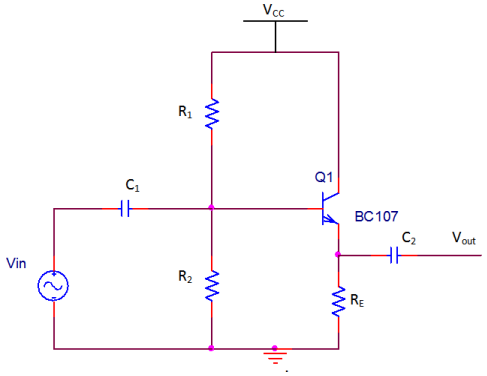
Apparatus Required:

S. No.	Apparatus	Range	Quantity
1	Transistor	BC107	1
2	Resistor	As per design	3
3	Capacitor	As per design	2
4	Power Supply	(0 - 30)V	1
5	Function Generator	(0 - 3)MHz	1
6	CRO	(0 - 30)MHz	1
7	Bread Board	-	1
8	Connecting wires	-	few

Theory:

In common-collector amplifier, the input is given at the base and the output is taken at the emitter. In this amplifier, there is no phase inversion between input and output. The input impedance of the CC amplifier is very high and output impedance is low. The voltage gain is less than unity. Here the collector is at ac ground and the capacitors used must have a negligible reactance at the frequency of operation. This amplifier is used for impedance matching and as a buffer amplifier. This circuit is also known as an emitter follower.

Circuit Diagram:



Design:

Given:

V_{cc} = 15 V; I_c = 10mA

To find V_E:

$V_E = I_E R_E$

$$I_E \cong I_C$$

V_E =

To find R_E:

$R_E = \frac{V_{CC} - V_{CE}}{I_C}$ =

R_E =

Find β from given transistor.

To find R_2:

Condition to be3 satisfied: $R_2 \leq 0.1\beta R_E$

R_2 =

To find V_B:

$V_{BE} = V_B - V_E$

$V_B = V_{BE} + V_E$

V_B =

To find R_1:

$$R_1 = \frac{V_{CC} - V_B}{V_B} \times R_2$$

R_1 =

Procedure:

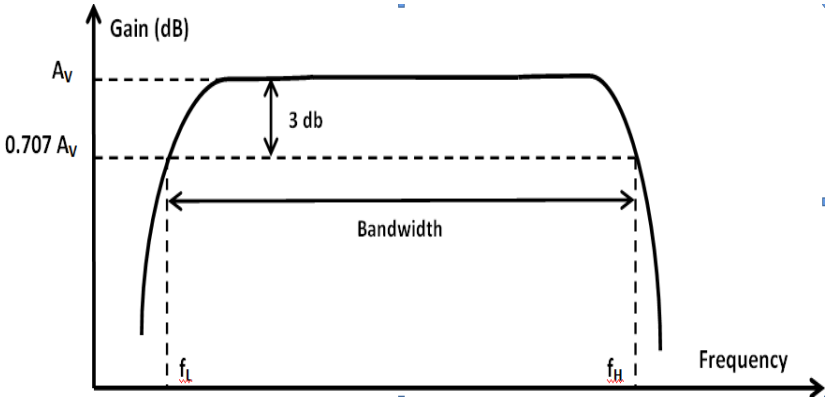
1. Connect the circuit as per the circuit diagram.
2. Set the input voltage to a constant value. (eg: 20 mV).
3. Vary the input frequency 0 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph (Gain (dB) Vs Frequency (Hz)).

Tabulation:

Input voltage, V_{in} (V) =

Frequency (Hz)	Output Voltage (volts) V_o	Gain= 20 log(V_o/V_{in}) (dB)

Model Graph:



Bandwidth Calculation:

f_L (Hz) =

f_H (Hz) =

Bandwidth (Hz) = f_H - f_L

Bandwidth (Hz) =

Result:

Thus the common collector amplifier circuit has been designed and the frequency response is obtained.

Outcome:

Able to design and construct a common collector amplifier circuit and determine the frequency response of the amplifier.

Practical Applications

1. Common-emitter amplifiers are used as audio amplifier and audio tuners
2. These configurations are widely used in impedance matching applications because of their high input impedance.
3. It is used as a switching circuit.
4. The high current gain combined with near unity voltage gain makes this circuit a great voltage buffer
5. It is also used for circuit isolation.

Viva – voce

1. What is the other name for CC Amplifier?
2. What are the uses of CC Amplifier?
3. Why this amplifier has got the name Emitter Follower?
4. What is the maximum Voltage gain of an Emitter Follower?
5. Why it is used as a Buffer amplifier?
6. What is the input resistance of common collector amplifier?
7. What is the output resistance of common collector amplifier?
8. In common collector amplifier, the input signal is applied to which terminal?
9. What is the current amplification factor for common collector amplifier?
10. To draw a d.c. equivalent circuit of a transistor amplifier, how capacitors are considered?
11. What is the purpose of coupling capacitor in a transistor amplifier?
12. If a transistor amplifier feeds a load (ex. Speaker)of low resistance, then what should be the value of the voltage gain?
13. What is the significance of operating point?
14. What is the importance of load line analysis?
15. Why does a.c. load line differ from d.c. load line?
16. Does phase reversal affect amplification?
17. What type of capacitors is used in transistor amplifier?
18. What will happen to the transistor amplifier if the input capacitor is short circuited?
19. Why the transistor amplifier has high output impedance?
20. Why common collector configuration is used for impedance matching?
21. List out the different types of biasing.
22. Define - Thermal runway

23. What is the range β of a BJT?
24. What are the input and output impedances of CC configuration?
25. Define current gain in CC configuration?
26. Why CE configuration is preferred for amplification?

Expt. No. 3 COMMON BASE AMPLIFIER

Aim:

To construct a common base amplifier circuit and plot the frequency response

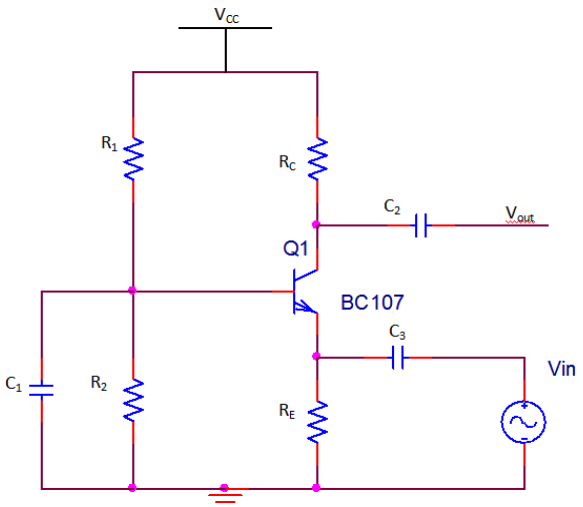
Apparatus Required:

S. No.	Apparatus	Range	Quantity
1	Transistor	BC107	1
2	Resistor	As per design	4
3	Capacitor	As per design	3
4	Power Supply	(0 - 30)V	1
5	Function Generator	(0 - 3)MHz	1
6	CRO	(0 - 30)MHz	1
7	Bread Board	-	1
8	Connecting wires	-	few

Theory:

In the common-base configuration, the input signal is applied to the emitter, the output is taken from the collector, and the base is the element common to both input and output. The common-base configuration has a low input resistance and a high output resistance. However, two factors limit its usefulness in some circuit applications: (1) its low input resistance and (2) its current gain of less than 1. Since the CB configuration will give voltage amplification, there are some additional applications, which require both a low-input resistance and voltage amplification that could use a circuit configuration of this type.

Circuit Diagram:



Design:

Given

V_{cc} = 15 V; I_c = 10mA

To findV_{CE}:

$V_{CE} = \frac{V_{cc}}{2}$ =

V_{CE} =

To find R_E:

$R_E = \frac{V_E}{I_E}$ =

R_E =

Find β from given transistor.

To find R_2:

$R_2 \leq 0.1\beta R_E$

R_2 =

To find V_B:

$V_{BE} = V_B - V_E$

$V_B = V_{BE} + V_E$

V_B =

To find R_1:

$$R_1 = \frac{R_2 V_{CC}}{V_B} - R_2$$

R_1 =

To find R_C:

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$\frac{V_{CC} - V_{CE} - I_E R_E}{I_C} = R_C$$

R_c =

Procedure:

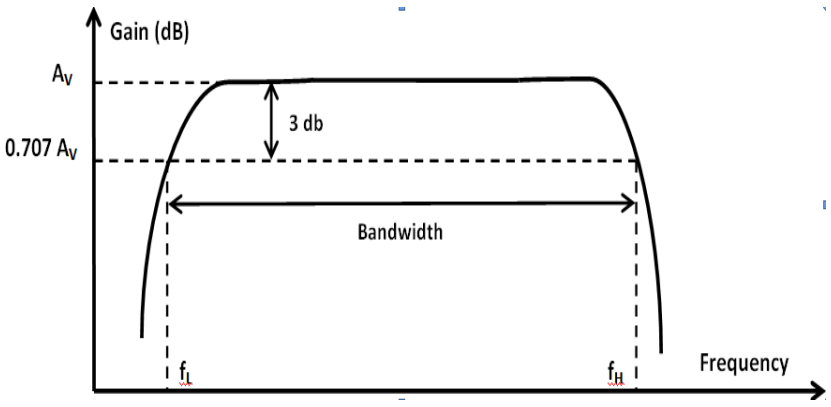
1. Connect the circuit as per the circuit diagram.
2. Set the input voltage to a constant value. (eg: 20 mV).
3. Vary the input frequency 0 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph (Gain (dB) Vs Frequency (Hz)).

Tabulation:

Input voltage, V_{in} (V) =

Frequency (Hz)	Output Voltage (volts) V_o	Gain= 20 log(V_o/V_{in}) (dB)

Model Graph:



Bandwidth Calculation:

f_L (Hz) =

f_H (Hz) =

Bandwidth (Hz) = $f_H - f_L$

Bandwidth (Hz) =

Result:

Thus the common base amplifier circuit has been designed and the frequency response is obtained.

Outcome:

Able to design and construct a common base amplifier circuit and determine the frequency response of the amplifier.

Practical Applications

1. Common base amplifier is used in moving coil microphone preamplifiers. These microphones have very low impedance levels.
2. It is used in UHF and VHF RF amplifiers.
3. It is mainly used at high frequencies where low source resistance is common.
4. It is used for impedance matching in circuits with very low output resistances to those with a high input resistance.

Viva – voce

1. What is the significance of Emitter Resistance?
2. If bypass capacitor is removed, what happens to the gain?
3. What is the current gain in C.B. Amplifier?
4. What is the "cut - in" voltage of a silicon-small signal transistor?
5. What is the "cut - in" voltage of a germanium-small signal transistor?
6. When will the transistor is said to be in saturation region?
7. When will the transistor is said to be in cut-off region?
8. What is the current amplification factor for common base configuration?

9. What is the input resistance of common base amplifier?
10. What is the output resistance of common collector amplifier?
11. In common base amplifier, the input signal is applied to which terminal?
12. List out the applications of common base amplifiers.
13. What will happen to the transistor if it is not properly biased?
14. Why voltage divider biasing is commonly used in amplifiers?
15. What is meant by bias compensation?
16. What is meant by bias stabilization?
17. Which type of BJT configurations has the lowest output impedance?
18. Why common collector circuit is known as an emitter follower?
19. In which direction the current I_{CBO} flows?

Expt. No. 4 COMMON SOURCE AMPLIFIER

Aim:

To construct a common source amplifier circuit and plot the frequency response

Apparatus Required:

S. No.	Apparatus	Range	Quantity
1	JFET	BFW10	1
2	Resistor	As per design	4
3	Capacitor	As per design	3
4	Power Supply	(0 - 30)V	1
5	Function Generator	(0 - 3)MHz	1
6	CRO	(0 - 30)MHz	1
7	Bread Board	-	1
8	Connecting wires	-	few

Theory:

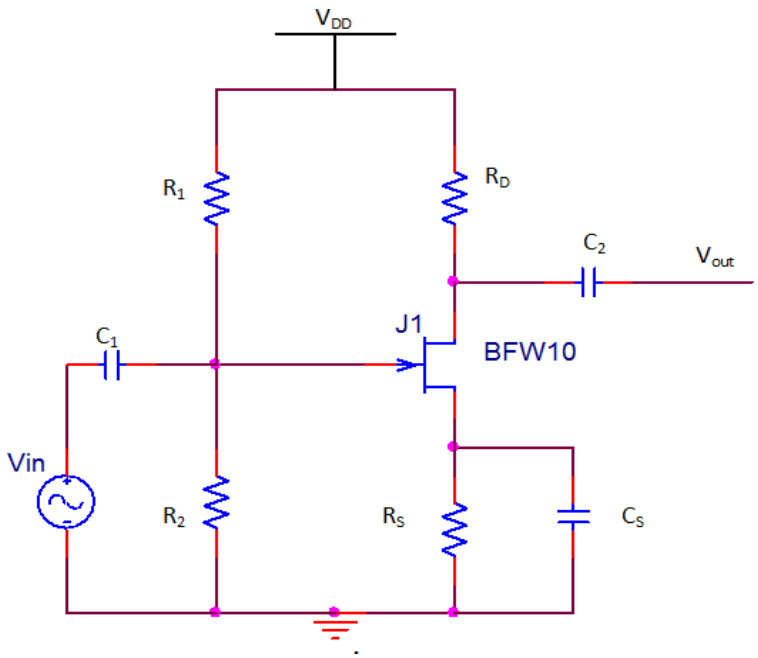
A field-effect transistor (FET) is a type of transistor commonly used for weak-signal amplification. The device can amplify analog or digital signals. It can also switch DC or function as an oscillator. In the FET, current flows along a semiconductor path called the channel. At one end of the channel, there is an electrode called the source. At the other end of the channel, there is an electrode called the drain. The physical diameter of the channel is fixed, but its effective electrical diameter can be varied by the application of a voltage to a control electrode called the gate. Field-effect transistors exist in two major classifications. These are known as the junction FET (JFET) and the Metal Oxide Semiconductor FET(MOSFET). The junction FET has a channel consisting of N-type semiconductor (N-channel) or P-type semiconductor (P-channel) material; the gate is made of the opposite semiconductor type.

In P-type material, electric charges are carried mainly in the form of electron deficiencies called holes. In N-type material, the charge carriers are primarily electrons. In a JFET, the junction is the boundary between the channel and the gate. Normally, this P-N junction is reverse-biased (a DC voltage is applied to it) so that no current flows between the channel and the gate. However, under some conditions there is a small current

through the junction during part of the input signal cycle. The FET has some advantages and some disadvantages relative to the bipolar transistor. Field-effect transistors are preferred for weak-signal work, for example in wireless, communications and broadcast receivers. They are also preferred in circuits and systems requiring high impedance. The FET is not, in general, used for high-power amplification, such as is required in large wireless communications and broadcast transmitters.

Field-Effect Transistors are fabricated onto silicon Integrated Circuit (IC) chips. A single IC can contain many thousands of FETs, along with other components such as resistors, capacitors, and diodes.

Circuit Diagram:



Procedure:

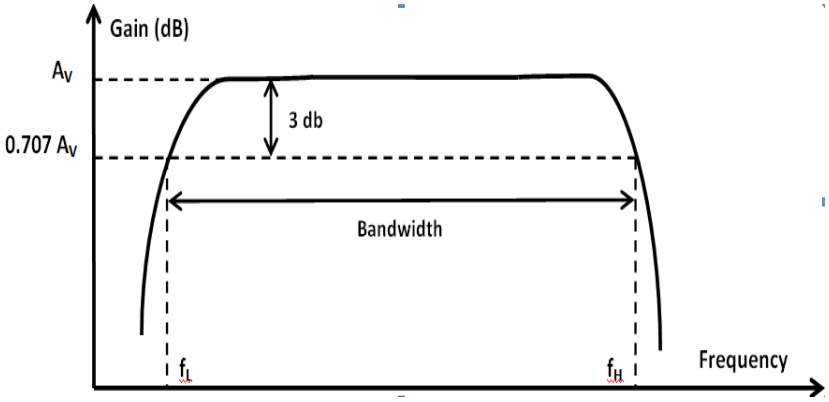
1. Connect the circuit as per the circuit diagram.
2. Set the input voltage to a constant value. (eg: 20 mV).
3. Vary the input frequency 0 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph (Gain (dB) Vs Frequency (Hz)).

Tabulation:

Input voltage, V_{in} (V) =

Frequency (Hz)	Output Voltage (volts) V_o	Gain= 20 log(V_o/V_{in}) (dB)

Model Graph:



Bandwidth Calculation:

f_L (Hz) =

f_H (Hz) =

Bandwidth (Hz) = f_H - f_L

Bandwidth (Hz) =

Result:

Thus the common source amplifier circuit has been designed and the frequency response is obtained.

Outcome:

Able to design and construct a common source amplifier circuit and determine the frequency response of the amplifier.

Practical Applications

1. Power Regulators
2. Audio Amplifier o/p stages
3. Used as switch

Viva – voce

1. What are the advantages of JFET over BJT?
2. Why input resistance in FET amplifier is more than the BJT amplifier?
3. Write the mathematical equation for g_m in terms of g_{mo}?
4. Why JFET has high input impedance?
5. List out the terminals in JFET.
6. What is the other name of JFET?
7. How gate terminal of JFET is bias?
8. What is the input control parameter of a JFET?
9. What is the output voltage of common source amplifier?
10. List out the advantages of JFET.
11. What is meant by VVR?
12. Why JFET is called unipolar transistor?
13. What is the importance of JFET?
14. In a JFET, what will happen to the depletion layers when drain voltage is equal to the pinch-off voltage?
15. Name the basic JFET amplifier configuration.
16. What is the other name of source follower?
17. Mention the applications of FET amplifier?
18. What are the differences between CS,CG and CD amplifier?
19. Mention the characteristics of CS amplifier?
20. What is gain BW product?
21. List out the different types of biasing for JFET.
22. Why FET is called as unipolar device?
23. Why the CS amplifier may be viewed as a transconductance amplifier or as a voltage amplifier?

Expt. No. 5 DARLINGTON AMPLIFIER

Aim:

To construct a Darlington amplifier circuit and plot the frequency response

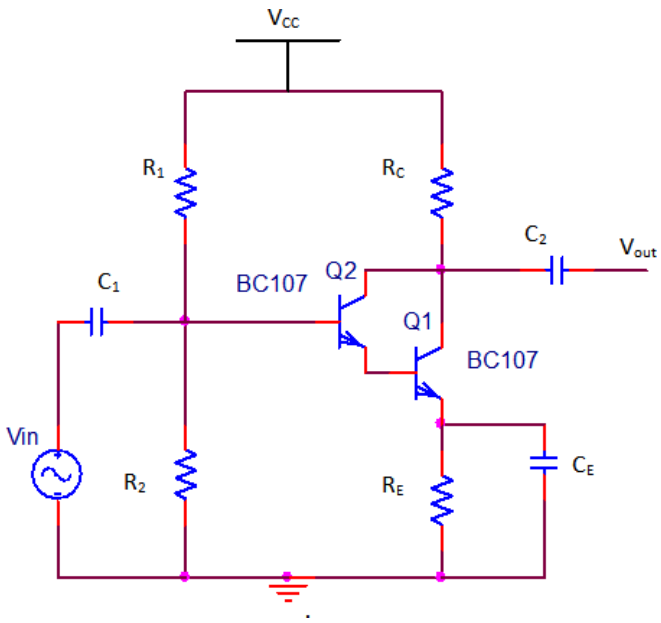
Apparatus Required:

S. No.	Apparatus	Range	Quantity
1	Transistor	BC107	2
2	Resistor	As per design	4
3	Capacitor	As per design	3
4	Power Supply	(0 - 30)V	1
5	Function Generator	(0 - 3)MHz	1
6	CRO	(0 - 30)MHz	1
7	Bread Board	-	1
8	Connecting wires	-	few

Theory:

In Darlington connection of transistors, emitter of the first transistor is directly connected to the base of the second transistor. Because of direct coupling, dc output current of the first stage is $(1+h_{fe})I_{b1}$. If Darlington connection for n transistor is considered, then due to direct coupling the dc output current foe last stage is $(1+h_{fe})$ n times I_{b1}.Due to very large amplification factor even two stage Darlington connection has large output current and output stage may have to be a power stage. As the power amplifiers are not used in the amplifier circuits, it is not possible to use more than two transistors in the Darlington connection. In Darlington transistor connection, the leakage current of the first transistor is amplified by the second transistor and overall leakage current may be high, which is not desired.

Circuit Diagram:



Design:

I_{CQ} = 50 mA

V_{CEQ} = 15 V

$V_E = \frac{V_{CC}}{10}$ \

V_E =

$R_E = \frac{V_E}{I_C} = \frac{1.5}{50\ \text{mA}}$

R_E =

Apply KVL to output loop,

$V_{CC} = I_C R_C + V_{CE} + I_E R_E$

$R_c = \frac{V_{CC} - V_{CE} - V_E}{I_C}$

R_C =

$R_2 = 0.1\beta\ R_E$

R_2 =

$V_{BE} = V_B - V_E$

$V_B = V_{BE} + V_E$

$V_B = \frac{R_2}{R_1 + R_2} \times V_{CC}$

$R_1 = R_2 \times \{\frac{V_{CC}}{V_B} - 1\}$

R_1 =

Procedure:

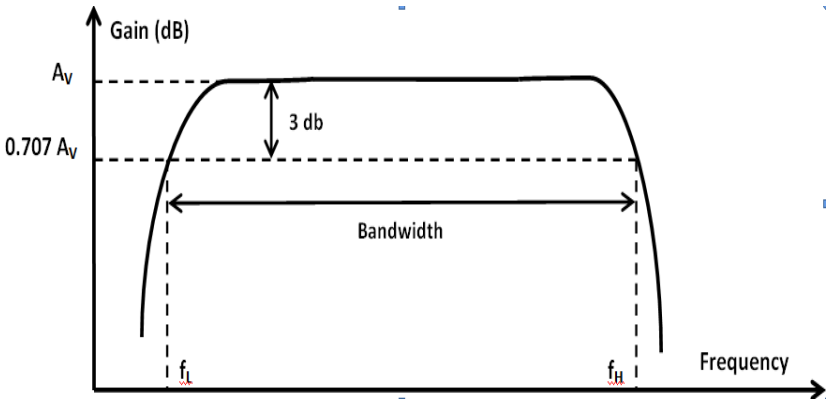
1. Connect the circuit as per the circuit diagram.
2. Set the input voltage to a constant value. (eg: 20 mV).
3. Vary the input frequency 0 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph (Gain (dB) Vs Frequency (Hz)).
5. Calculate the bandwidth from the graph.

Tabulation:

Input voltage, V_{in} (V) =

Frequency (Hz)	Output Voltage (volts) V_o	Gain= 20 log(V_o/V_{in}) (dB)

Model Graph:



Bandwidth Calculation:

f_L (Hz) =

f_H (Hz) =

Bandwidth (Hz) = f_H - f_L

Bandwidth (Hz) =

Result:

Thus the Darlington amplifier circuit has been designed and the frequency response is obtained.

Outcome:

Able to design and construct a Darlington amplifier circuit and determine the frequency response of the amplifier.

Practical Applications

1. Darlington amplifier is used as high power amplifier
2. A Darlington pair can be sensitive enough to respond to the current passed by skin contact even at safe voltages. Thus it can form the input stage of a touch-sensitive switch.
3. Darlington transistors can be used in high-current circuits, such as that involving computer control of motors or relays. The current is amplified from the normal low level of the computer output line to the amount needed by the connected device.
4. Power Regulators
5. Audio Amplifier o/p stages
6. Display drivers
7. Controlling of Solenoid
8. Light and touch sensors

Viva – voce

1. What is a Darlington pair?
2. Give few applications of Darlington amplifier.
3. What are the advantages of using Darlington pair of transistors?
4. Why do you avoid RC or transformer coupling for amplifying extremely low frequency signals?
5. Why transformer coupling does give poor frequency response?
6. List out the techniques to improve the input impedance.
7. Why Darlington connection is given to the circuit?
8. What is meant by bootstrapping technique?
9. What is the value of reactance capacitances at low frequencies?
10. What is the name of an amplifier in which voltage gain is more important than power gain?
11. Whether Darlington connection can be used for more number of stages?

12. What is meant by “equivalent circuit” of a transistor?
13. List out the benefits of h-parameters.
14. Write the current gain of Darlington amplifier.
15. Write the voltage gain of Darlington amplifier.

Expt. No. 6 CASCADE AMPLIFIER

Aim:

To construct a Cascade amplifier circuit and plot the frequency response

Apparatus Required:

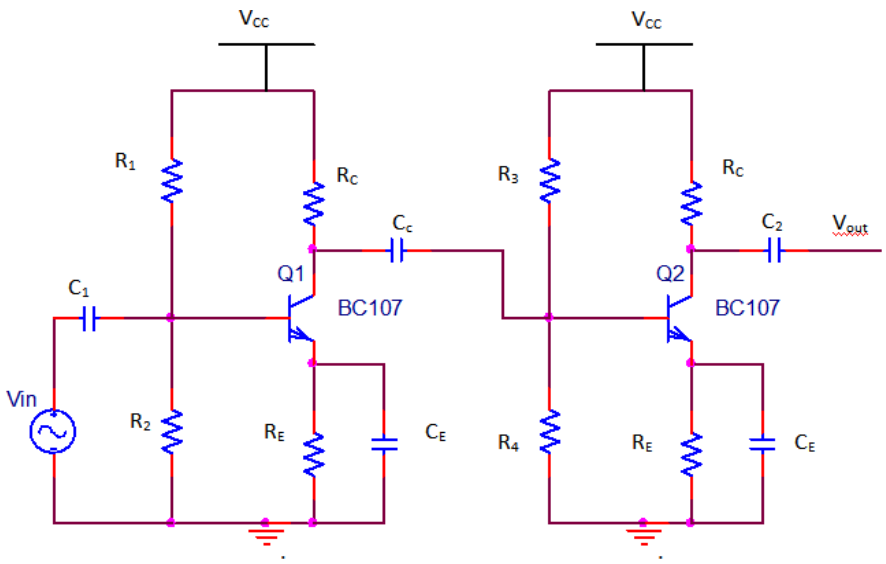
S. No.	Apparatus	Range	Quantity
1	Transistor	BC107	2
2	Resistor	As per design	8
3	Capacitor	As per design	5
4	Power Supply	(0 - 30)V	1
5	Function Generator	(0 - 3)MHz	1
6	CRO	(0 - 30)MHz	1
7	Bread Board	-	1
8	Connecting wires	-	few

Theory:

Multistage amplifiers are made up of single transistor amplifiers connected in cascade. The first stage usually provides a high input impedance to minimize loading the source (transducer). The middle stages usually account for most of the desired voltage gain. The final stage provides a low output impedance to prevent loss of signal (gain) and to be able to handle the amount of current required by the load. In analyzing multistage amplifiers, the loading effect of the next stage must be considered since the input impedance of the next stage acts as the load for the current stage. Therefore the AC analysis of a multistage amplifier is usually done starting with the final stage. The individual stages are usually coupled by either capacitor or direct coupling. Capacitor coupling is most often used when the signals being amplified are AC signals. In capacitor coupling, the stages are separated by a

capacitor which blocks the DC voltages between each stage. This DC blocking prevents the bias point of each stage from being upset.

Circuit Diagram:



Procedure:

1. For stage 1, Connect the circuit as per the circuit diagram.
2. Set the input voltage to a constant value. (eg: 20 mV).
3. Vary the input frequency 0 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph (Gain (dB) vs Frequency (Hz)).
5. Perform frequency response analysis for stage 2.
6. Connect the output of stage 1 to the input of stage 2 by capacitive coupling
7. Perform frequency response analysis for the cascade stage.

Tabulation:

Stage 1:

Input voltage, V_{in} (V) =

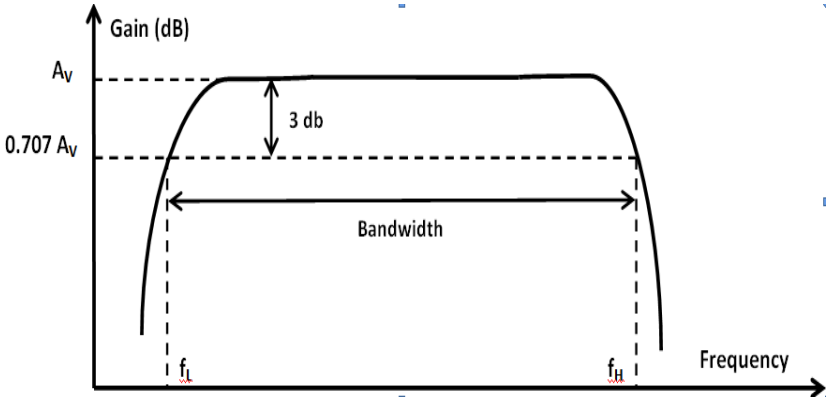
Frequency (Hz)	Output Voltage (volts) V_o	Gain= 20 log(V_o/V_{in}) (dB)

Stage 2:

Input voltage, V_{in} (V) =

Frequency (Hz)	Output Voltage (volts) V_o	Gain= 20 log(V_o/V_{in}) (dB)

Model Graph:



Cascade Stage:

Input voltage, V_{in} (V) =

Frequency (Hz)	Output Voltage (volts) V_o	Gain= 20 log(V_o/V_{in}) (dB)

Bandwidth Calculation:

f_L (Hz) =

f_H (Hz) =

Bandwidth (Hz) = $f_H - f_L$

Bandwidth (Hz) =

Result:

Thus the cascade amplifier circuit has been designed and the frequency response is obtained.

Outcome:

Able to design and construct a cascade amplifier circuit and determine the frequency response of the amplifier.

Practical Applications

1. Cascading amplifiers are used to increase signal strength in Television receiver.
2. Used in computers,
3. Used in regulator circuits
4. It also forms a building block for differential amplifiers and operational amplifiers.

Viva – voce

1 What is an effect of cascading?

2 List out the difference between cascade and cascode amplifiers.

3 Give the reason why RC coupling is not used to amplify extremely low frequencies.

4 What type of coupling is used in final stage of the multistage transistor amplifier?

5 What do you understand by multistage transistor amplifier?

6 Why is transformer coupling used in the final stage of a multistage amplifier?

7 How will you achieve impedance matching with transformer coupling?

8 Why do you prefer to express the gain in db?

9 Give the advantages of RC coupling.

10 In a RC coupled amplifier, what will be the voltage gain over the mid-frequency range?

11 When we use transformer coupling?

12 What is the other name of upper and lower cutoff frequency?

13 What is the purpose of RC or transformer coupling?

14 What type of transformer is normally used for impedance matching?

15 What is meant by direct coupling?

Expt. No. 7 CASCODE AMPLIFIER

Aim:

To construct a cascode amplifier circuit and plot the frequency response

Apparatus Required:

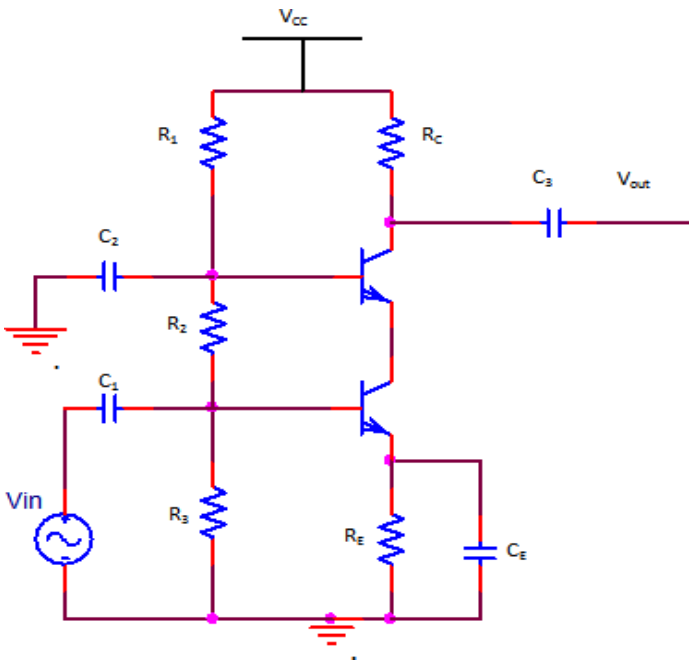
S. No.	Apparatus	Range	Quantity
1	Transistor	BC107	1
2	Resistor	As per design	5
3	Capacitor	As per design	4
4	Power Supply	(0 - 30)V	1
5	Function Generator	(0 - 3)MHz	1
6	CRO	(0 - 30)MHz	1
7	Bread Board	-	1
8	Connecting wires	-	few

Theory:

An important amplifier configuration is known as cascode amplifier. It consists of a common-emitter (CE) stage followed by a common-base (CB) stage as shown in figure. The common-emitter configuration presents a relatively high input resistance $(\beta_{ac} + 1) * r_e$ to the signal source. The common-base configuration presents a

very low input resistance r_e . By replacing the collector resistance R_C in the CE amplifier stage with a common base CB amplifier stage, the CE-CB configuration virtually eliminates the Miller effect of C_{u1} . This will lead to higher 3dB frequency than is possible with a simple common-emitter amplifier. An extension in the upper cutoff frequency is achieved without reducing the midband gain (Gain-Bandwidth rule), since the collector of Q_2 carriesa current almost equal to the collector current of Q_1. Another reason for extending the upper cutoff frequency isthat, in the CB configuration the Miller effect does not exist and does not limit the high-frequency response. Notice that the effective load resistance seen by the CE transistor Q_1 is very low and equal to the input resistance r_e of the CB transistor Q_2. The transistor Q_2 acts as a current buffer or an impedance transformer.

Circuit Diagram:



Procedure:

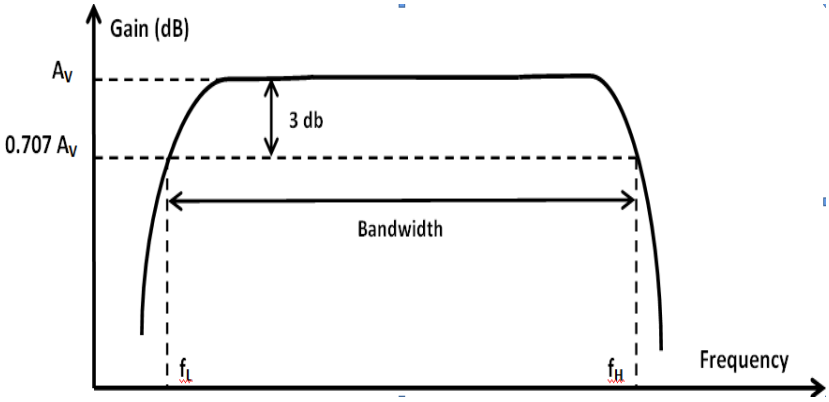
1. Connect the circuit as per the circuit diagram.
2. Set the input voltage to a constant value. (eg: 20 mV).
3. Vary the input frequency 0 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph (Gain (dB) Vs Frequency (Hz)).

Tabulation:

Input voltage, V_{in} (V) =

Frequency (Hz)	Output Voltage (volts) V_o	Gain= 20 log(V_o/V_{in}) (dB)

Model Graph:



Bandwidth Calculation:

f_L (Hz) =

f_H (Hz) =

Bandwidth (Hz) = f_H - f_L

Bandwidth (Hz) =

Result:

Thus the cascode amplifier circuit has been designed and the frequency response is obtained.

Outcome:

Able to design and construct a cascode amplifier circuit and determine the frequency response of the amplifier.

Practical Applications

1. Cascode amplifier has high output impedance and high gain
2. It is used to insulate o/p and i/p (coupling due to parasitic capacitances (Cgd)).
3. Cascode doesn't contribute to noise and mismatch and it is used to improve gain.

Viva – voce

1. What is cascading and cascoding?
2. Why is a cascode amplifier called as wide band amplifier?
3. What are the characteristics of a cascode amplifier?
4. List out the uses of cascode amplifier.
5. Name some multistage amplifier.
6. Which type of connection is made for cascode amplifier?
7. What is the most desirable feature of a transformer coupled amplifier?
8. Why cascode amplifier is called as wide band amplifier?
9. What are the characteristics of cascode amplifier?
10. Which type of coupling is used in the initial stages of a multi stage amplifier?
11. Compare the bandwidth of a single stage amplifier with that of a multi stage amplifier.

Expt. No. 8 DIFFERENTIAL AMPLIFIER USING BJT

Aim:

To construct a differential amplifier using BJT and to determine

1. The transfer characteristic of transistors
2. Calculate the CMRR value

Apparatus Required:

S. No.	Apparatus	Range	Quantity
1	Transistor	BC107	2
2	Resistor	As per design	3
3	Power Supply	(0 - 30)V	4
4	Multimeter	-	1
5	Bread Board	-	1
6	Connecting wires	-	few

Formula:

Common mode Gain (A_c)= V_O / V_{IN}

Differential mode Gain (A_d)= V_0 / V_{IN}

where, $V_{IN}=V_1 - V_2$

Common Mode Rejection Ratio (CMRR) = A_d/A_c

where, A_d is the differential mode gain, A_c is the common mode gain.

Theory:

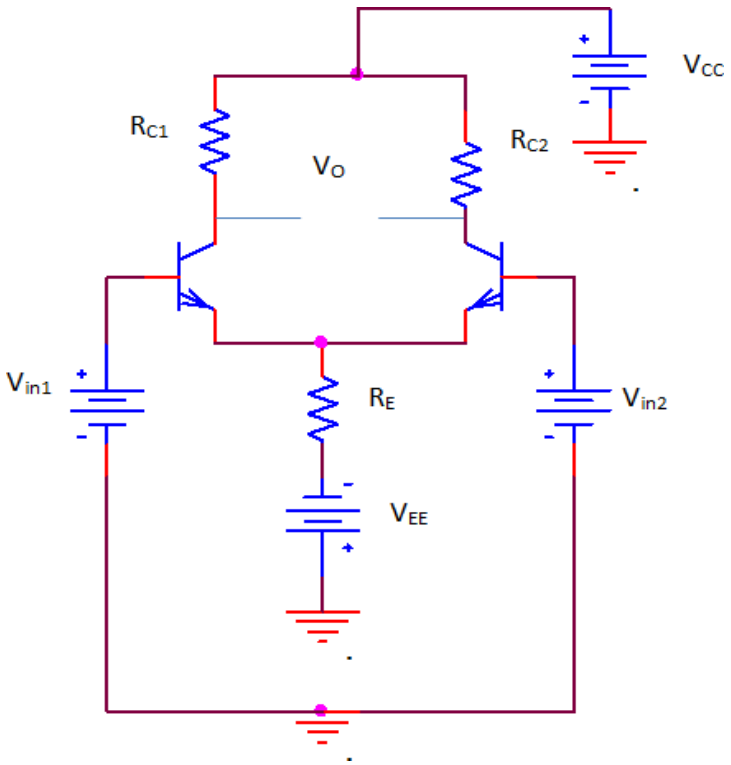
The differential amplifier is a basic stage of an integrated operational amplifier. It is used to amplify the difference between two signals. It has excellent stability, high versatility and immunity to noise. In a practical differential amplifier, the output depends not only upon the difference of the two signals but also depends upon the common mode signal.

Transistor Q_1 and Q_2 have matched characteristics. The values of R_{C1} and R_{C2} are equal. R_{e1} and R_{e2} are also equal and this. The output is taken between the two output terminals. For the differential mode operation the input is taken from two different sources and the common mode operation the applied signals are taken from the same source Common Mode Rejection Ratio (CMRR) is an important parameter of the differential amplifier. CMRR is defined as the ratio of the differential mode gain, A_d to the common mode gain, A_c.

CMRR = A_d / A_c In ideal cases, the value of CMRR is very high.

Circuit Diagram:

Differential mode:

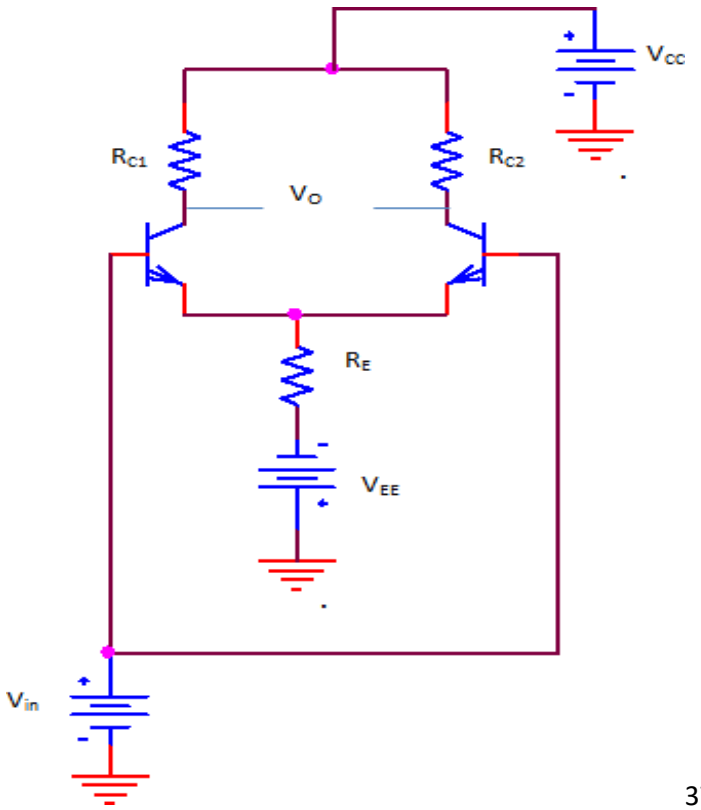


Tabulation:

V_{in1}(V)	V_{in2}(V)	V_{in} (V)	V_{o1}(V)	V_{o2}(V)	V_o(V)	A_D

Circuit Diagram:

Common Mode:



Tabulation:

V_{in} (V)	V_{o1}(V)	V_{o2}(V)	V_o(V)	A_D

Procedure:

1. Connections are given as per the circuit diagram.
2. To determine the common mode gain, set input signal with voltage V_{IN} and determine V_o at the collector terminals. Calculate common mode gain, $A_c=V_o/V_{in}$.
3. To determine the differential mode gain, set input signals with voltages V_1 and V_2. Compute $V_{in}=V_1-V_2$ and find V_o at the collector terminals. Calculate differential mode gain, $A_d=V_o/V_{in}$.
4. Calculate the CMRR= A_d / A_c.

Result:

Thus the differential amplifier using BJT have been designed and the CMRR is calculated.

Outcome:

Able to construct a differential amplifier circuit and determine the CMRR value.

Practical Applications

1. microphone preamplifiers
2. audio preamplifiers
3. FM/AM radio signal recovery
4. TV signal recovery
5. digital to analog converters (get rid of any common quantisation noise)

Viva – voce

1. What are the methods of improving CMRR?
2. Define Common Mode Rejection Ratio.
3. Give few applications of differential amplifier
4. How do you overcome common mode noise?
5. State the various configurations of differential amplifier.
6. What is double ended and single ended input?
7. What is current mirror?
8. What is an active load?
9. What is the differential gain of a differential amplifier?
10. What is the ideal value of CMRR?
11. State two modes of operation for differential amplifier.
12. State the various features of differential amplifier.
13. State the various methods of improving CMRR.
14. What is the ideal value of common-mode gain of differential amplifier?
15. When do you called output of differential amplifier as balanced output?

Expt. No. 9

SIMULATION OF COMMON EMITTER AND COMMON SOURCE AMPLIFIER USING PSpice

Aim:

To design, simulate and to obtain the frequency response of

(i) Common emitter amplifier

(ii) Common source amplifier circuit using PSpice.

Apparatus Required:

S. No.	Apparatus	Range	Quantity
1	PC System	-	1
2	OrCAD PSpice Version 9.1	-	-

Theory:

The CE amplifier provides high gain and wide frequency response. The emitter lead is common to both input & output circuits and is grounded. The emitter-base circuit is forward biased. The collector current is controlled by the base current rather than emitter current. The input signal is applied to base terminal of the transistor and amplifier output is taken across collector terminal. A very small change in base current produces a much larger change in collector current. When positive half-cycle is fed to the input circuit, it opposes the forward bias of the circuit which causes the collector current to decrease; it decreases the voltage further more negative. Thus when input cycle varies through a negative half-cycle, it increases the forward bias of the circuit, which causes the collector current to increases thus the output signal in common emitter amplifier is out of phase with the input signal.

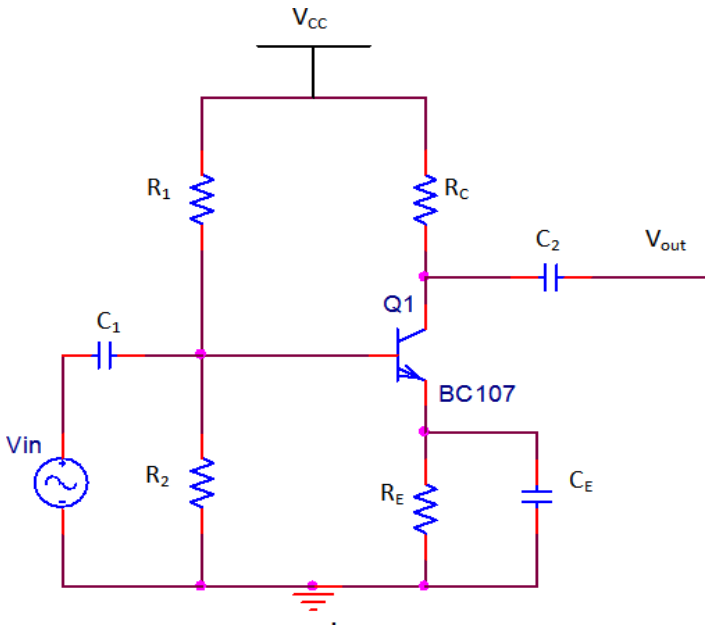
A field-effect transistor (FET) is a type of transistor commonly used for weak-signal amplification. The device can amplify analog or digital signals. It can also switch DC or function as an oscillator. In the FET, current flows along a semiconductor path called the channel. At one end of the channel, there is an electrode called the source. At the other end of the channel, there is an electrode called the drain. The physical diameter of the channel is fixed, but its effective electrical diameter can be varied by the application of a voltage to a control electrode called the gate. Field-effect transistors exist in two major classifications. These are known as the junction FET (JFET) and the Metal Oxide Semiconductor FET (MOSFET). The junction FET has a channel consisting of N-type semiconductor (N-channel) or P-type semiconductor (P-channel) material; the gate is made of the opposite semiconductor type.

In P-type material, electric charges are carried mainly in the form of electron deficiencies called holes. In N-type material, the charge carriers are primarily electrons. In a JFET, the junction is the boundary between the channel and the gate. Normally, this P-N junction is reverse-biased (a DC voltage is applied to it) so that no current flows between the channel and the gate. However, under some conditions there is a small current through the junction during part of the input signal cycle. The FET has some advantages and some disadvantages relative to the bipolar transistor. Field-effect transistors are preferred for weak-signal work, for example in wireless, communications and broadcast receivers. They are also preferred in circuits and systems requiring high impedance. The FET is not, in general, used for high-power amplification, such as is required in

large wireless communications and broadcast transmitters. Field-Effect Transistors are fabricated onto silicon integrated circuit (IC) chips. A single IC can contain many thousands of FETs, along with other components such as resistors, capacitors, and diodes.

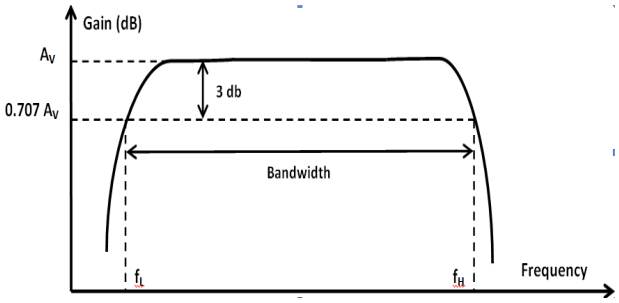
Circuit Diagram:

Common Emitter Amplifier:



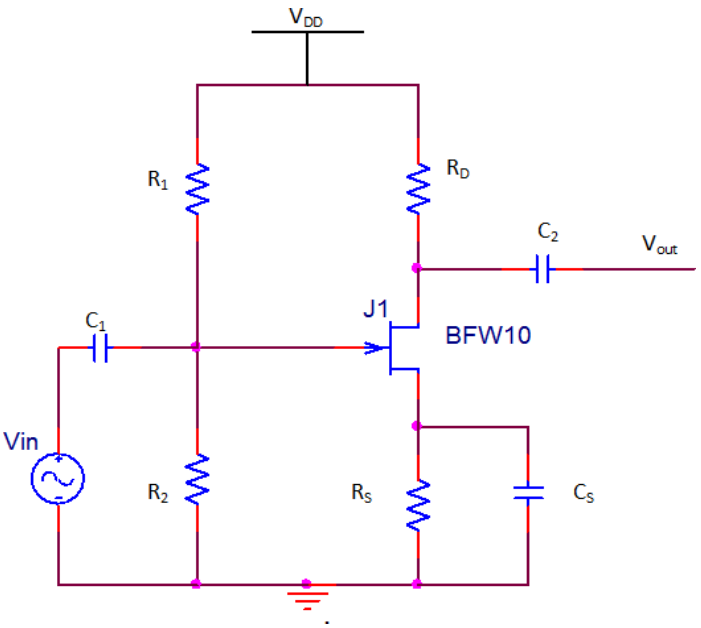
Model Graph:

Common Emitter Amplifier:



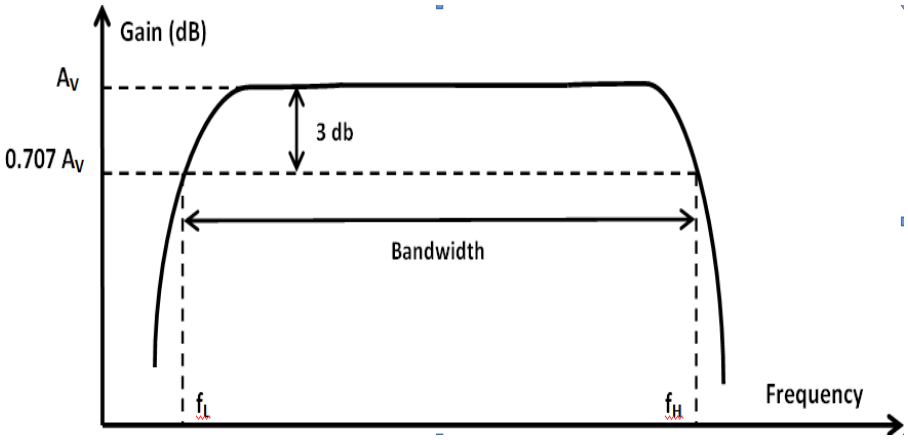
Circuit Diagram:

Common Source Amplifier:



Model Graph:

Common Source Amplifier:



Procedure:

1. Start the program
2. Select the ORCAD release 9 capture CIS
3. Go to new and select project
4. Create the title of the project
5. Drag the elements as per the circuit diagram requirement.
6. Make connections as per the circuit diagram using wire icon.
7. Create the new simulation
8. Set the output level setting.
9. Placed the voltage markers in input and output mode.

10. Run the circuit diagram and print the output.

Result:

Thus the common emitter and common source amplifier circuits have been designed and simulated using PSpice and the frequency response is obtained.

Outcome:

Able to design and construct a CE and CS amplifier circuit and determine the frequency response of the amplifier using PSpice.

Practical Applications

1. Common emitter amplifiers are used as Low frequency voltage amplifier.
2. Common emitter amplifiers are also used in radio frequency transceiver circuits. (Radio)
3. Common emitter configuration commonly used in low-noise amplifiers.
4. Common emitter amplifiers have both voltage and current gain, hence they are used as driving stages of many audio amplifiers. It can amplify headphone audio, condenser mic audio.
5. Common emitter amplifiers are also used in output drive stages of a large LED circuit or in a circuit with multiple loads like LED, Buzzer, Resistor, coils, etc
6. Common Source amplifier is used in Power Regulators, Audio Amplifier o/p stages and Used as switch

Viva – voce

1. What is PSpice?
2. Compare the Gain Bandwidth product of CE and CS amplifier.
3. Write the types of analysis performed by PSpice.
4. Write the types of sources available in PSpice.
5. What will happen to the output signal if the operating point locates nearer to the cut-off region?
6. What will happen to the output signal if the operating point locates nearer to the saturation region?
7. What is meant by a.c. load line?
8. What is meant by Beta?
9. Give the relationship between Alpha and Beta.
10. What is the phase difference between the output and input voltages of a CE amplifier?
11. What is the purpose of capacitors in a transistor amplifier?
12. To obtain highest power gain, which transistor configuration is used?

13. What is the other name CE amplifier?
14. List out the advantages of JFET.
15. What is meant by VVR?
16. Why JFET is called unipolar transistor?
17. What is the importance of JFET?
18. In a JFET, what will happen to the depletion layers when drain voltage is equal to the pinch-off voltage?
19. Name the basic JFET amplifier configuration.
20. What is the other name of source follower?
21. Mention the applications of FET amplifier?

Expt. No. 10 DESIGN AND IMPLEMENTATION OF CODE CONVERTOR

Aim:

To design and implement 4-bit

(i) Binary to gray code converter
(ii) Gray to binary code converter
(iii) BCD to excess-3 code converter
(iv) Excess-3 to BCD code converter

APPARATUS REQUIRED:

Sl.No.	Component	Specification	Qty.
1.	X-OR GATE	IC 7486	1
2.	AND GATE	IC 7408	1
3.	OR GATE	IC 7432	1
4.	NOT GATE	IC 7404	1
5.	IC TRAINER KIT	-	1
6.	PATCH CORDS	-	35

THEORY:

The availability of large variety of codes for the same discrete elements of information results in the use of different codes by different systems. A conversion circuit must be inserted between the two systems if each uses different codes for same information. Thus, code converter is a circuit that makes the two systems compatible even

though each uses different binary code.

The bit combination assigned to binary code to gray code. Since each code uses four bits to represent a decimal digit. There are four inputs and four outputs. Gray code is a non-weighted code.

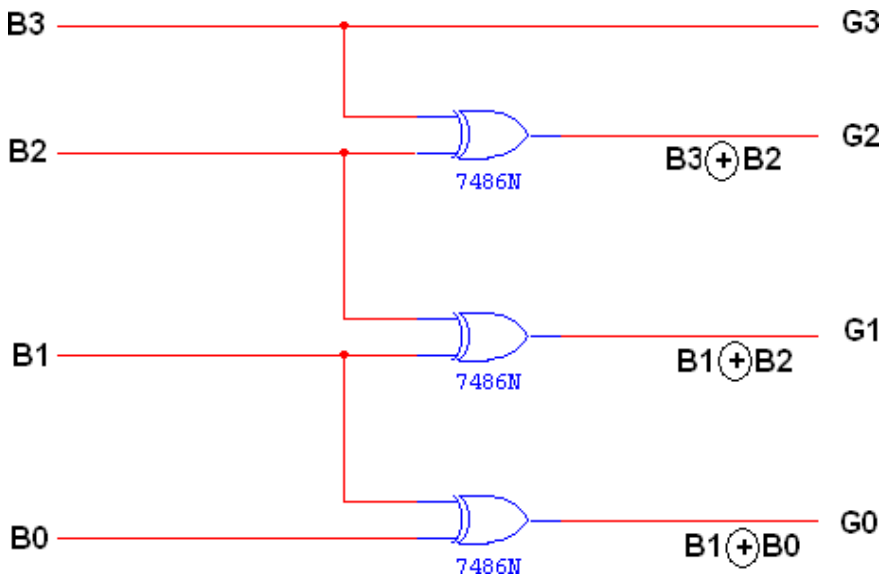
The input variable are designated as B3, B2, B1, B0 and the output variables are designated as C3, C2, C1, Co. from the truth table, combinational circuit is designed. The Boolean functions are obtained from K-Map for each output variable.

A code converter is a circuit that makes the two systems compatible even though each uses a different binary code. To convert from binary code to Excess-3 code, the input lines must supply the bit combination of elements as specified by code and the output lines generate the corresponding bit combination of code. Each one of the four maps represents one of the four outputs of the circuit as a function of the four input variables.

A two-level logic diagram may be obtained directly from the Boolean expressions derived by the maps. These are various other possibilities for a logic diagram that implements this circuit. Now the OR gate whose output is C+D has been used to implement partially each of three outputs.

Logic Diagram:

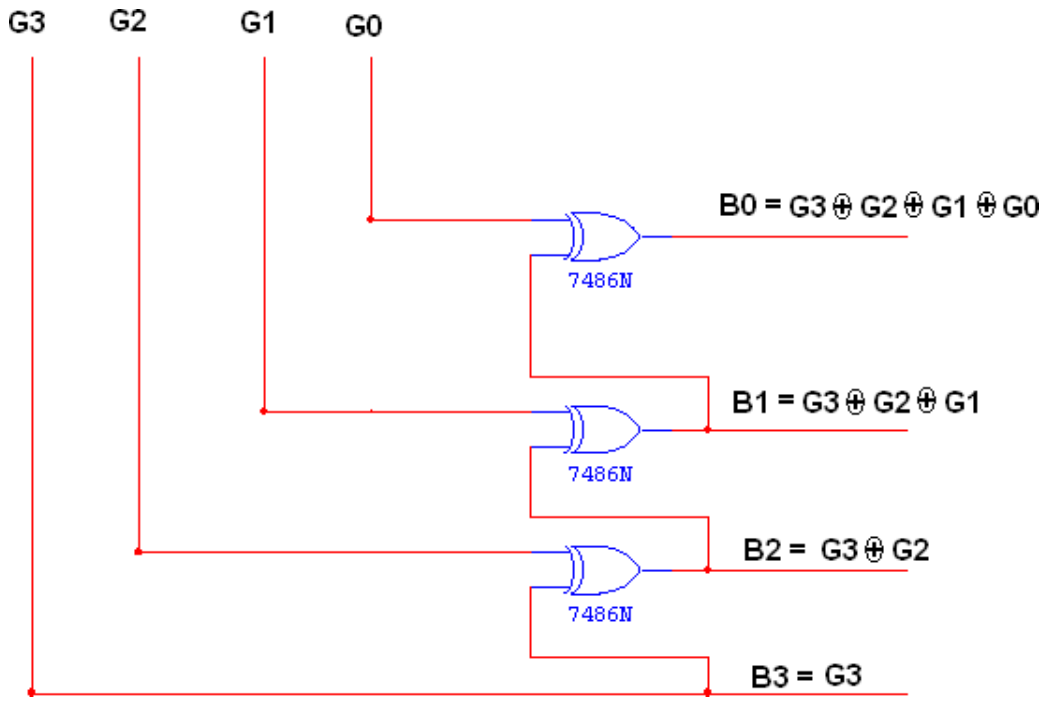
BINARY TO GRAY CODE CONVERTOR


B3
B2
B1
B0
7486N
7486N
7486N
G3
G2
B3⊕B2
G1
B1⊕B2
G0
B1⊕B0

Truth Table:

Binary input				Gray code output			
B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

Logic Diagram:



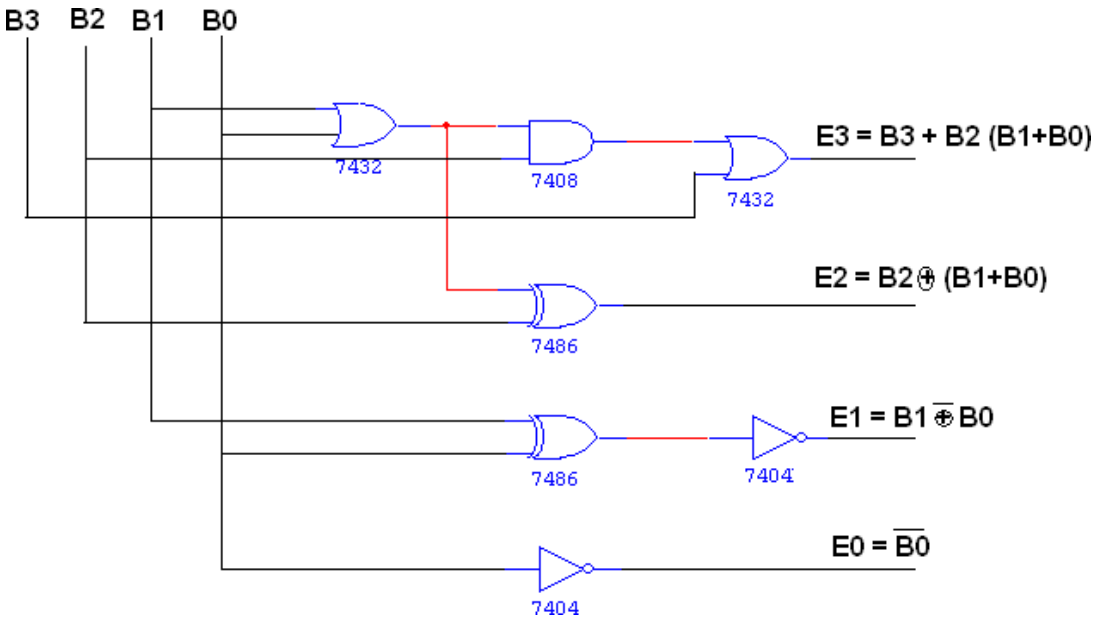
Truth Table:

| Gray Code | Binary Code |

G3	G2	G1	G0	B3	B2	B1	B0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

Logic Diagram:

BCD TO EXCESS-3 CONVERTOR

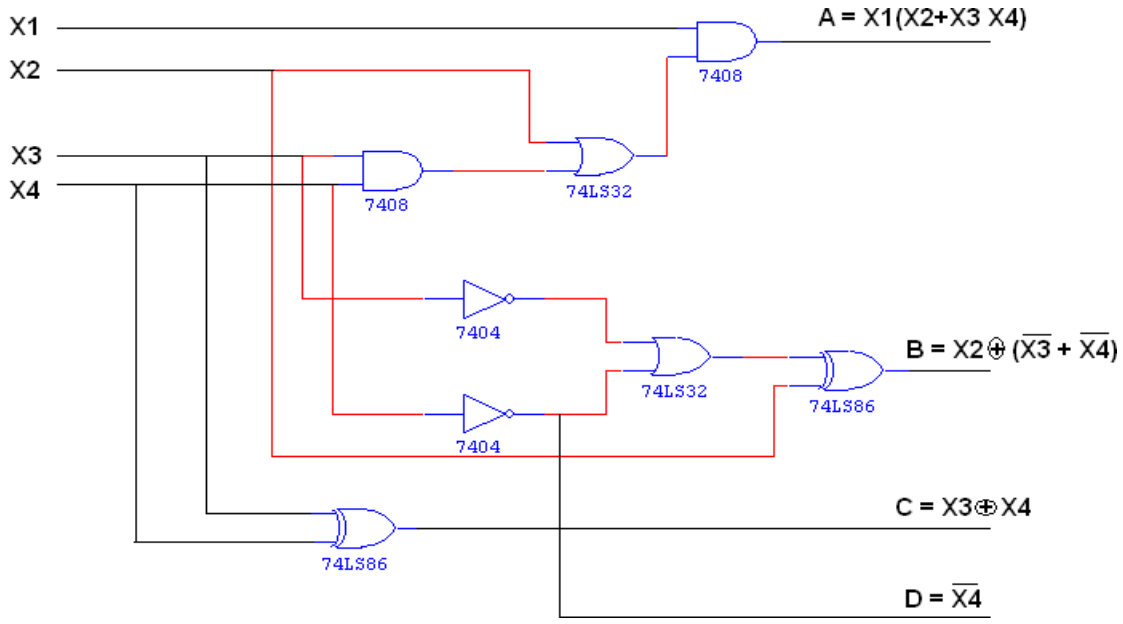


Truth Table:

BCD input				Excess – 3 output			
B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	x	x	x	x
1	0	1	1	x	x	x	x
1	1	0	0	x	x	x	x
1	1	0	1	x	x	x	x
1	1	1	0	x	x	x	x
1	1	1	1	x	x	x	x

Logic Diagram:

EXCESS-3 TO BCD CONVERTOR


X1
X2
X3
X4
A = X1(X2+X3 X4)
7408
7408
74LS32
7404
7404
74LS32
74LS86
B = X2⊕(X3 + X4)
74LS86
C = X3⊕X4
D = X4

Truth Table:

Excess – 3 Input				BCD Output			
B3	B2	B1	B0	G3	G2	G1	G0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0

1 1 1	0 0 1	1 1 0	0 1 0	0 1 1	1 0 0	1 0 0	1 0 1

PROCEDURE:

(i) Connections were given as per circuit diagram.
(ii) Logical inputs were given as per truth table
(iii) Observe the logical output and verify with the truth tables.

Result:

Thus, binary to gray code converter, Gray to binary code converter, BCD to excess-3code converter, Excess-3 to BCD code converter was implemented.

Outcomes:

Able to understand the concept, realize and implement the code converter.

Practical Applications

1. Code conversions are widely used to facilitate error correction in digital communications such as digital terrestrial television and some cable TV systems.
2. It is used in Digital System design
3. It is used in Computers
4. It is used in telephone transmission
5. It is used in television transmission

Viva – voce

1. What is combinational circuit?
2. What is code converter?
3. What is the other name for Gray code?

4. What is the application of Excess-3 Code?
5. What is ASCII code?
6. How many bits are there in an ASCII code?
7. What is the primary use for Gray code?
8. Give any one way to convert BCD to binary using the hardware approach.
9. Why is the Gray code more practical to use when coding the position of a rotating shaft?
10. Which binary code has a progress such that only one bit changes between two successive codes?
11. Find the equivalent decimal number for gray code 1011.
12. What is the other name for Excess “3” code?
13. Give expansion of BCD code.
14. What is the modified form of BCD number?
15. How to derive an Excess - 3 code from natural BCD code?
16. Why Gray code is often used in digital systems?
17. Name few weighted codes.
18. What is the difference between weighted and non weighted code?
19. How many numbers are used out of possible 16 code combination in Excess-3 code?
20. What is Most Significant Bit (MSB)?
21. What are the classifications of binary codes?
22. What are the two steps in Gray to binary code conversion?
23. What are the two steps in binary to Gray code conversion?
24. What are the basic logic gates?

Expt . No. 11 DESIGN OF 4-BIT ADDER/SUBTRACTOR AND BCD ADDER

Aim:

To design and implement 4-bit adder/subtractor and BCD adder using IC 7483

Apparatus Required

Sl.No.	Component	Specification	Qty.
1.	IC	IC 7483	1
2.	EX-OR Gate	IC 7486	1
3.	NOT Gate	IC 7404	1
3.	IC Trainer Kit	-	1
4.	Patch Cords	-	40

Theory:

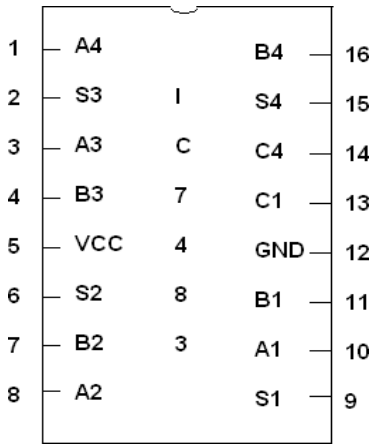
4 Bit Binary Adder / Subtractor:

The addition and subtraction operation can be combined into one circuit with one common binary adder. The mode input M controls the operation. When M=0, the circuit is adder circuit. When M=1, it becomes subtractor. 4 Bit BCD Adders:

Consider the arithmetic addition of two decimal digits in BCD, together with an input carry from a previous stage. Since each input digit does not exceed 9, the output sum cannot be greater than 19, the 1 in the sum being an input carry. The output of two decimal digits must be represented in BCD and should appear in the form listed in the columns. A BCD adder that adds 2 BCD digits and produce a sum digit in BCD. The 2 decimal digits, together with the input carry, are first added in the top 4 bit adder to produce the binary sum.

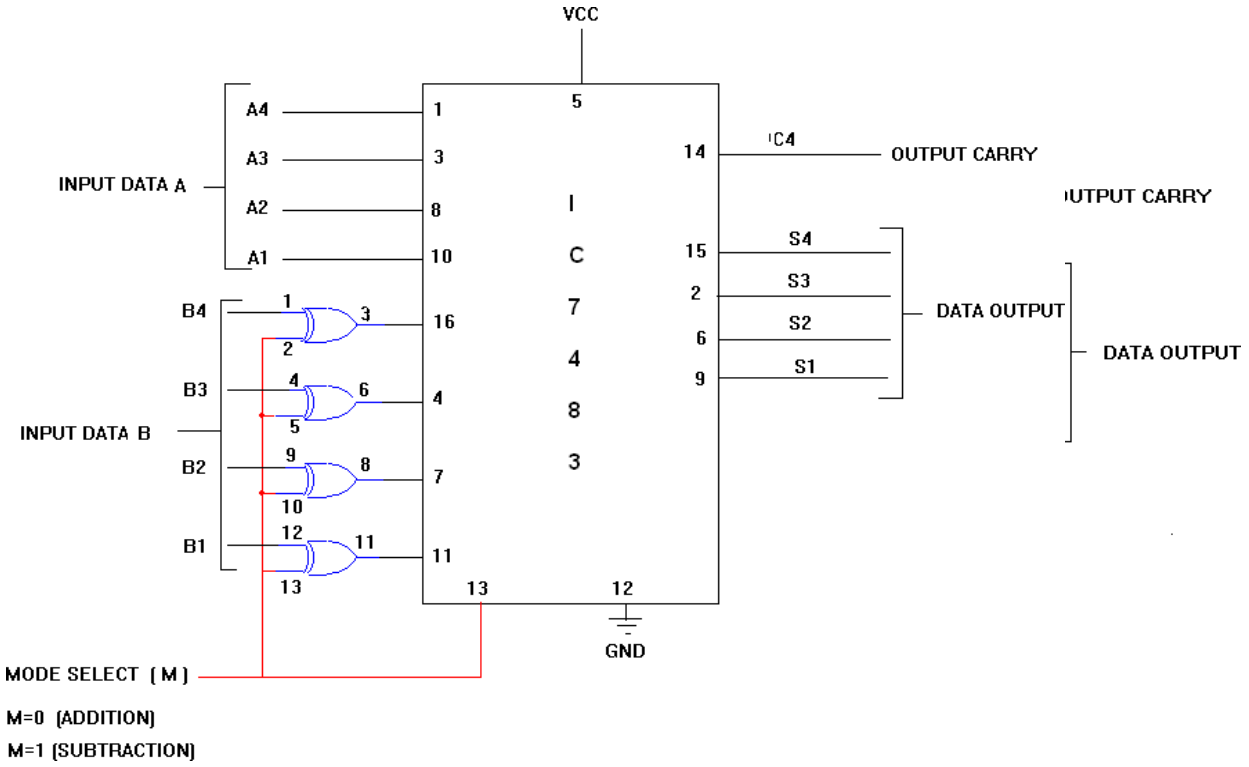
4 Bit Binary Adder / Subtractor:

Pin Diagram - IC 7483:



Logic Diagram:

4-Bit Binary Adder / subtractor



Truth Table:

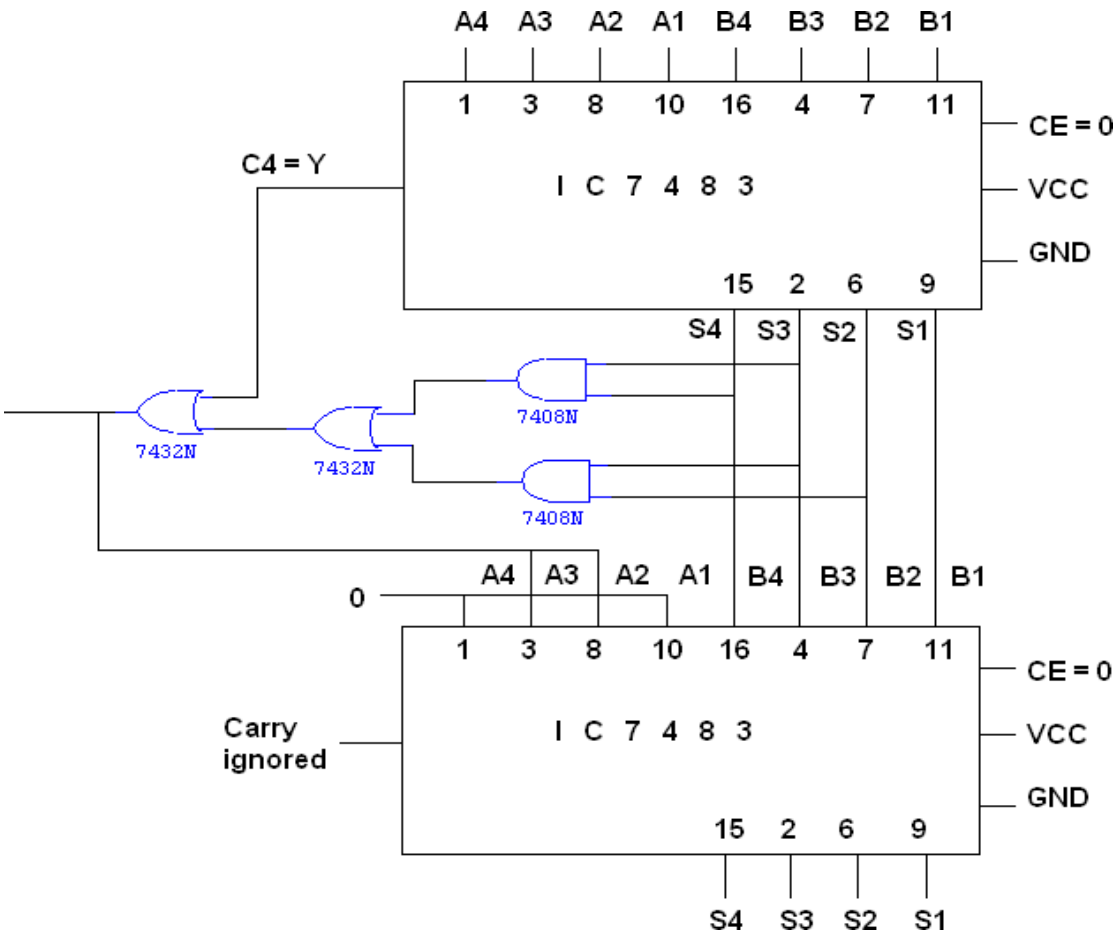
4-Bit Binary Adder/Subtractor:

Input Data A				Input Data B				Addition					Subtraction				
A4	A3	A2	A1	B4	B3	B2	B1	C	S 4	S3	S 2	S1	B	D4	D3	D2	D1
1	0	0	0	0	0	1	0	0	1	0	1	0	1	0	1	1	0
1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0
0	0	1	0	1	0	0	0	0	1	0	1	0	0	1	0	1	0
0	0	0	1	0	1	1	1	0	1	0	0	0	0	1	0	1	0

1	0	1	0	1	0	1	1	1	0	0	1	0	0	1	1	1	1
1	1	1	0	1	1	1	1	1	1	0	1	0	0	1	1	1	1
1	0	1	0	1	1	0	1	1	0	1	1	1	0	1	1	0	1

Logic Diagram:

BCD Adder:



Truth Table for BCD Adders:

BCD SUM				CARRY
S4	S3	S2	S1	C
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Procedure:

(i) Make the connections as per circuit diagram.

(ii) Apply logical inputs as per truth table.

(iii) Observe the logical output and verify with the truth tables.

Result:

Thus the 4-bit adder / subtractor and BCD adder using IC 7483 was designed and implemented.

Outcomes:

Able to understand the concept, realize and implement the 4-bit adder / Subtractor and BCD adder.

Practical Applications

1. Smart thermostats
2. appliances such as washing machines or driers that have digital read outs
3. digital alarm clocks, digital wrist watches
4. game consoles

Viva – voce

1. Define Half and Full adder
2. What is a BCD adder?

3. What is the difference between a binary adder and a BCD adder?
4. What are the two types of basic adder circuits?
5. What is the use of an half adder?
   What is the difference between a half adder and a full adder?
6. What is the difference between a binary adder and a BCD adder?
7. What are the two types of basic subtractor circuits?
8. What is the difference between a binary adder and a full adder?
9. Write down the truth table of a full adder
10. Write down the truth table of a full sub tractor
11. Write down the truth table of a half sub tractor.
12. What is the sum when a binary adder is used as BCD adder?
13. How a full subtractor can be implemented from a full adder?
14. Design a circuit for finding the 9's compliment of a BCD number using 4-bit binary adder and some external logic gates.
15. Write the Boolean expression for half adder.
16. Write the Boolean expression for full adder.
17. Write the Boolean expression for half subtractor.
18. Write the Boolean expression for full subtractor.
19. Give few applications of adder circuits.
20. Give few applications of BCD adder circuits.
21. Give few applications of subtractor circuits.
22. What are don't care condition?
23. What are combinational circuits?

Expt. No. 12 DESIGNS AND IMPLEMENTATION OF MULTIPLEXER AND DE-MULTIPLEXER

Aim:

To design and implement multiplexer and demultiplexer using logic gates

Apparatus Required

Sl.No.	Component	Specification	Qty.
1.	3 I/P AND GATE	IC 7411	2
2.	OR GATE	IC 7432	1
3.	NOT GATE	IC 7404	1
2.	IC TRAINER KIT	-	1
3.	PATCH CORDS	-	32

Theory:

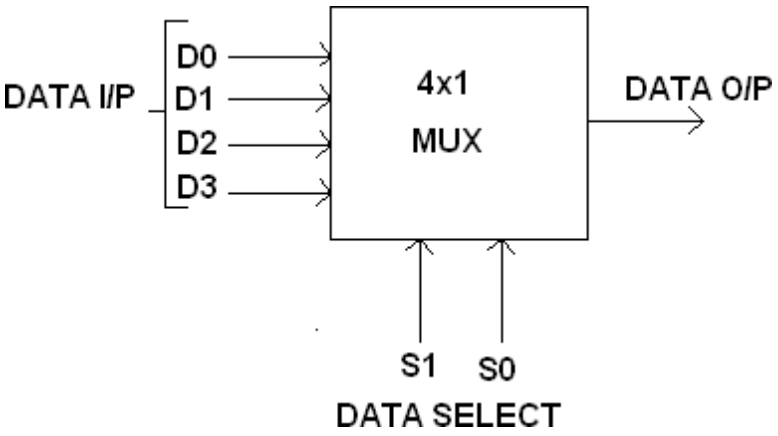
Multiplexer:

Multiplexer means transmitting a large number of information units over a smaller number of channels or lines. A digital multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally there are 2^n input line and n selection lines whose bit combination determine which input is selected.

Demultiplexer:

The function of demultiplexer is in contrast to multiplexer function. It takes information from one line and distributes it to a given number of output lines. For this reason, the demultiplexer is also known as a data distributor. Decoder can also be used as demultiplexer. In the 1: 4 demultiplexer circuit, the data input line goes to all of the AND gates. The data select lines enable only one gate at a time and the data on the data input line will pass through the selected gate to the associated data output line.

Block Diagram for 4:1 Multiplexer:

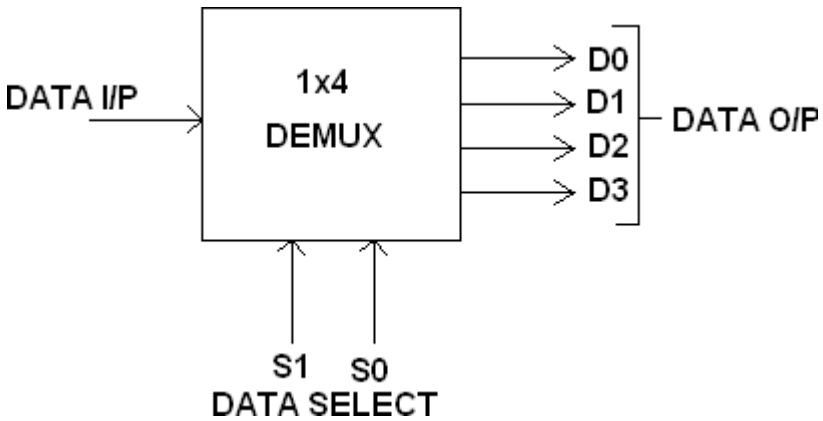


Function Table:

S1	S0	INPUTS Y
0	0	D0 → D0 S1' S0'
0	1	D1 → D1 S1' S0
1	0	D2 → D2 S1 S0'
1	1	D3 → D3 S1 S0

$$Y = D0\ S1'\ S0' + D1\ S1'\ S0 + D2\ S1\ S0' + D3\ S1\ S0$$

Block Diagram for 1:4 Demultiplexers:

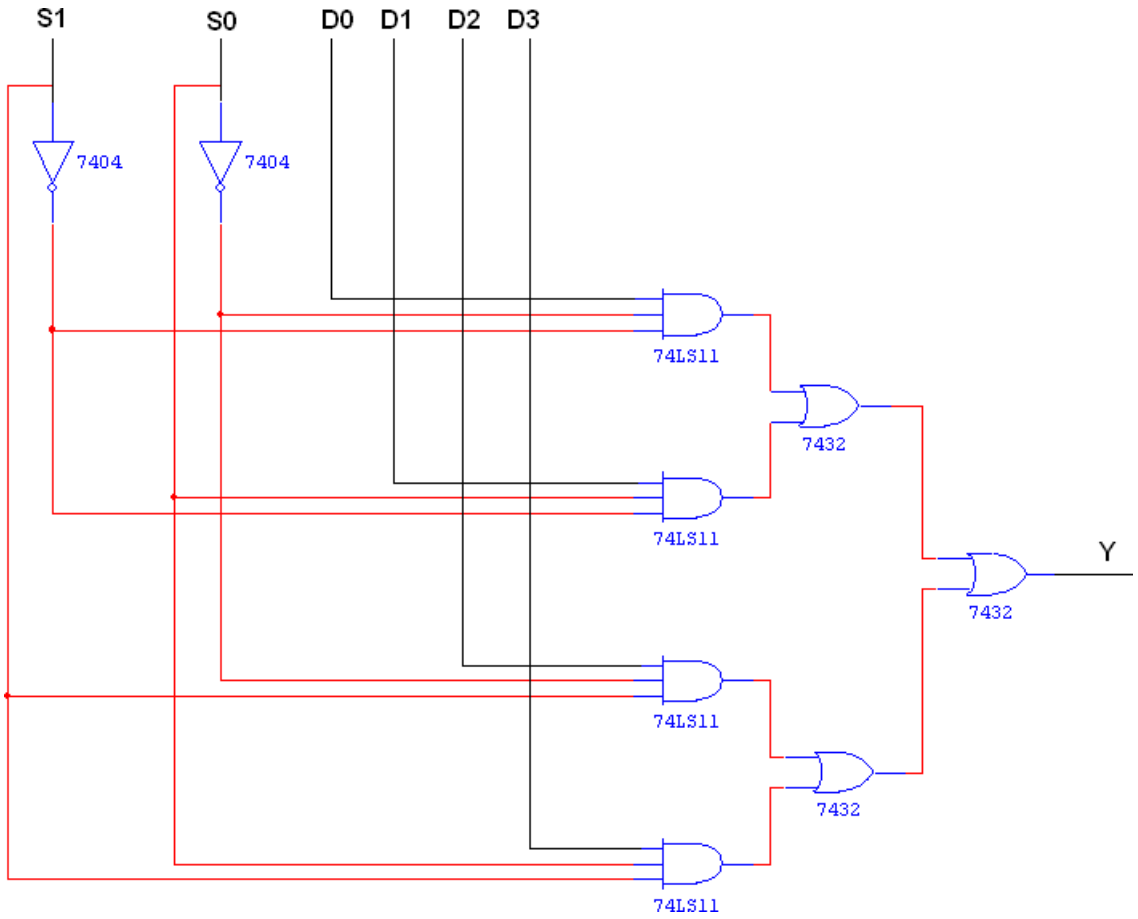


Function Table:

S1	S0	INPUT
0	0	X → D0 = X S1' S0'
0	1	X → D1 = X S1' S0
1	0	X → D2 = X S1 S0'
1	1	X → D3 = X S1 S0

Y = X S1' S0' + X S1' S0 + X S1 S0' + X S1 S0

Circuit Diagram For Multiplexer:

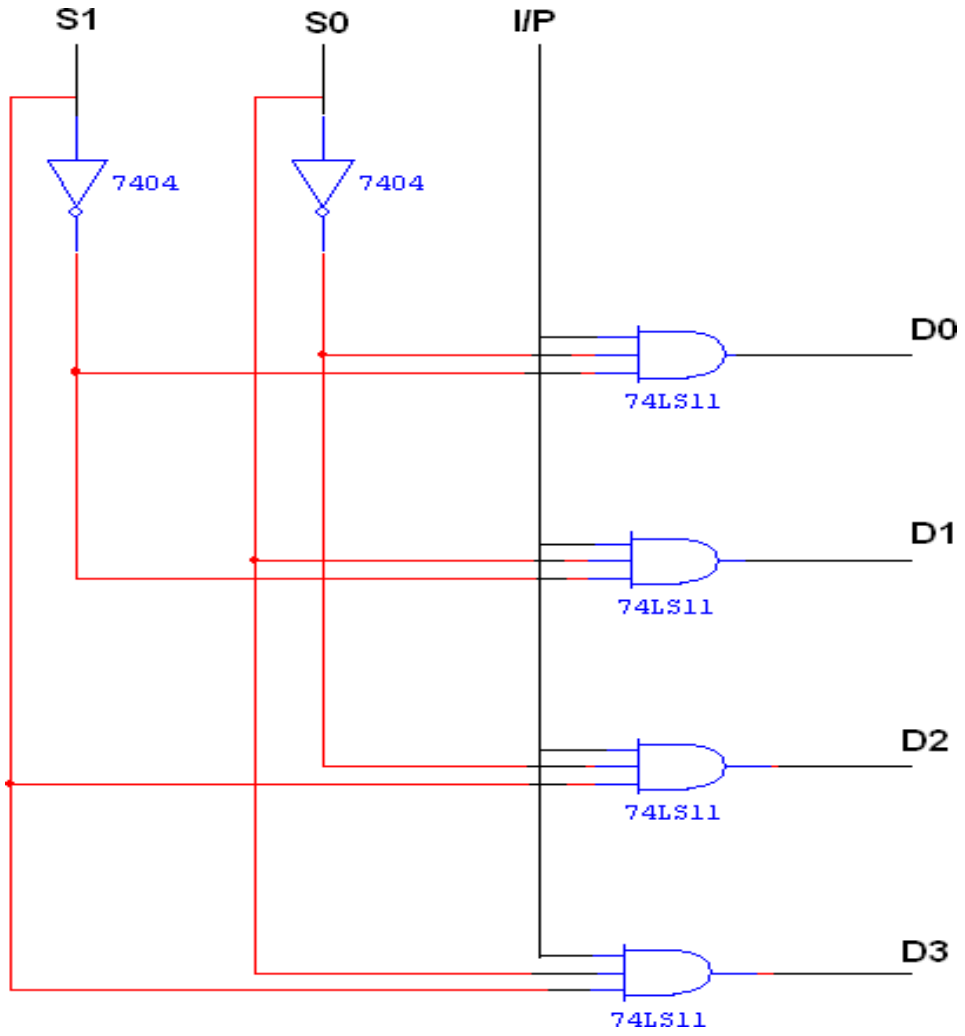


Truth Table:

S 1	S0	Y = OUTPUT
0	0	D0
0	1	D1
1	0	D2

1	1	D3

Logic Diagram for Demultiplexer:



Truth Table:

INPUT			OUTPUT			
S1	S0	I/P	D0	D1	D2	D3
0	0	0	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	1	0	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	1	0
1	1	0	0	0	0	0
1	1	1	0	0	0	1

Procedure:

(i) Make the connections as per circuit diagram.

(ii) Apply logical inputs as per truth table.

(iii) Observe the logical output and verify with the truth tables.

Result:

Thus the design and implementation of multiplexer and demultiplexer using logic gates were done.

Outcomes:

Able to understand the concept, realize and implement the 4-bit adder / Subtractor and BCD adder.

Practical Applications

Applications of Multiplexers

A Multiplexer is used in various applications wherein multiple data can be transmitted using a single line.

1. Communication System - A Multiplexer is used in communication systems, which has a transmission system and also a communication network. A Multiplexer is used to increase the efficiency of the communication system by allowing the transmission of data, such as audio & video data from different channels via cables and single lines.
2. Computer Memory - A Multiplexer is used in computer memory to keep up a vast amount of memory in the computers, and also to decrease the number of copper lines necessary to connect the memory to other parts of the computer.
3. Telephone Network - A multiplexer is used in telephone networks to integrate the multiple audio signals on a single line of transmission.

Applications of Demultiplexer

Demultiplexers are used to connect a single source to multiple destinations. These applications include the following:

1. **Communication System** - Multiplexer and Demultiplexer both are used in communication systems to carry out the process of data transmission. A De-multiplexer receives the output signals from the multiplexer; and, at the receiver end, it converts them back to the original form.
2. **Arithmetic Logic Unit** - The output of the arithmetic logic unit is fed as an input to the De-multiplexer, andthe o/p of the demultiplexer is connected to a multiple registers. The output of the ALU can be stored in multiple registers.
3. **Serial to Parallel Converter** - The serial to parallel converter is used to reform parallel data. In this method, serial data are given as an input to the De-multiplexer at a regular interval, and a counter is attached to the demultiplexer at the control i/p to sense the data signal at the demultiplexer's o/p. When all data signals are stored, the output of the demultiplexer can be read out in parallel.

Viva – voce

1. What are the advantages of Multiplexer?
2. Realize the Truth-table of Multiplexer?
3. What is the difference between Multiplexer and Demultiplexer?
4. What is combinational circuit?
5. Most demultiplexers facilitate which type of conversion?
6. How the inputs/outputs of an analog multiplexer/demultiplexer are said to be bidirectional?
7. What is the function of an enable input on a multiplexer chip?
8. State few application of a digital multiplexer.
9. Why is a demultiplexer called a data distributor?
10. How many exclusive-NOR gates would be required for an 8-bit comparator circuit?
11. What is the status of the inputs S_0, S_1, and S_2 of the 74151 eight-line multiplexer in order for the output Y to be a copy of input I_5?
12. How many select lines would be required for an 8-line-to-1-line multiplexer? 3
13. Which device has one input and many outputs?
14. How many select lines are required for a 4 : 1 multiplexer requires?
15. Give few applications of multiplexer.
16. Give few applications of demultiplexer.

Expt. No. 13 DESIGN AND IMPLEMENTATION OF ENCODER AND DECODER

Aim:

To design and implement encoder and decoder using logic gates

Apparatus Required:

Sl.No.	Component	Specification	Qty.
1.	3 I/P NAND Gate	IC 7410	2
2.	OR Gate	IC 7432	3
3.	NOT Gate	IC 7404	1
2.	IC Trainer Kit	-	1
3.	Patch Cords	-	27

Theory:

Encoder**:**

An encoder is a digital circuit that performs inverse operation of a decoder. An encoder has 2^n input lines and n output lines. In encoder the output lines generates the binary code corresponding to the input value. In octal to binary encoder it has eight inputs, one for each octal digit and three output that generate the corresponding binary code. In encoder it is assumed that only one input has a value of one at any given time otherwise the circuit is meaningless. It has an ambiguila that when all inputs are zero the outputs are zero. The zero outputs can also be generated when D0 = 1.

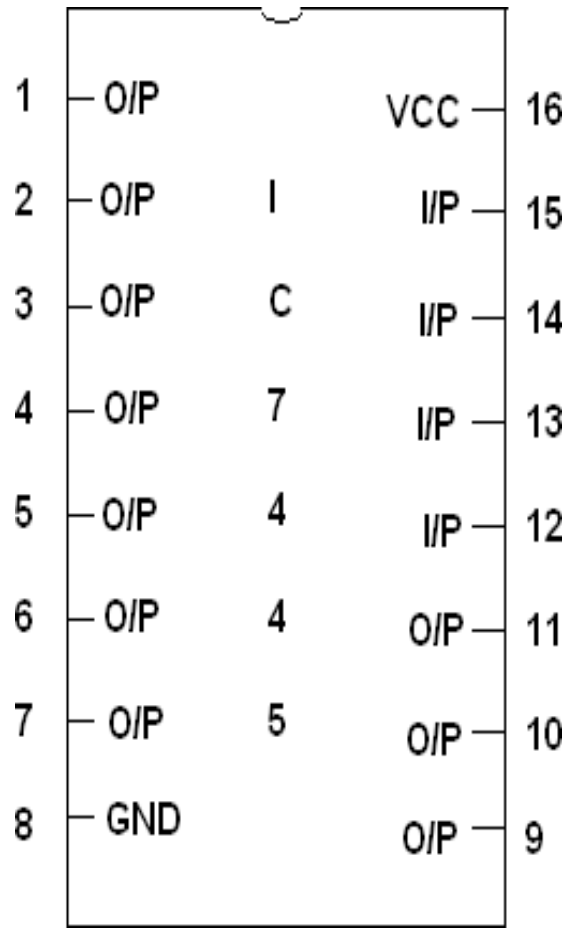
Decoder:

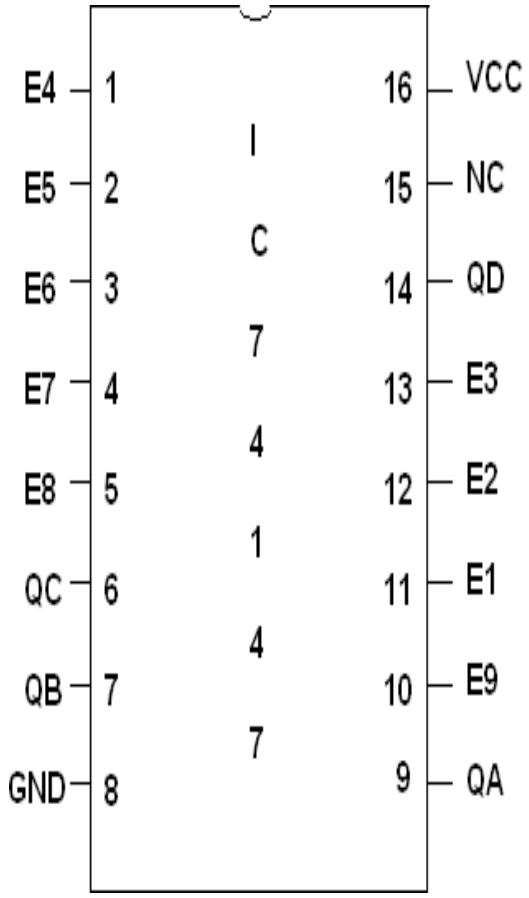
A decoder is a multiple input multiple output logic circuits which converts coded input into coded output where input and output codes are different. The input code generally has fewer bits than the output code. Each input code word produces a different output code word i.e there is one to one mapping can be expressed in truth table. In the block diagram of decoder circuit the encoded information is present as n input producing 2^n possible outputs. 2^n output values are from 0 through out $2^n - 1$.

PIN Diagram for IC 7445:

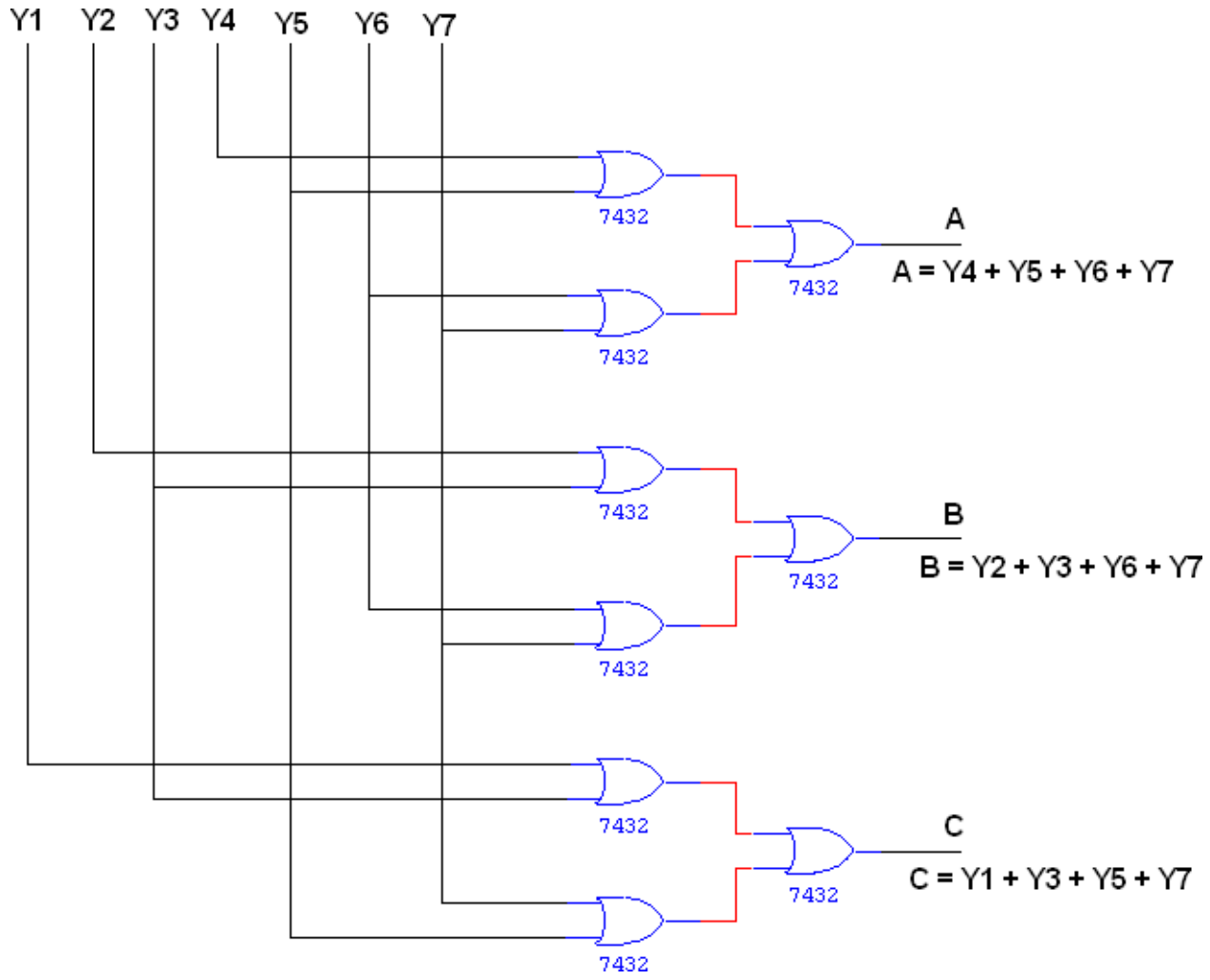
PIN Diagram for IC 74147:

BCD to Decimal Decoder:





Logic Diagram for Encoder:

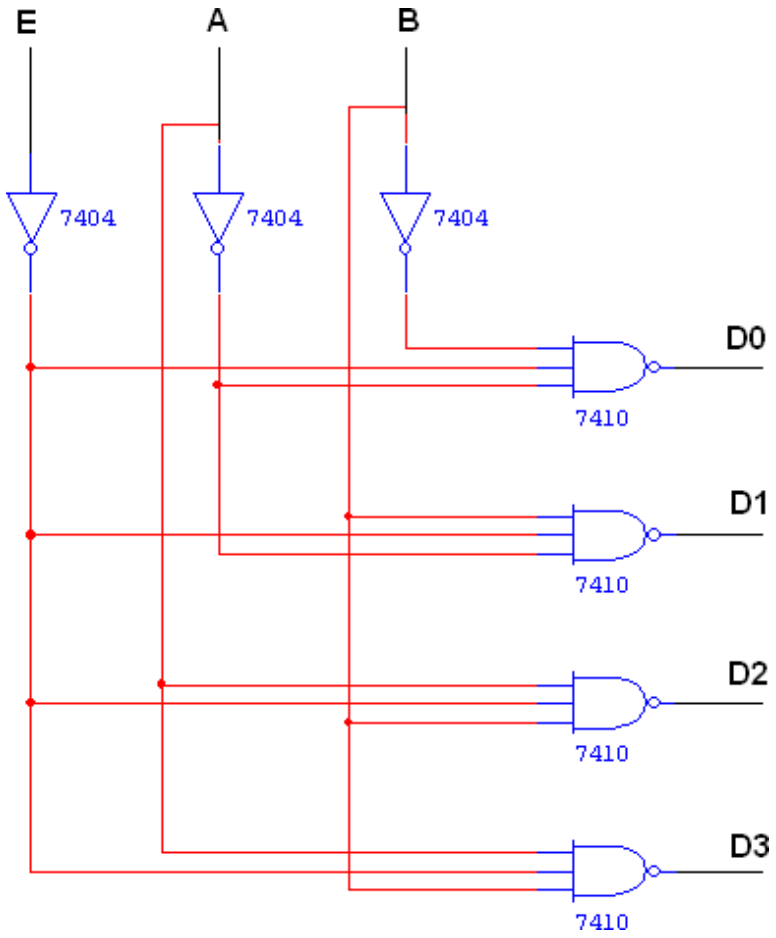


Truth Table:

INPUT							OUTPUT		
Y1	Y2	Y3	Y4	Y5	Y6	Y7	A	B	C
1	0	0	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	1	1
0	0	0	1	0	0	0	1	0	0

0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	1	1	1	1

Logic Diagram for Decoder:



Truth Table:

INPUT			OUTPUT			
E	A	B	D0	D1	D2	D3

1	0	0	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

Procedure:

(i) Make the connections as per circuit diagram.

(ii) Apply logical inputs as per truth table.

(iii) Observe the logical output and verify with the truth tables.

Result:

Thus the encoder and decoder using logic gates were designed.

Outcomes:

Able to understand the concept, realize and implement the encoder and decoder using logic gates.

Practical Applications

1. Data privacy and security
2. Data communication
3. Data compression
4. QR code
5. War field flying robot with a night vision flying camera
6. Robotic vehicle with the metal detector
7. RF based home automation system

Viva – voce

1. What is combinational circuit?
2. What are encoder and the decoder?
3. State any two applications of encoder and decoder.
4. How is an encoder different from a decoder? The output of an encoder is a binary code for 1-of-N input.
5. Design a 3:6 decoder.
6. A BCD decoder will have how many rows in its truth table?
7. How many possible outputs would a decoder have with a 6-bit binary input?
8. How many outputs are on a BCD decoder?
9. Which digital system translates coded characters into a more useful form?
10. How many inputs will a decimal-to-BCD encoder have?
11. What control signals may be necessary to operate a 1-line-to-16 line decoder?
12. How many inputs are required for a 1-of-10 BCD decoder?
13. What is the name of the process when two or more inputs are active simultaneously?
14. How many outputs are on a BCD decoder?
15. How many inputs are required for a 1-of-16 decoder?
16. Give some applications of decoder.
17. Give some applications of encoder.
18. What is the difference between a decoder and a demultiplexer?
19. Give the steps involved in designing a decder.

Expt. No. 14

CONSTRUCTIONS AND VERIFICATION OF 4 BIT RIPPLE COUNTER AND MOD-10/ MOD-12 RIPPLE COUNTERS

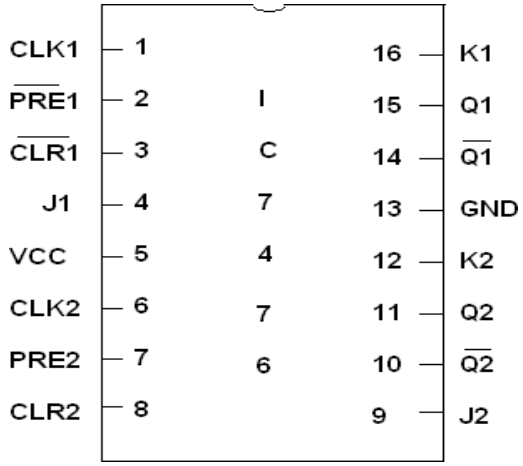
Apparatus Required:

Sl.No.	Component	Specification	Qty.
1.	JK FLIP FLOP	IC 7476	2
2.	NAND GATE	IC 7400	1
3.	IC TRAINER KIT	-	1
4.	PATCH CORDS	-	30

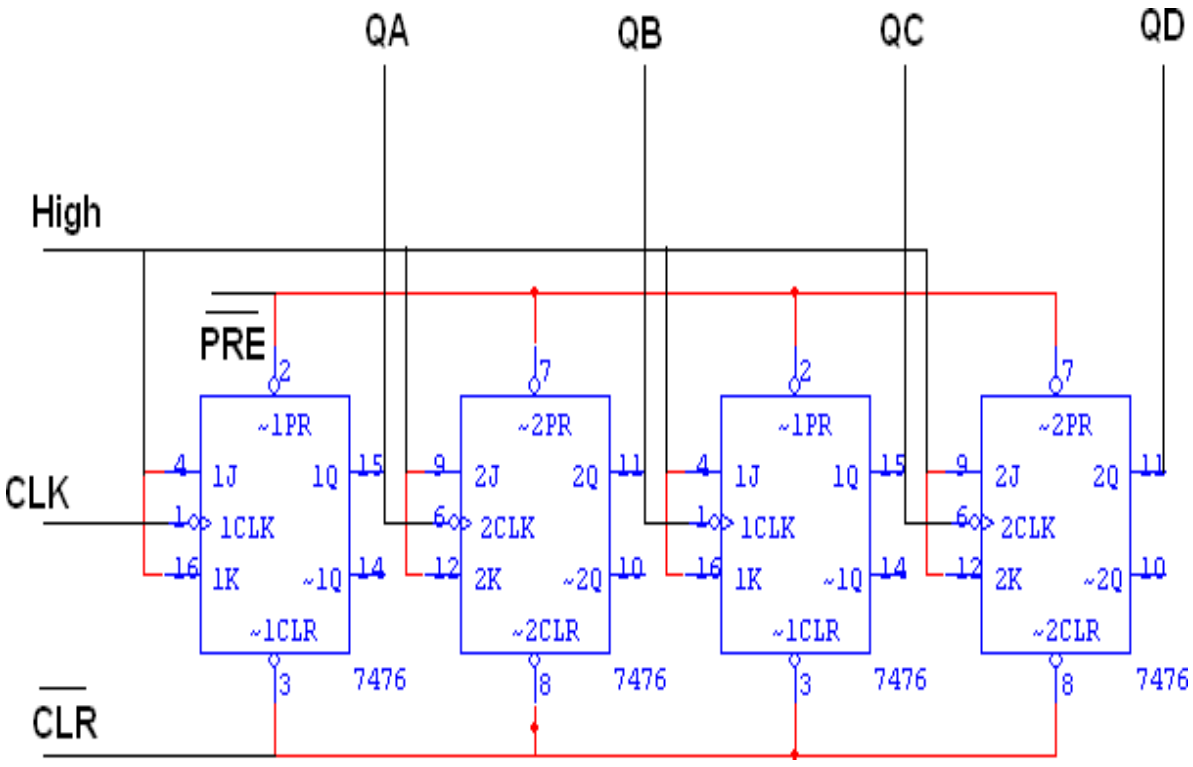
Theory:

A counter is a register capable of counting number of clock pulse arriving at its clock input. Counter represents the number of clock pulses arrived. A specified sequence of states appears as counter output. This is the main difference between aregister and a counter. There are two types of counter, synchronous and asynchronous. In synchronous common clock is given to all flip flop and inasynchronous first flip flop is clocked by external pulse and then each successive flip flop is clocked by $\overline{Q}$ or Q output of previous stage. A soon the clock of second stage is triggered by output of first stage. Because of inherent propagation delay time all flip flops are not activated at same time which results in asynchronous operation.

PIN Diagram for IC 7476:



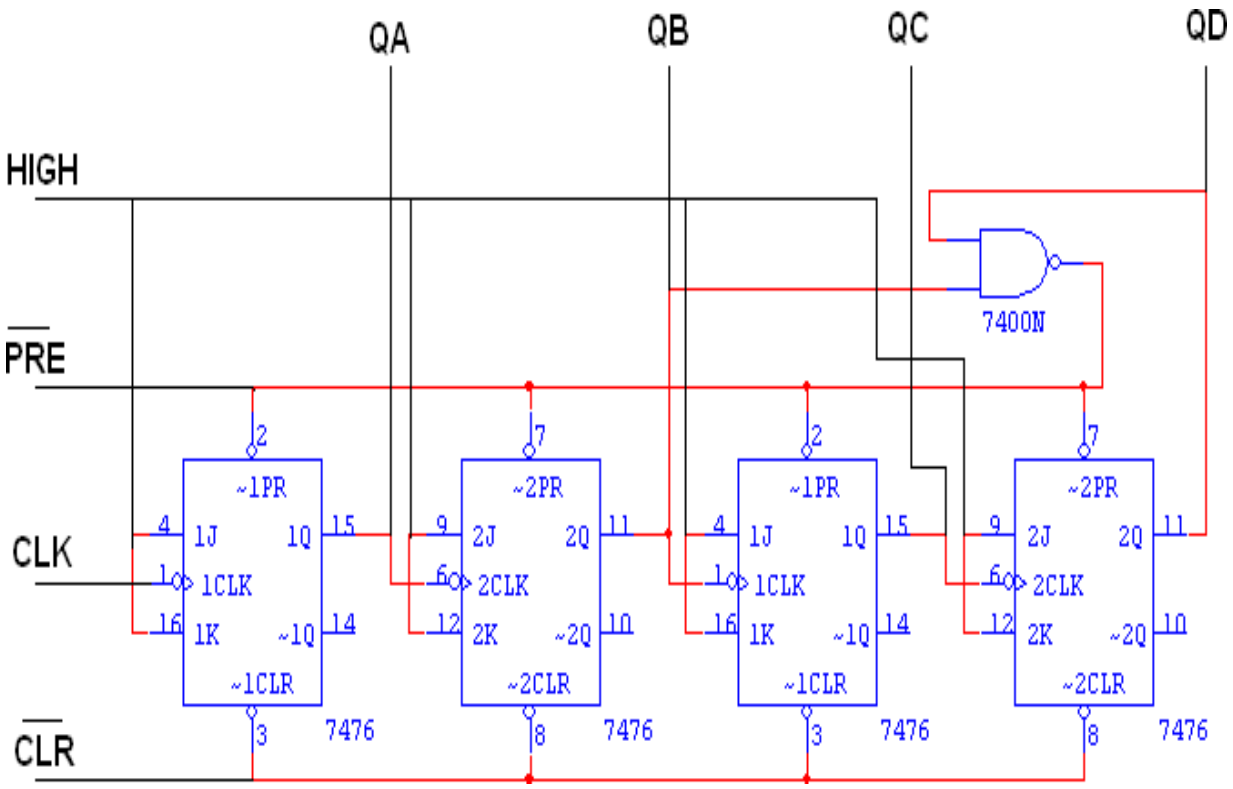
Logic Diagram for 4 Bit Ripple Counter:



Truth Table:

CLK	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

Logic Diagram for Mod - 10 Ripple Counter:

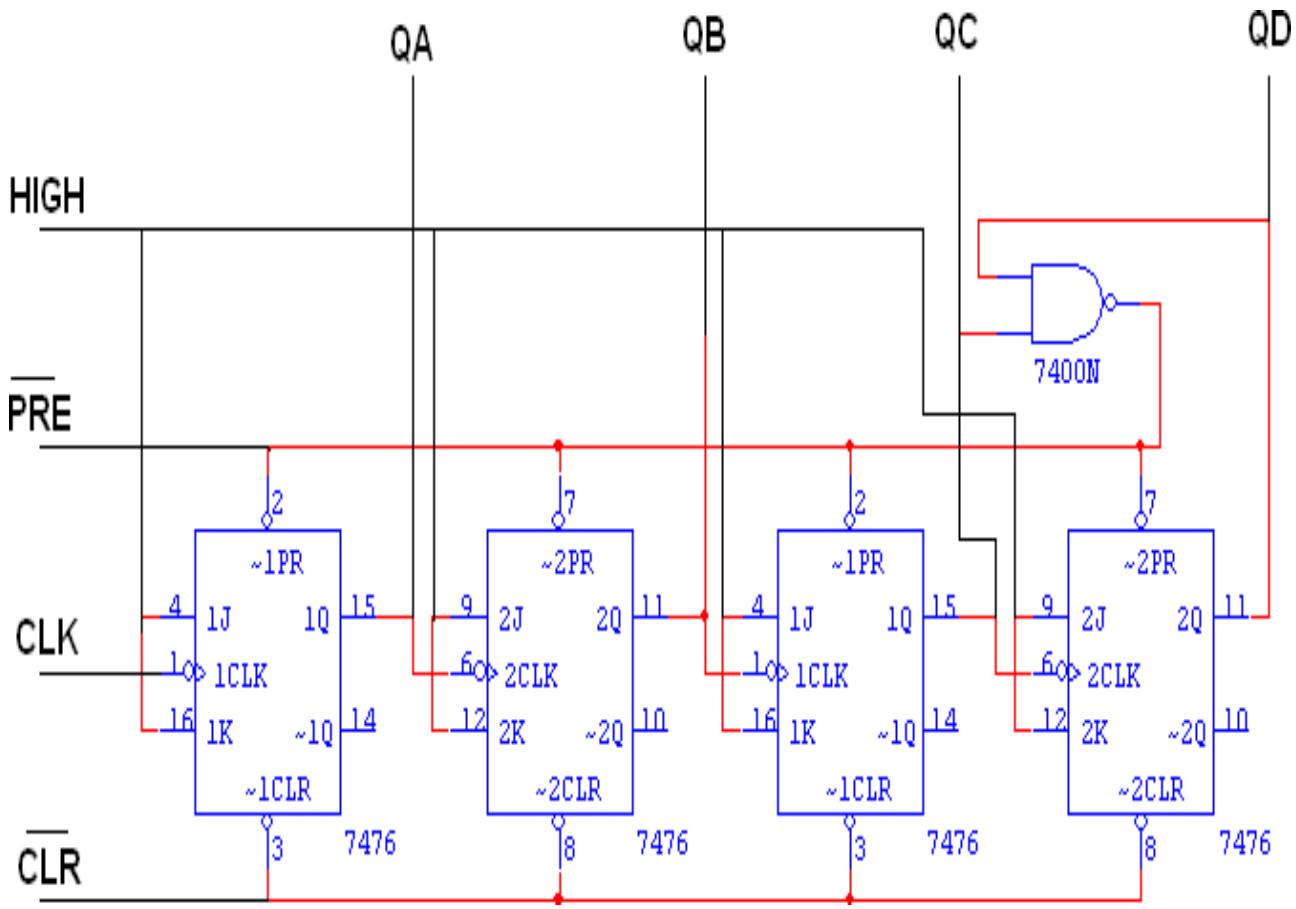


Truth Table:

CLK	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

10	0	0	0	0

Logic Diagram for Mod - 12 Ripple Counter:



Truth Table:

CLK	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0

5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	0	0

Procedure:

(i) Make the connections as per circuit diagram.

(ii) Apply logical inputs as per truth table.

(iii) Observe the logical output and verify with the truth tables.

Result:

Thus the 4 bit ripple counter mod 10/ mod 12 ripple counters was implemented and the truth table were verified.

Outcomes:

Able to understand the concept, realize and implement the 10/mod 12 ripple counters.

Practical Applications

Viva – voce

1. Define – Sequential Circuit.
2. What is the difference between latch and flip-flop?
3. What are the disadvantages of S-R Flip-Flop?
4. How can you convert the JK Flip-flop to a D Flip-flop?
5. Name two sequential switching circuits.
6. How many flip-flops are required to build a binary counter that counts 0 to 1023?
7. If the counter is initially at zero, what count it will hold after 2060 clock pulses?
8. Determine the frequency at the output of last(MSB) flip-flop for an input clock frequency of 2 MHz.
9. List the types of counters.
10. Distinguish between asynchronous and synchronous counters.
11. What is meant by ripple counter?

12. What is meant by modulo counter?
13. Define – Flip Flop
14. What are the different types of flip- flop?
15. What is the operation of RS flip-flop?
16. What is the operation of SR flip-flop?
17. What is the operation of D flip- flop?
18. What do you mean by present state and next state?
19. What are the types of sequential circuits?

Expt. No. 15 DESIGN AND IMPLEMENTATION OF 3-BIT SYNCHRONOUS UP/DOWN COUNTER

Aim:

To design and implement 3 bit synchronous up/down counter.

Apparatus Required:

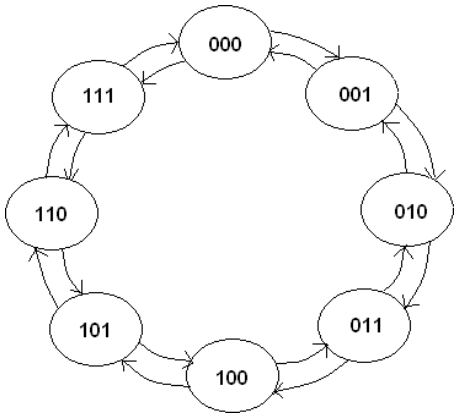
Sl.No.	Component	Specification	Qty.
1.	JK FLIP FLOP	IC 7476	2
2.	3 I/P AND GATE	IC 7411	1
3.	OR GATE	IC 7432	1
4.	XOR GATE	IC 7486	1
5.	NOT GATE	IC 7404	1
6.	IC TRAINER KIT	-	1
7.	PATCH CORDS	-	35

Theory:

A counter is a register capable of counting number of clock pulse arriving at its clock input. Counter represents the number of clock pulses arrived. An up/down counter is one that is capable of progressing in increasing order or decreasing order through a certain sequence. An up/down counter is also called bidirectional counter. Usually up/down operation of the counter is controlled by up/down signal. When this signal is high counter goes through up sequence and when up/down signal is low counter follows reverse sequence.

Design:

State Diagram:

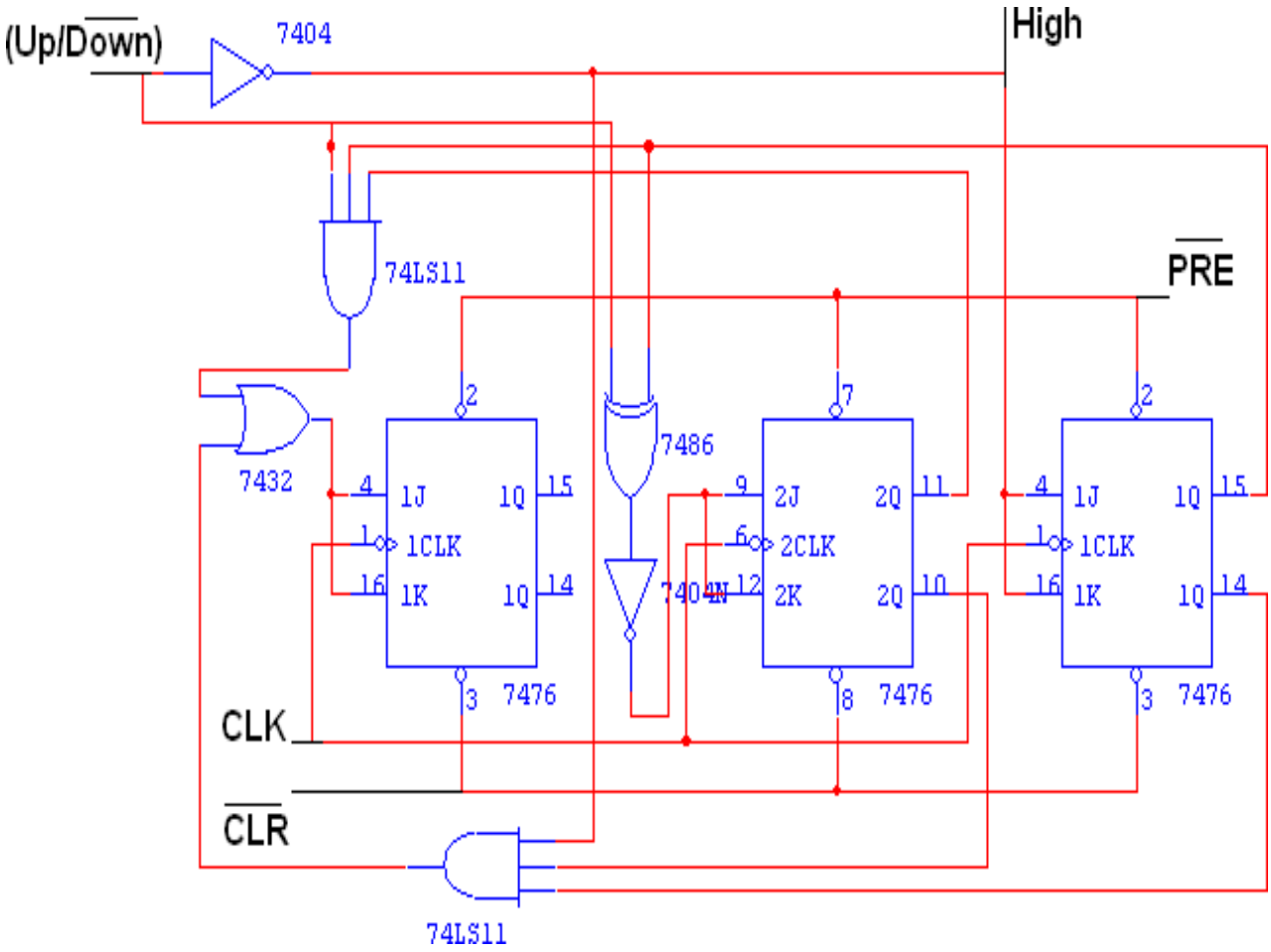


Truth Table:

Input Up/Down	Present State			Next State			A		B		C	
	Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	1	1	1	1	X	1	X	1	X
0	1	1	1	1	1	0	X	0	X	0	X	1
0	1	1	0	1	0	1	X	0	X	1	1	X
0	1	0	1	1	0	0	X	0	0	X	X	1
0	1	0	0	0	1	1	X	1	1	X	1	X
0	0	1	1	0	1	0	0	X	X	0	X	1

0	0	1	0	0	0	1	0	X	X	1	1	X
0	0	0	1	0	0	0	0	X	0	X	X	1
1	0	0	0	0	0	1	0	X	0	X	1	X
1	0	0	1	0	1	0	0	X	1	X	X	1
1	0	1	0	0	1	1	0	X	X	0	1	X
1	0	1	1	1	0	0	1	X	X	1	X	1
1	1	0	0	1	0	1	X	0	0	X	1	X
1	1	0	1	1	1	0	X	0	1	X	X	1
1	1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	1	0	0	0	X	1	X	1	X	1

Logic Diagram:



Procedure:

(i) Make the connections as per circuit diagram.

(ii) Apply logical inputs as per truth table.

(iii) Observe the logical output and verify with the truth tables.

Result:

Thus the design and implementation of 3 bit synchronous up/down counter were done.

Outcomes:

Able to understand the concept, realize and implement the 3 bit synchronous up/down counter.

Viva – voce

1.Difference between Synchronous and Asynchronous counter.

2.What is difference between latch and flip-flop?

chronous counter?5.What is meant by

3. What is Johnson counter?

synchronous counter? 6.What is

meant by up counter?

7. What is meant by down counter?

8. What is the primary disadvantage of an asynchronous

counter?9.Define –Master Slave Flip Flop

10. Draw the state diagram of 'T' FF, 'D' FF
11. Define – Counter
12. What is the primary disadvantage of an asynchronous counter?
13. How synchronous counters differ from asynchronous counters?
14. Give some applications of on counter.
15. Compare Moore and Mealy models
16. What is up counter?
17. What is down counter?

4. What is meant by asyn

16.DESIGN AND IMPLEMENTATION OF SHIFT REGISTER

To design and implement

(i) Serial in serial out
(ii) Serial in parallel out
(iii) Parallel in serial out
(iv) Parallel in parallel out

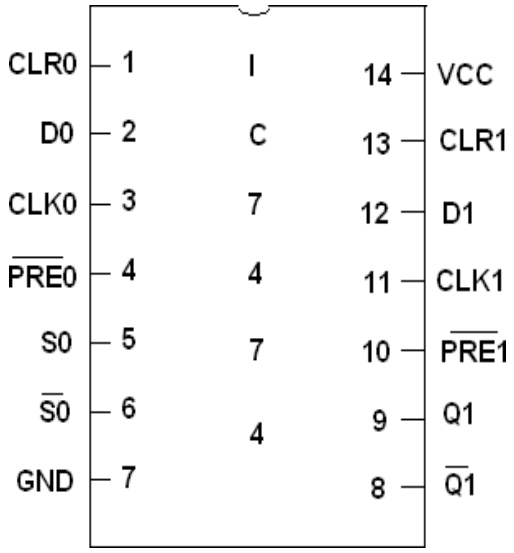
Apparatus Required:

Sl.No.	COMPONENT	SPECIFICATION	QTY.
1.	D FLIP FLOP	IC 7474	2
2.	OR GATE	IC 7432	1
3.	IC TRAINER KIT	-	1
4.	PATCH CORDS	-	35

Theory:

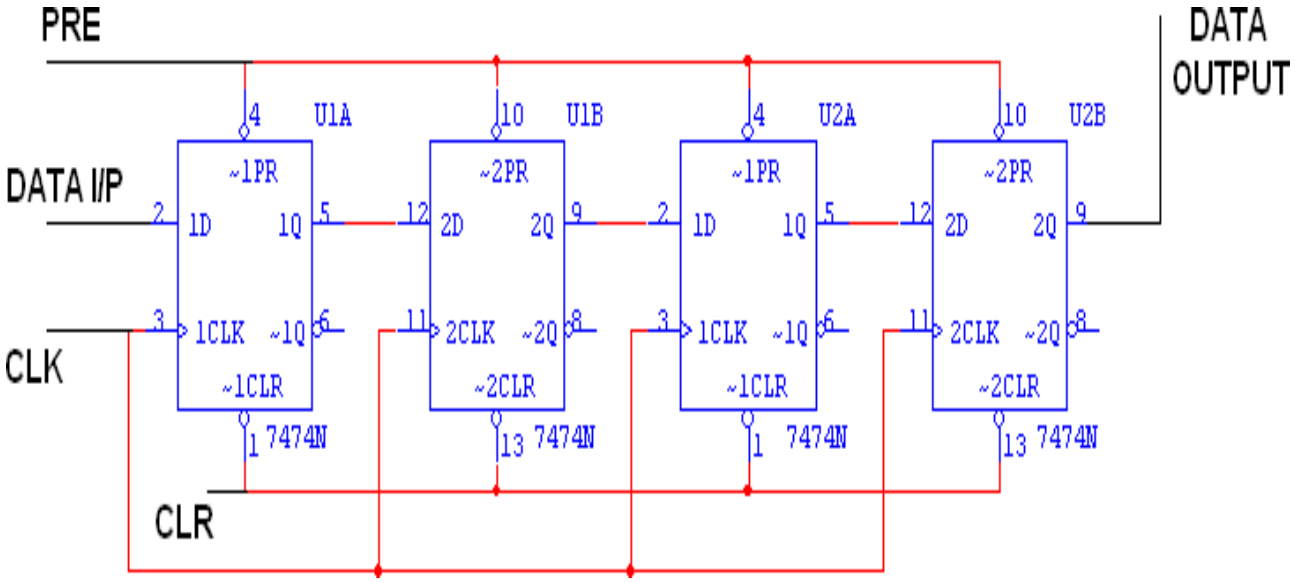
A register is capable of shifting its binary information in one or both directions is known as shift register. The logical configuration of shift register consist of a D-Flip flop cascaded with output of one flip flop connected to input of next flip flop. All flip flops receive common clock pulses which causes the shift in the output of the flip flop.The simplest possible shift register is one that uses only flip flop. The output of a given flip flop is connected to the input of next flip flopof the register. Each clock pulse shifts the content of register one bit position to right.

Pin Diagram:



Logic Diagram:

SERIAL IN SERIAL OUT:

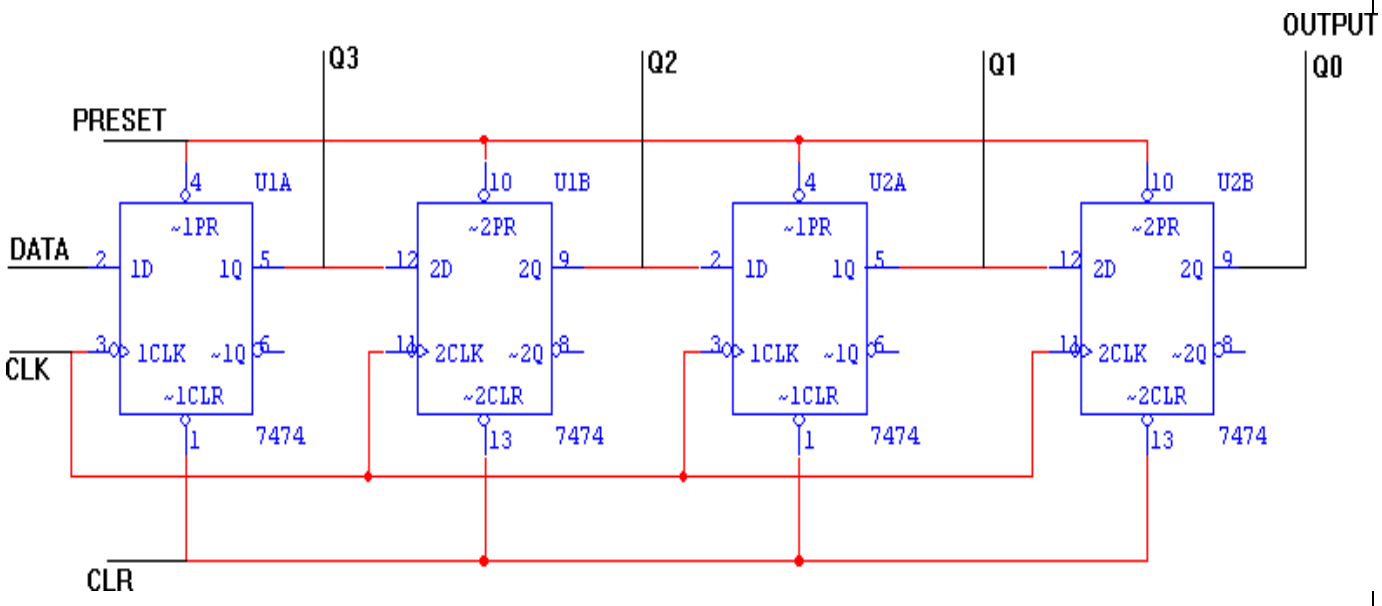


Truth Table:

CLK	Serial in	Serial out
1	1	0
2	0	0
3	0	0
4	1	1
5	X	0
6	X	0
7	X	1

Logic Diagram:

SERIAL IN PARALLEL OUT:

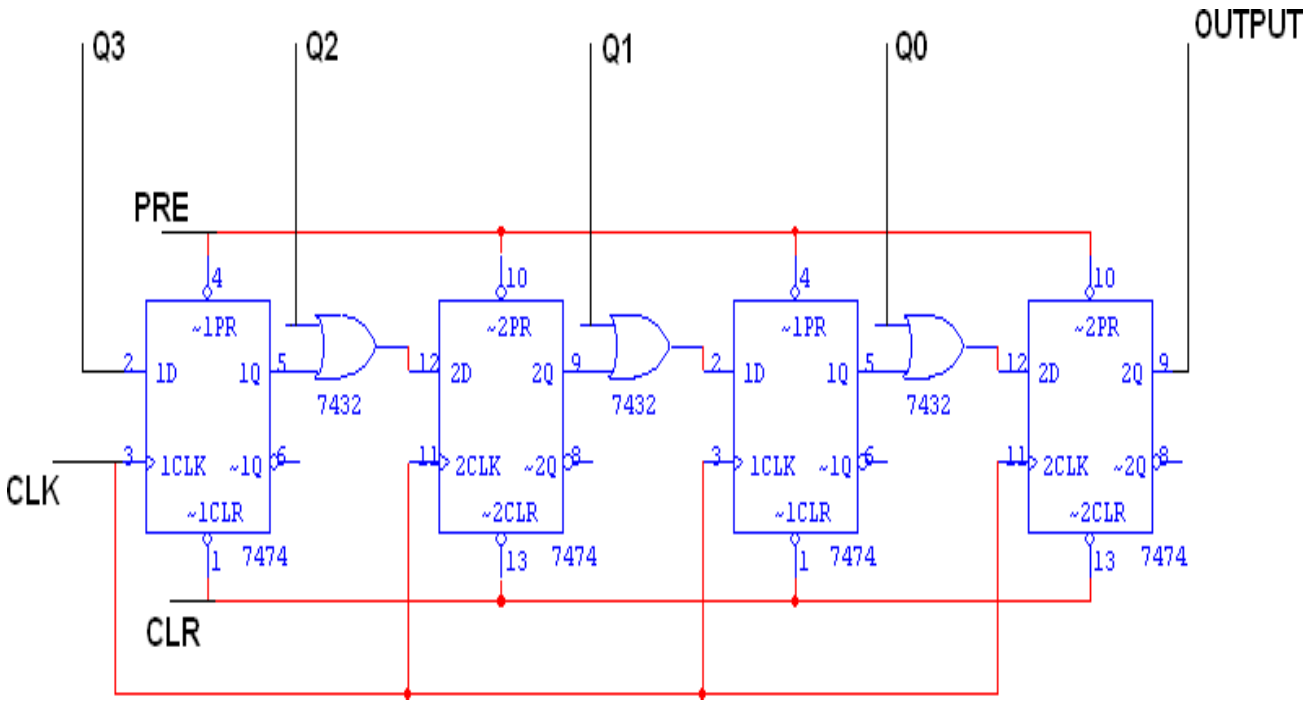


Truth Table:

CLK	DATA	OUTPUT			
		Q_A	Q_B	Q_C	Q_D
1	1	1	0	0	0
2	0	0	1	0	0
3	0	0	0	1	1
4	1	1	0	0	1

Logic Diagram:

PARALLEL IN SERIAL OUT:

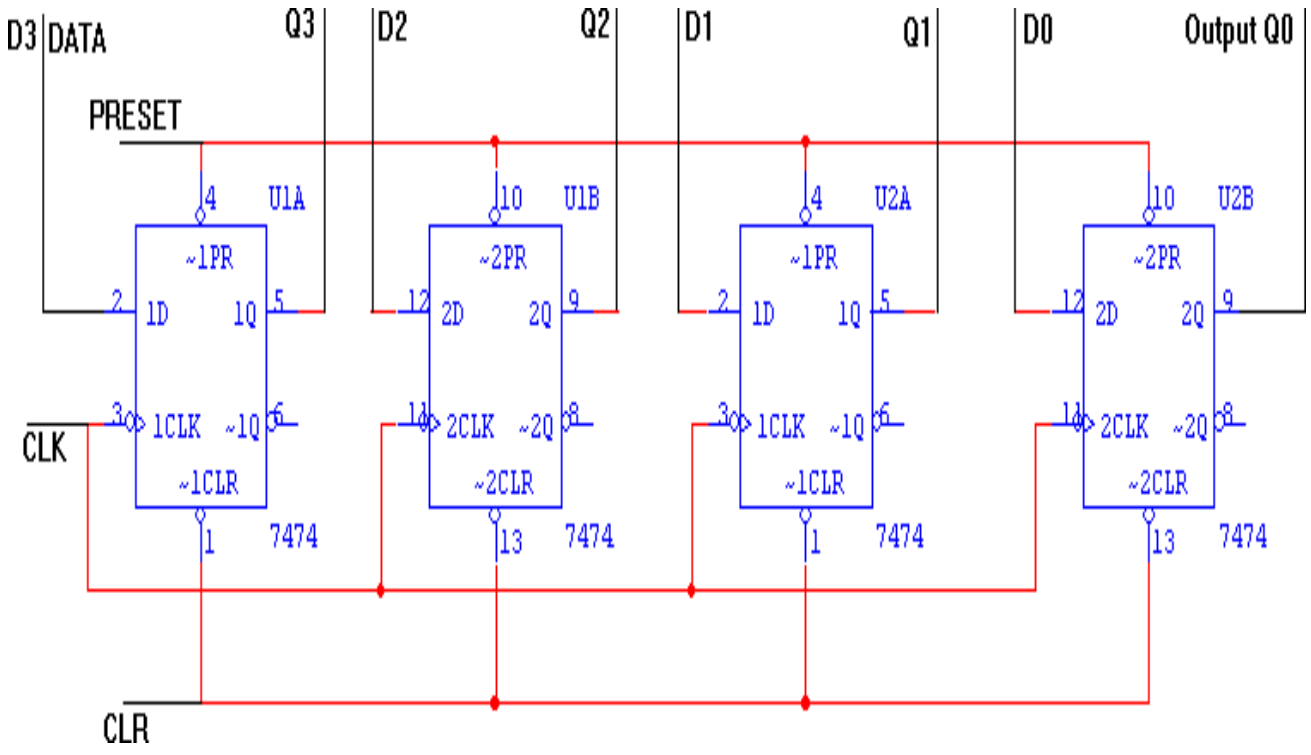


Truth Table:

CLK	Q3	Q2	Q1	Q0	O/P
0	1	0	0	1	1
1	0	0	0	0	0
2	0	0	0	0	0
3	0	0	0	0	1

Logic Diagram:

PARALLEL IN PARALLEL OUT:



Truth Table:

CLK	DATA INPUT				OUTPUT			
	D_A	D_B	D_C	D_D	Q_A	Q_B	Q_C	Q_D
1	1	0	0	1	1	0	0	1
2	1	0	1	0	1	0	1	0

A register capable of shifting its binary information in one or both directions is known as shift register. The logical configuration of shift register consist of a D-Flip flop cascaded with output of one flip flop connected to input of next flip flop. All flip flops receive common clock pulses which causes the shift in the output of the flip flop. The simplest possible shift register is one that uses only flip flop. The output of a given flip flop is connected to the input of next flip flop of the register. Each clock pulse shifts the content of register one bit position to the right.

Procedure:

(i) Make the connections as per circuit diagram.

(ii) Apply logical inputs as per truth table.

(iii) Observe the logical output and verify with the truth tables.

Result:

Thus the design and implementation of shift register were done.

Outcomes:

Able to understand the concept, realize and implement the shift register.

Viva – voce

1. What is a shift register?
2. What are the disadvantages of S-R Flip-Flop?
3. How many inputs and outputs are obtained for a 4 - bit serial in parallel out shift register?
4. How many flip -flops are needed to build an 8 bit shift register?
5. How will you complement of the counters of the register.

6. List the basic types of shift registers in terms of data movement.
7. What are the advantages of shift registers?
8. What are the types of shift register?
9. For realizing a 8-bit SISO shift register using flip-flops what is the minimum number of flip-flops required?
10. A serial in/parallel out, 4-bit shift register initially contains all 1s. The data nibble 0111 is waiting to enter. After four clock pulses, what does the register contains?
11. What is a shift register that will accept a parallel input, or a bidirectional serial load and internal shift features, called?
12. How can parallel data be taken out of a shift register simultaneously?
13. What is meant by parallel load of a shift register?
14. What are the Q outputs after four clock pulses? If the bit sequence 10011100 is serially entered (right-most bit first) into an 8-bit parallel out shift register that is initially clear.
15. What is a re-circulating register?
16.

Expt. No. 17 STUDY OF OP-AMP IC741

Aim:

To study the working principle of Op-Amp IC741

Theory:

Introduction:

The term operational amplifier or "op-amp" refers to a class of high-gain DC coupled amplifiers with two inputs and a single output. The modern integrated op-amp. Some of the general characteristics of the IC version are:

- High gain, on the order of a million
- High input impedance, low output impedance AN
- Used with split supply, usually +/- 15V
- Used with feedback, with gain determined by the feedback network.

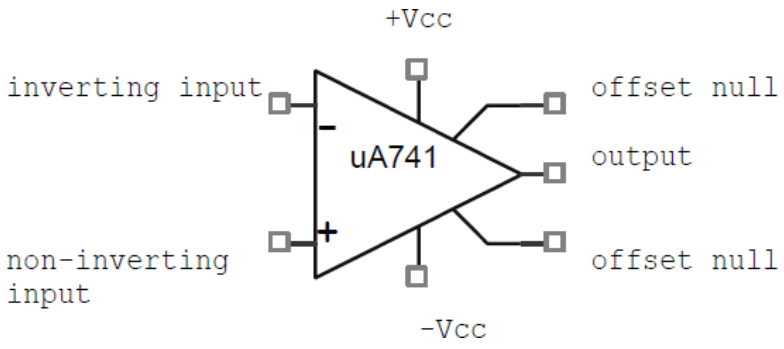
Op-amps can perform mathematical operations like summation integration, differentiation, logarithm, anti-logarithm, etc., and hence the name operational amplifier op-amps are also used as video and audio amplifiers, oscillators and so on, in communication electronics, in instrumentation and control, in medical electronics, etc.

Op-Amp IC741:

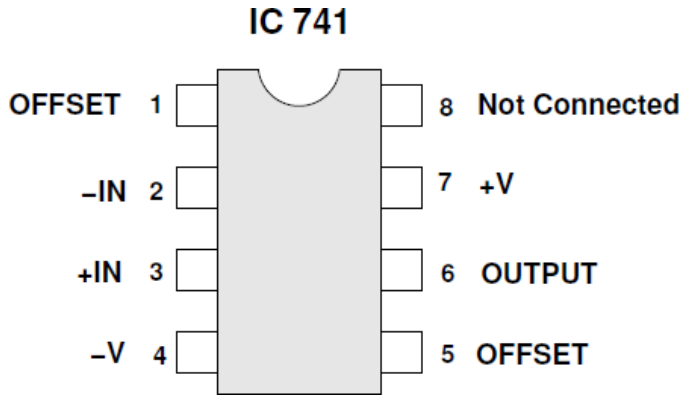
Circuit symbol and op-amp terminals:

The circuit schematic of an op-amp is a triangle as shown in figure and it has two input terminal. The minus input, marked (-) is the inverting input. A signal applied to the minus terminal will be shifted in phase 180° at the output. The plus input, marked (+) is the non-inverting input. A signal applied to the plus terminal will appear in the same phase at the output as at the input. +VCC denotes the positive and negative power supplies. Most op- amps operate with a wide range of supply voltages. A dual power supply of +15V is quite common in practical op- amp circuits. The use of the positive and negative supply voltages allows the output of the op-amp to swing inboth positive and negative directions.

Circuit symbol:



IC741 Pin Configuration:

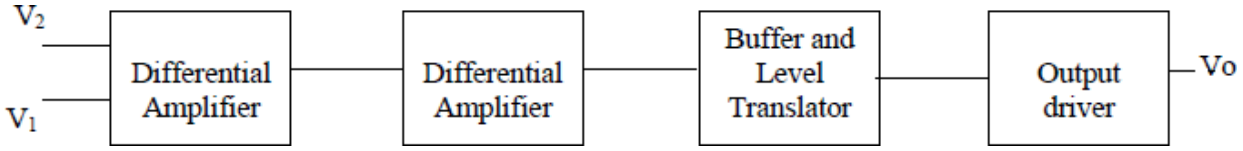


Internal Block Diagram:

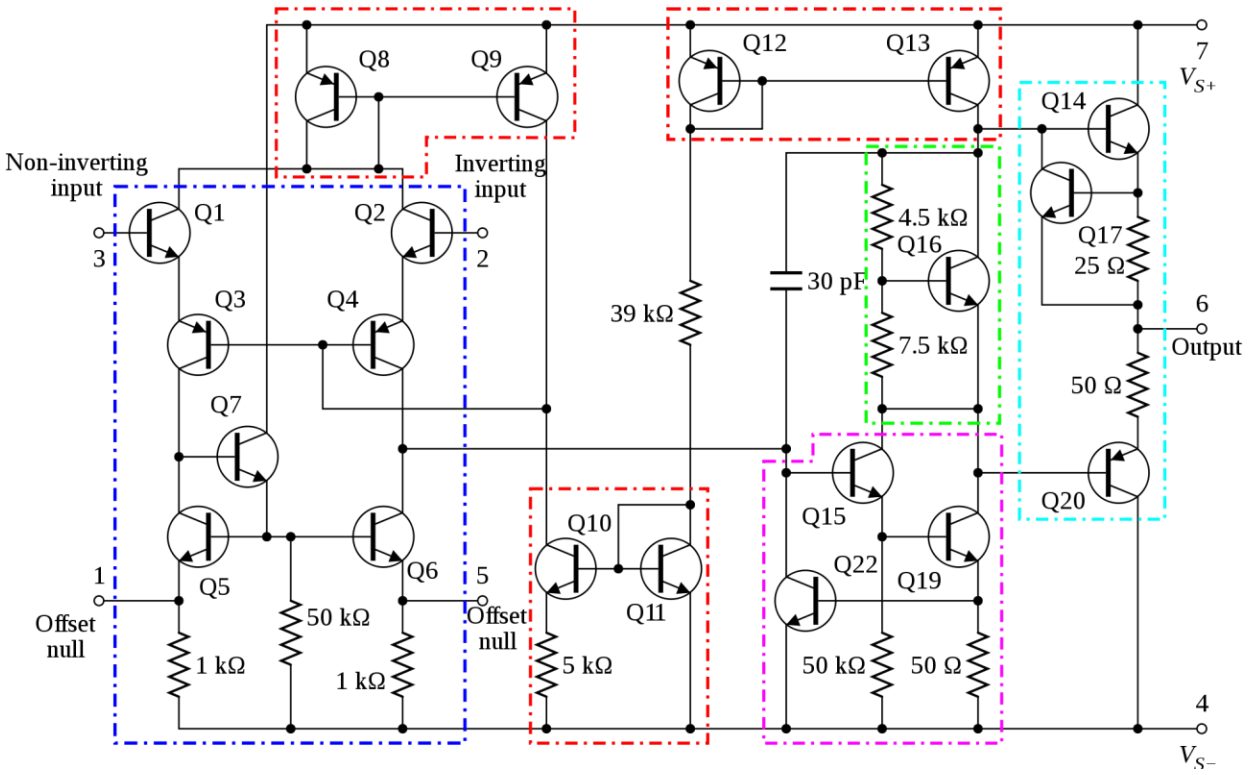
Commercial integrated circuit OP-amps usually consists of your cascaded blocks as shown in figure.

1. Input Stage:
    - Dual input, Balanced output Differential amplifier
    - Provides - High voltage gain and input resistance of Op-Amp
2. Intermediate Stage:
    - Dual input, Unbalanced output Differential amplifier
    - Drives the output of first stage
    - Direct coupling
3. Level Translator or Shifting Stage:
    - DC voltage level to zero with respect to ground
4. Output Stage:
    - Increase output voltage swing
    - Raises current supply capability of Op-Amp
    - Provides - Low resistance

The first two stages are cascaded difference amplifier used to provide high gain. The third stage is a buffer and the last stage is the output driver. The buffer is usually an emitter following whose input impedance is very high so that it prevents loading of the high gain stage. The output stage is designed to provide low output impedance. The buffer stage along with the output stage also acts as a level shifter so that output voltage is zero for zero inputs.



Functional Block Diagram:



Op-Amp Characteristics:

An ideal op-amp draws no current from the source and its response is also independent of temperature. However, a real op-amp does not work this way. Current is taken from the source into op-amp inputs. Also the two inputs respond differently to current and voltage due to mismatch in transistors. A real op-amp also shifts its operation with temperature. These non-ideal characteristics are:

1. Input bias current
2. Input offset current
3. Input offset voltage
4. Thermal drift
5. Slew rate
6. Input and output voltage ranges

Input bias current:

The op-amp's input is a differential amplifier, which may be made of BJT or FET. In either case the input transistors must be biased into this linear region by supplying currents into the bases. In an ideal op-amp, no current is drawn from the input terminals. However, practically, input terminals conduct a small value of dc current to bias the input transistors when base currents flow through external resistances, they produce a small differential input voltage or unbalance; this represents a false input signal. When amplified, this small input unbalance produces an offset in the output voltage.

The input bias current shown on data sheets is the average value of base currents entering into the terminals of an op-amp.

$$I_B = \frac{(I_B^+ + I_B^-)}{2}$$

For 741, the bias current is 500nA or less. The smaller the input bias current, the smaller is the offset at the output voltage.

Input offset current:

The input offset current is the difference between the two input currents driven from a common source

$$|I_{OS}| = I_B^+ + I_B^-$$

It tells you how much larger one current is than the other. Bias current compensation will work if both bias currents IB^+ and IB^- are equal. So, the smaller the input offset current the better the OP-amp. The 741 op-amps have input offset current of 20nA.

Input offset voltage:

Ideally, the output voltage should be zero when the voltage between the inverting and non-inverting inputs is zero. In reality, the output voltage may not be zero with zero input voltage. This is due to un-avoidable imbalances, mismatches, tolerances, and so on inside the op-amp. In order to make the output voltage zero, we have to apply a small voltage at the input terminals to make output voltage zero. This voltage is called input offset voltage .i.e., input offset voltage is the voltage required to be applied at the input for making output voltage to zero volts. The 741 op-amp has input offset voltage of 5mV under no signal conditions. Therefore, we may haveto apply a differential input of 5mV, to produce an output voltage of exactly zero.

Thermal drift:

Bias current, offset current and offset voltage change with temperature. A circuit carefully mulled at 25°C may not remain so when the temperature rises to 35°C. This is called drift often, offset current drift is expressed in n A/°C and offset voltage drift in mV/°C. These indicate the change is offset for each degree Celsius change in temperature. There are very few techniques that can be used to minimize the effect of drift.

Slew rate:

Among all specifications affecting the ac operation of the op-amp, slew rate is the most important because it places a severe limit on a large signals operation. **Slew rate** is defined as the maximum rate at which the output

voltage can change. The 741 op-amp has a typical slew rate of 0.5 volts per microsecond (V / µs). This is the ultimate speed of a typical 741; its output voltage can change no faster than 0.5V / µs. If we drive a 741 with large step input, it takes 20µs (0.5 V/µsx10V) for the output voltage to change from 0 to 10V.

Band width:

Slew rate distortion of a sine wave starts at a point where the initial slope of the sine wave equals the slew rate of the op-amp. The maximum frequency at which the op-amp can be operated without distortion is

$$f_{\max} = \frac{SR}{(2\pi V_P)}$$

where, SR=slew rate of op-amp, VP= peak voltage of output sine wave. As an example, if the output sine wavehas a peak voltage of 10V and the op-amp slew rate is 0.5 V / µs, the maximum frequency for large signal operation is

$$f_{\max} = \frac{0.5V/\mu s}{2\pi \times 10V} = 7.96 \text{ KHz}$$

Frequency f_{max} is called bandwidth of op-amp. The 741 op-amp has a bandwidth of approximately 8 KHz. This means the undistorted band width for large signal operation is 8 KHz.

Input and output voltage ranges:

Maximum positive and negative input voltage applied to the op-amp for undistorted output gives the input voltage range. Maximum positive and negative undistorted output voltage of the op-amp gives the output voltage range.

Op-Amp applications:

Signal conditioners

- Linear - eg. Adder, subtractor, differentiator, integrator, V-I converter, etc.
- Non-Linear - eg., log amplifier, anti-log amplifier, multiplier, divider, etc.

Signal Processors

- Linear - eg., voltage follower, instrumentation amplifier, etc.
- Non-Linear - eg., log amplifier, anti-log amplifier, multiplier, divider, etc.

Result:

Thus the working principle of Op-Amp IC741were studied.

Outcomes:

Able to understand the concept of Operational amplifiers.

Viva – voce

1. What are the input and the output stages for a 741 Op-Amp?
2. What is input bias current?
3. What is slew rate?
4. What is a differential amplifier?
5. What is meant by non-inverting and inverting input of a differential amplifier?
6. List out the applications of op-amp.
7. What is meant by open-loop voltage gain?
8. What is meant by gain-bandwidth product?
9. List out the ideal op-amp parameters.
10. How op-amp works as a Subtractor?
11. What is the input stage of an op-amp?
12. What is meant by comparators?
13. What type of signals is applied in differential mode operation of an op-amp?
14. Compare common-mode gain and differential-mode gain.
15. What is CMRR?
16. What are the characteristics of ideal Op-amp?
17. What is perfect balance in Op-amp?
18. Why Op-amp called direct coupled high differential circuit?

Expt. No. 18 APPLICATION OF OP-AMP

Aim:

To design a inverting and non-inverting op-amp

Apparatus Required:

S. No.	Apparatus	Range	Quantity
1	Op-Amp	IC 741	1
2	Resistor		
3	Capacitor	As per design	3
4	Power Supply		2
5	Function Generator		1
6	CRO	(0 - 30)MHz	1

7	Bread Board	-	1
8	Connecting wires	-	few

Theory:

Inverting Amplifier:

The Op-Amp IC741 is the most widely used of all the Op-amp circuits. An inverting amplifier uses negative feedback to invert and amplify a voltage.

In the inverting amplifier only one input is applied and that is to the inverting input (V2) terminal. The non-inverting input terminal (V1) is grounded. Since, V1= 0 V & V2= V_{in}

The output V0 is given by

$$V_{Out} = V_{in} (-R_f / R_{in})$$

where, the gain of amplifier is - Rf / Rin

$$V_{Out} = -AV_{in}$$

The negative sign indicates the output voltage is 180° out of phase with respect to the input and amplified by gain A.

Non-Inverting Amplifier:

The input is applied to the non-inverting input terminal and the Inverting terminal is connected to the ground.

$$V_1 = V_{in} \text{ and } V_2 = 0 \text{ volts}$$

The output voltage is larger than the input voltage by gain A & is in phase with the input signal. The signal is applied to the non-inverting input terminal and feedback is given to inverting terminal. The circuit amplifiers the input signals without inverting it. The output V_{out} is given by

$$V_{out} = V_{in}\left[1+\frac{R_2}{R_1}\right]$$

The voltage gain is given by given by

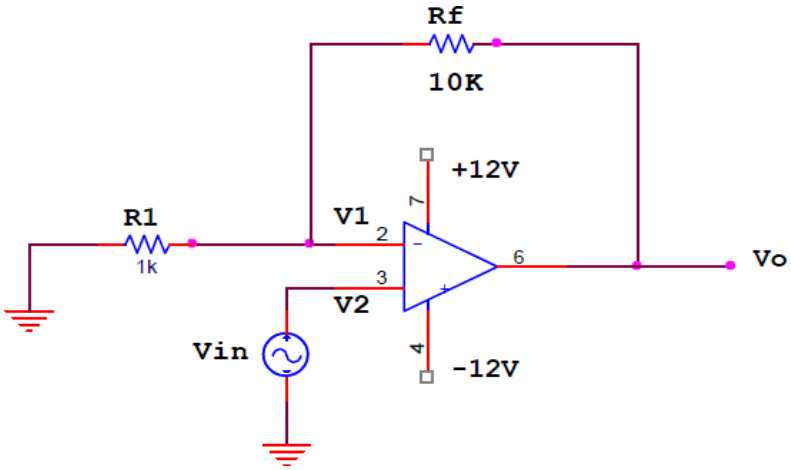
$$A_{CL} = \frac{V_{0ut}}{Vin} = \left[1+\frac{R_2}{R_1}\right]$$

$$V_{Out} = A_{CL}Vin$$

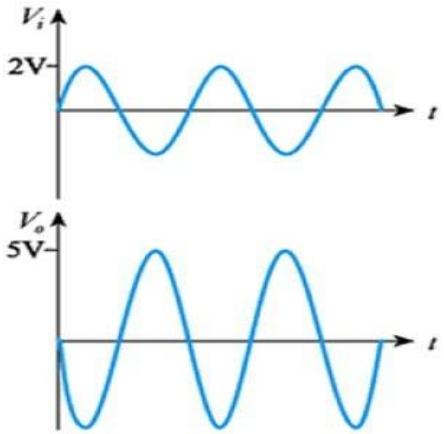
Compared to the inverting amplifier, the input resistance of the non-inverting is extremely large.

Circuit Diagram:

Inverting Amplifier:



Model Graph:

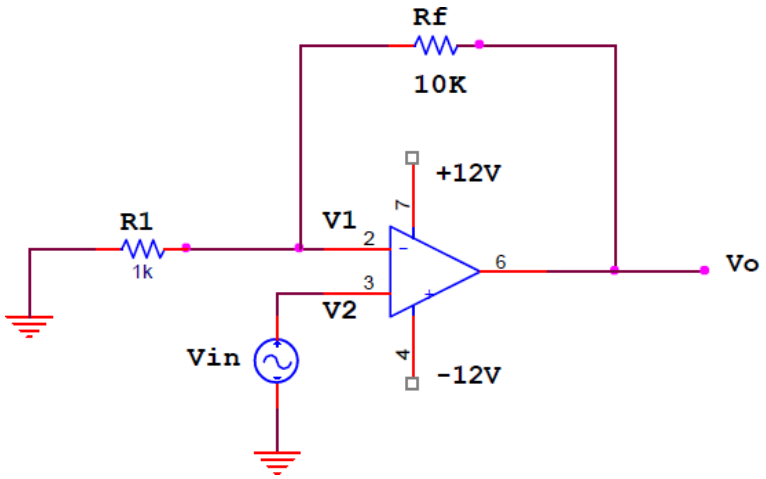


Tabulation:

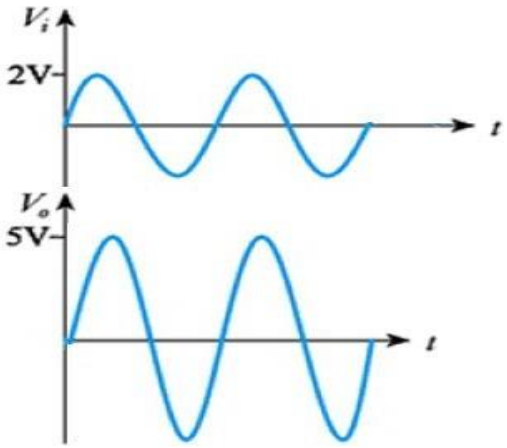
Time Period (ms)	Input voltage V_{in} (V)	Output Voltage V_o (V)

Circuit Diagram:

Non-Inverting Amplifier:



Model Graph:



Tabulation:

Time Period (ms)	Input voltage V_{in} (V)	Output Voltage V_o (V)

Procedure:

1. Make the connection as per the circuit diagram.

2. Set the input voltage to a constant value.
3. Feed input from function generator and observe the output on CRO.
4. Draw the input and output waveforms.

Result:

Thus an inverting and a non-inverting amplifier were designed using IC741 Op-Amp.

Outcomes:

Able to understand the concept of various applications of Operational amplifier.

Viva – voce

1. What is an operational amplifier?
2. What is the input impedance of a non-inverting operational amplifier (op-amp) amplifier?
3. If the open loop gain of an op-amp is very large, does the closed loop gain depend upon the external components or the op-amp?
4. Define – Common Mode Rejection Ratio
5. Explain the meaning of open loop and closed loop operation of an op- amp?
6. What is a practical op-amp? Draw its equivalent circuit.
7. What will be the output if negative feedback is applied to the op-amp?
8. What is the common-mode gain of an op-amp?
9. What is the differential-mode gain of an op-amp?
10. What is the use of negative feedback in an op-amp?
11. What is an op-amp?
12. What is common-mode and differential-mode signals?
13. What is the importance of CMRR?