# SRI SHANMUGHA COLLEGE OF ENGINEERING AND TECHNOLOGY, SANKARI

DEPARTMENT OF

ELECTRONICS AND COMMUNICATION ENGINEERING

LAB RECORD

# EC8462 – LINEAR INTEGRATED CIRCUITS LABORATORY

Student Name :

Reg.No :

Year/ Section :

# EC8462 – LINEAR INTEGRATED CIRCUITS LABORATORY

## OBJECTIVES

- To understand the basics of linear integrated circuits and available ICs
- To understand the characteristics of the operational amplifier.
- To apply operational amplifiers in linear and nonlinear applications.
- To acquire the basic knowledge of special function IC.
- To use SPICE software for circuit design.

## LIST OF EXPERIMENTS

1. Inverting, Non inverting and differential amplifiers.
2. Integrator and Differentiator.
3. Instrumentation amplifier.
4. Active low-pass, High-pass and band-pass filters.
5. Astable&Monostable multivibrators using Op-amp .
6. Schmitt Trigger using op-amp.
7. Phase shift and Wien bridge oscillators using Op-amp.
8. Astable and Monostable multivibrators using NE555 Timer.
9. PLL characteristics and its use as Frequency Multiplier, Clock synchronization.
10. R-2R Ladder Type D- A Converter using Op-amp.
11. DC power supply using LM317 and LM723.
12. Study of SMPS.

### SIMULATION USING SPICE

1. Active low-pass, High-pass and band-pass filters using Op-amp.
2. Astable and Monostable multivibrators using NE555 Timer.
3. A/ D converter
4. Analog multiplier

## Course Outcomes

CO1: Design amplifiers, Differentiator and Integrator using operational amplifiers.

CO2: Design and analyze the frequency response of filters using op-amp .

CO3: Design Oscillators and multivibrators using operational amplifiers.

CO4: Analyze the working of PLL and describe its application as a frequency multiplier.

CO5: Design D-A converter using operational amplifiers.

CO6: Design DC power supply using ICs.

CO7: Use SPICE tool to design and simulate circuits using Op-amp.

### Laboratory Discipline

The laboratory can be a very enjoyable place to work in. In order to make it even more enjoyable for yourself and for others, some basic discipline is required by everyone. Please note the following points:

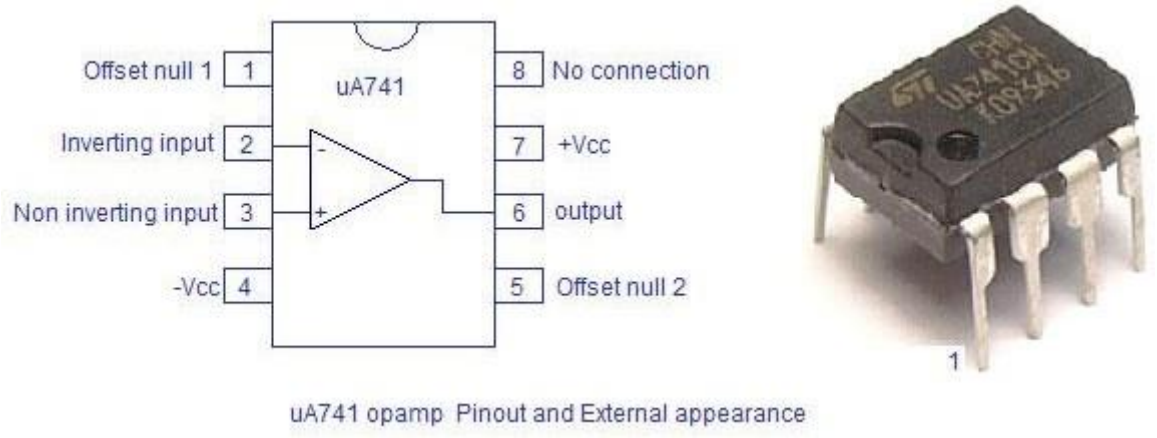
1. Come to the lab on time, and don't leave before time.
2. Keep your bags on the racks provided in the lab.
3. Don't move equipment from one table to another without permission.
4. Clean up the table after use. no pieces of wire, components, etc. should be left lying around.
5. If any equipment is not working, please leave a note on the equipment and inform the lab staff.
6. Follow the dress code in lab as per our college rules.
7. Always power down the electrical equipment, disconnect the power cord, and wait for a few seconds before touching exposed wires.
8. Each group is responsible for their Lab bench. After the Lab exercise is over, all equipment should be powered down and all probes, cords, etc. returned to their proper position.

# Content

# About the uA741 Op-amp IC

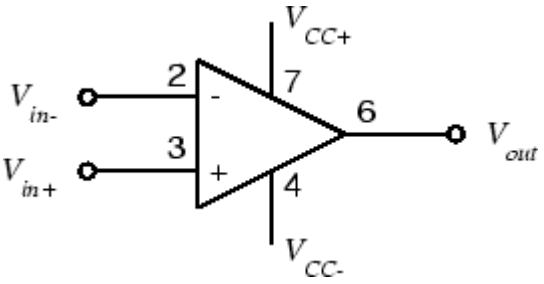
The 741 IC was designed by Dave Fullagar of Fairchild Semiconductor in 1968. The 741 IC is the successful predecessor of the LM 101 IC, and the only difference between the two was that an additional 30pF internal compensation capacitor was added for the 741 IC. But, this simple addition has made this IC evergreen in the electronics world and is still manufactured by different companies in different versions and specifications, and is made recognizable by adding the famous number 741 in the series.

The 741 IC is available in the market as 8-pin metal can, 10-pin flat pack, 8 or 14 pin DIP. The pin configuration for 8 pin metal can package is shown below.



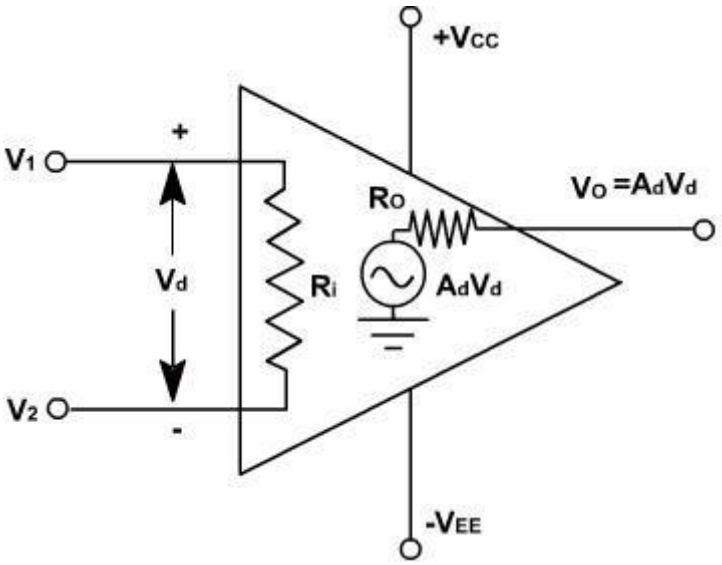

uA741 opamp Pinout and External appearance

Op-amp Symbol:




The input voltage range for a 741 IC is ±15V. i.e $V_{CC+}$=+15V and $V_{CC-}$ =-15V .

**Equivalent Circuit of an Op-amp:**




**Ideal Characteristics of an Op-amp**

1.Open Loop Voltage gain = infinite.

2.Input impedance Ri= infinite.

3.Output impedance Ro= Zero.

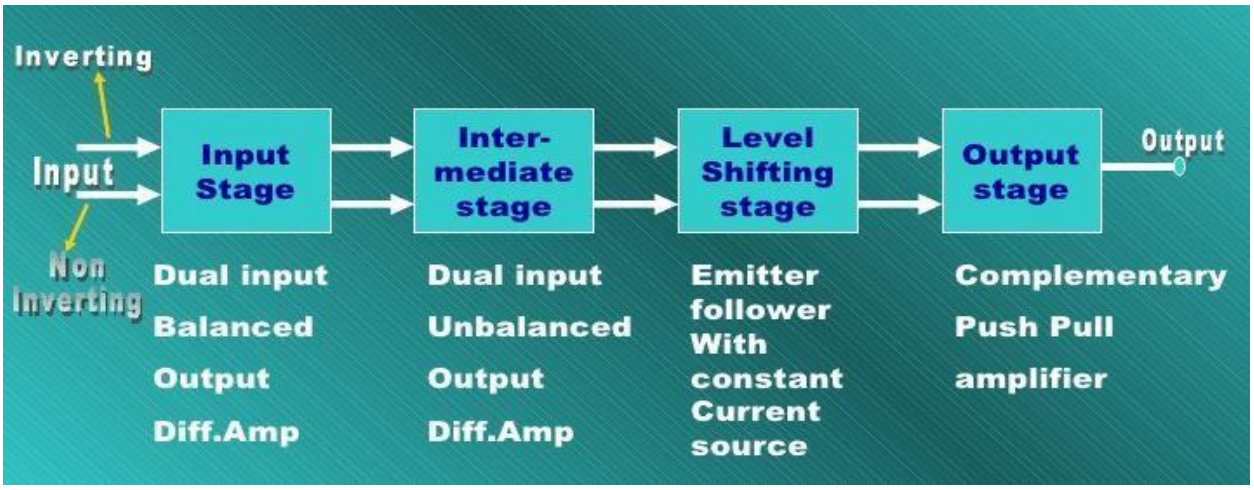
4.Bandwidth (BW) = infinite.

5. Zero input offset voltage. (if input is zero ,output also zero.)

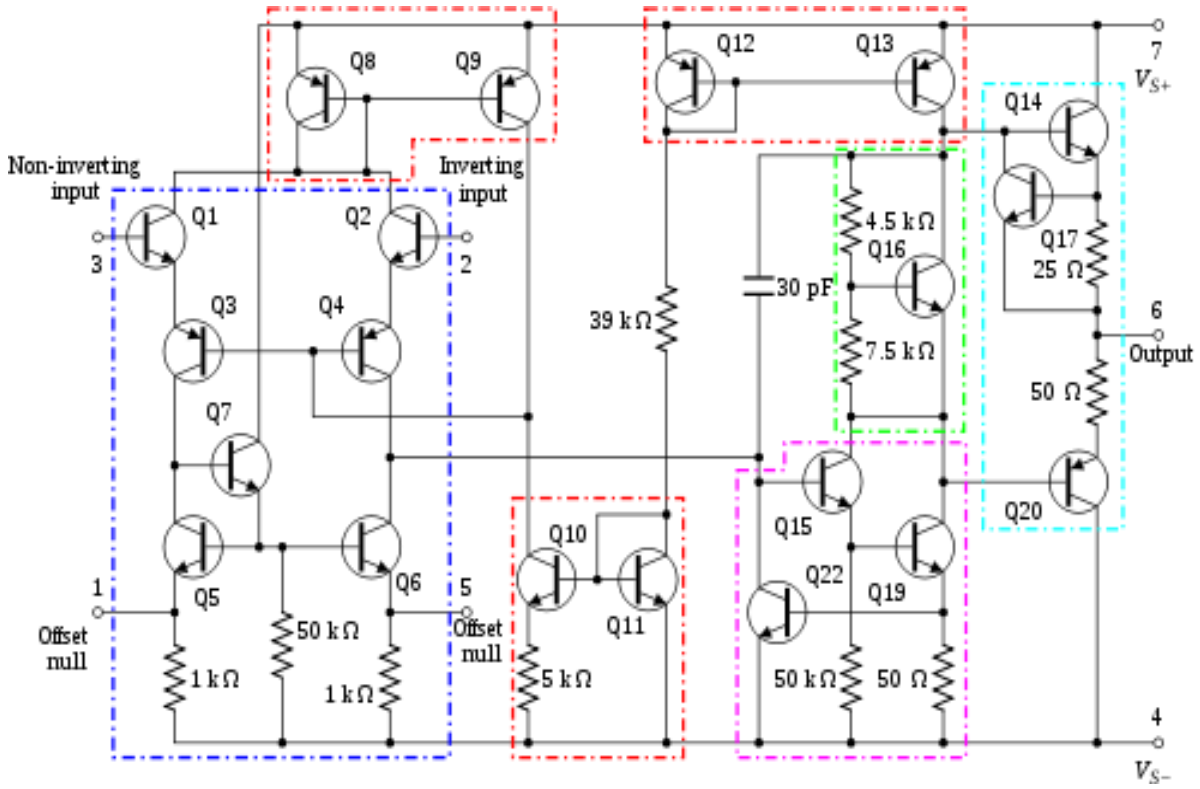
6. Infinite slew rate

7. Infinite common-mode rejection ratio (CMRR)

**Block Diagram of an µA 741:**




**Internal Circuit Diagram of an Op-amp:**



## Exp.No: 1 Inverting, Non inverting and differential amplifiers.

Date:

**Aim:** To design inverting, Non inverting and Differential amplifiers using Op-amp.

**Apparatus Required:**

| S.No | Components | Specification | Quantity |
|---|---|---|---|
| 1. | Op-amp | µA741 | |
| 2. | Resistor | | |
| 3. | Regulated Power supply | | |
| 4. | Function Generator | | |
| 5. | CRO | | |

## Theory:

As the open loop DC gain of an operational amplifier is extremely high we can therefore afford to lose some of this high gain by connecting a suitable resistor across the amplifier from the output terminal back to the inverting input terminal to both reduce and control the overall gain of the amplifier. This then produces and effect known commonly as Negative Feedback, and thus produces a very stable Operational Amplifier based system.

Negative Feedback is the process of "feeding back" a fraction of the output signal back to the input, but to make the feedback negative, we must feed it back to the negative or "inverting input" terminal of the op-amp using an external Feedback Resistor called R$f$. This feedback connection between the output and the inverting input terminal forces the differential input voltage towards zero.

This effect produces a closed loop circuit to the amplifier resulting in the gain of the amplifier now being called its **Closed-loop Gain**. Then a closed-loop inverting amplifier uses negative feedback to accurately control the overall gain of the amplifier, but at a cost in the reduction of the amplifiers gain.

**3 op-amp circuit to achieve a closed loop gain using negative feed back ,**

1. **Inverting amplifier**
   Input signal is given to inverting input terminal of an Op-amp.
2. **Non inverting amplifier**
   Input signal is given to non-inverting input terminal of an Op-amp.
3. **Differential amplifier**
   Two input signal V1 and V2 given to both inverting and Non inverting input terminals of an Op-amp.

**Design 1: To design inverting amplifier with the gain of 10.Choose input resistor is equal to 10 KΩ.**

**Output voltage of inverting amplifier** $Vo = -\frac{RF}{R1}\ Vin$

**Closed Loop gain**$ACL = \frac{RF}{R1}$**If R 1 =10 KΩ and gain is 10 .**

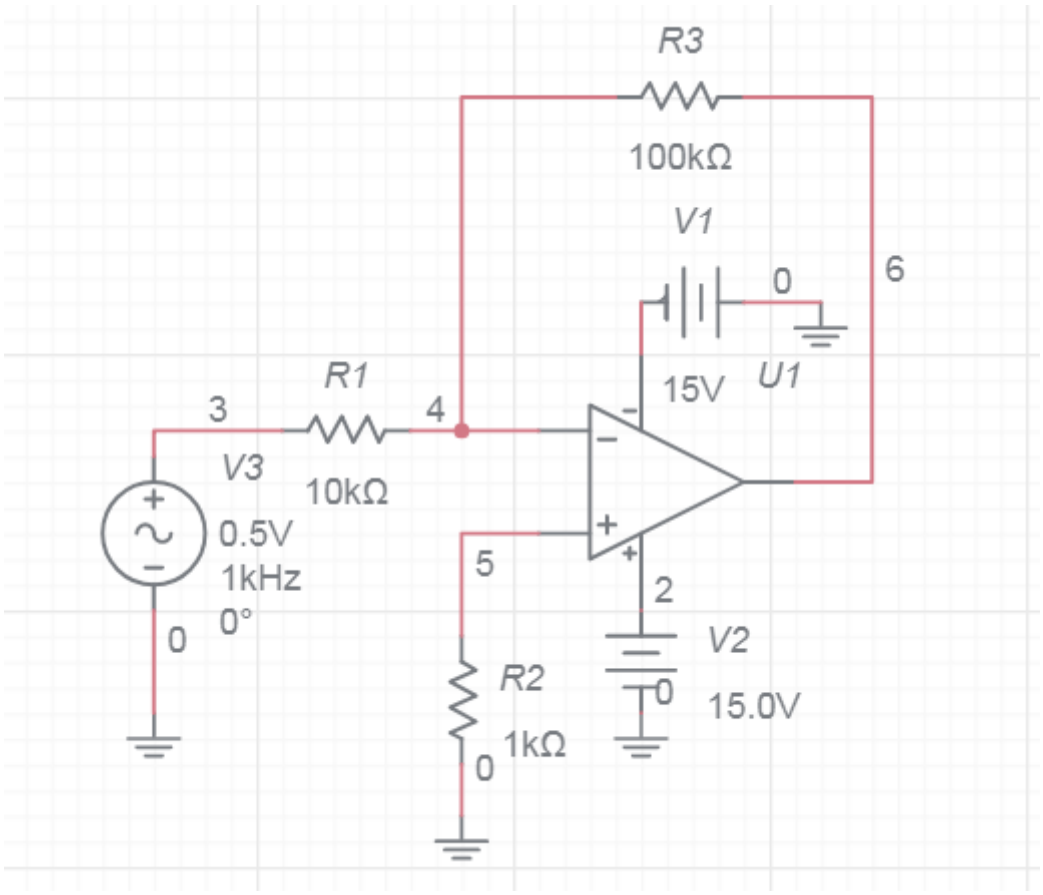
$$10 = \frac{RF}{10\ K\Omega}$$

**So $R_F$ = 100KΩ**

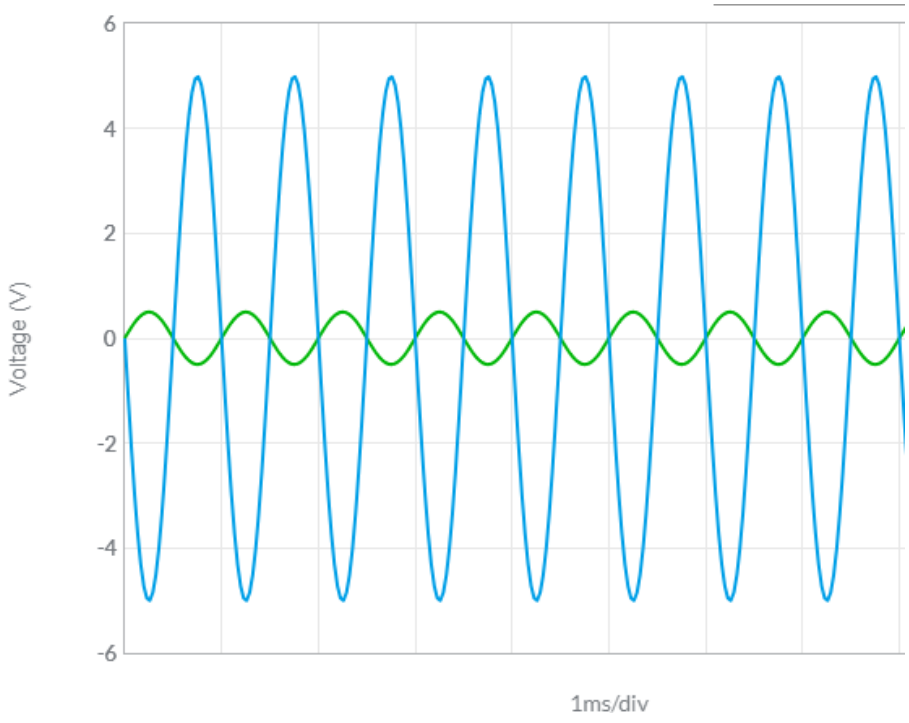
| $R_F$ | Amplitude | Time |
|---|---|---|
| | **Input =**<br>**Output =** | |
| | **Input =**<br>**Output =** | |
| | **Input =**<br>**Output =** | |
| | **Input =**<br>**Output =** | |

**Note: Find at what gain op amp output will saturate?**

**Circuit:**




**Output waveform:**



**Design 2: Design a Non inverting amplifier. Let $R_1$=5 KΩ , $R_F$=20 KΩ and Vi=1V. A load resistor 5 KΩ is connected at the output .Calculate (i) Vo (ii) $A_{CL}$ (iii) Load Current $I_L$. Verify the output both theory and Practical. if both the outputs are not same, justify the reason.**

**Solution: Theoretical -The output voltage of Non inverting amplifier**

**(i)** $Vo = (1 + \frac{RF}{R1})\, Vi$

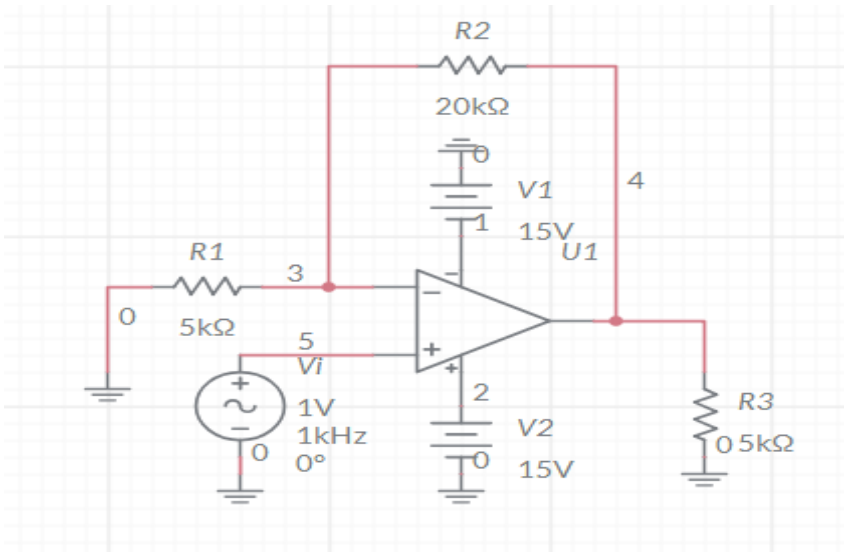
**(ii)** $A_{CL} = (1 + \frac{RF}{R1})$

**(iii)** $I_L = Vo/R_L$

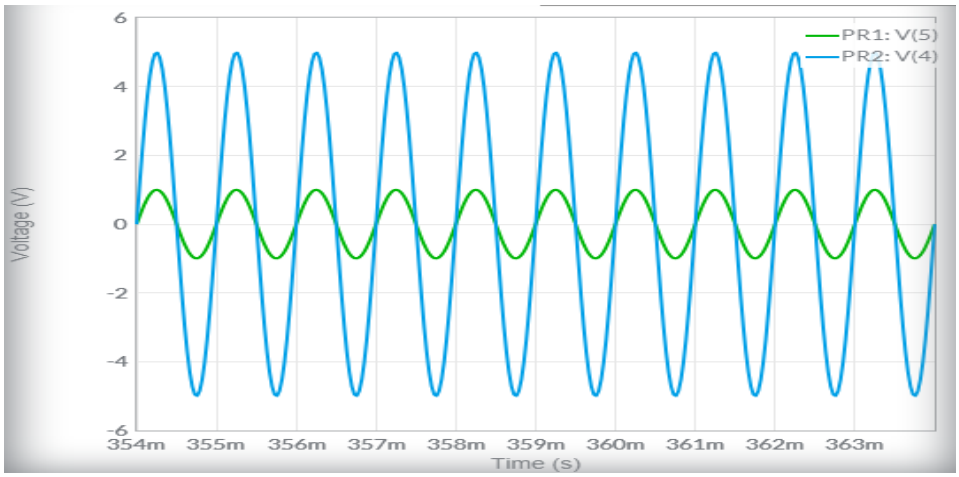
**Practical:**

| | Amplitude | Time |
|---|---|---|
| **Input** | | |
| **Output (Vo)** | | |
| **Load Current ($I_L$)** | | |

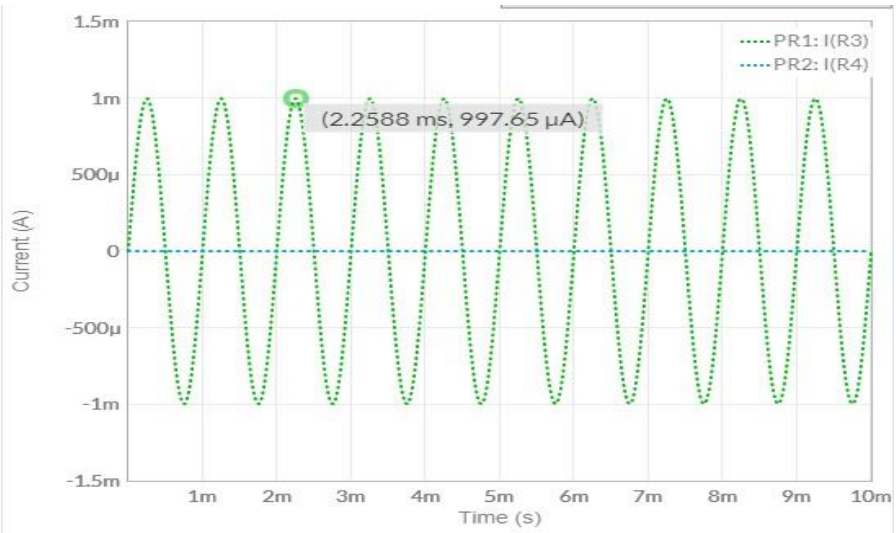
**Circuit:**




**Output : Voltage**




**Current:**



**Design 3: Design a Differential amplifier circuit with unity gain and determine the CMRR for Different values of $V_1$ and $V_2$.**

**Solution :**

Output of Differential amplifier is Vo = $Vo = \frac{R2}{R1}(V^+ - V^-)$

Usually $V^+$ input at non inverting terminal and $V^-$ input at inverting terminal of an Op-amp.

Common mode rejection ratio

$$CMRR = \frac{A_d}{A_c}$$

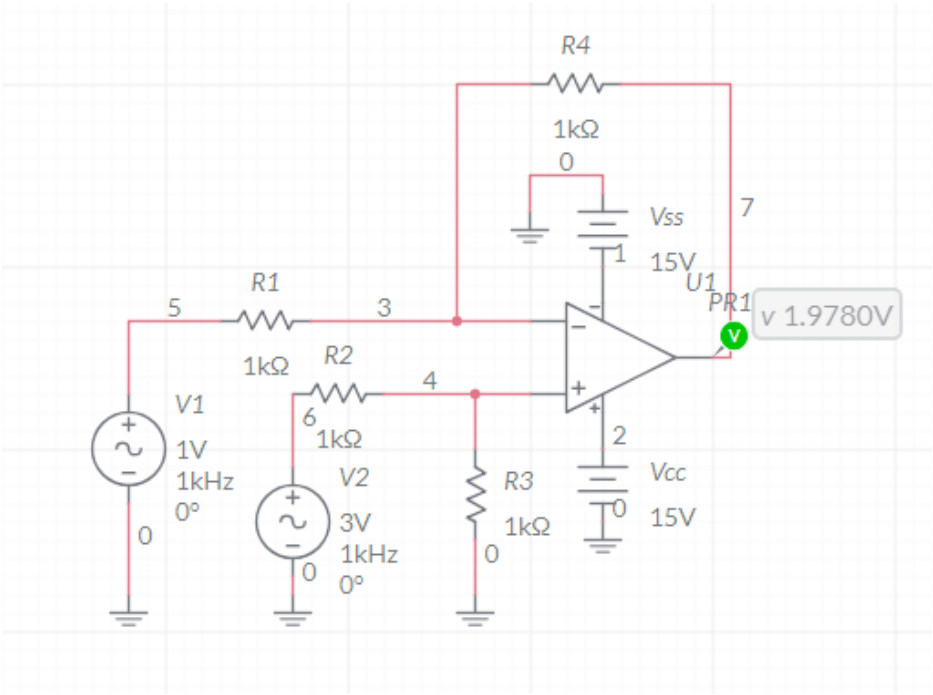
**Where $A_d$ = Differential Mode gain** **$A_c$=common mode gain**

$$A_d = \frac{V_{out}}{V_2 - V_1} \quad A_c = \frac{2\,V_{out}}{V_2 + V_1}$$

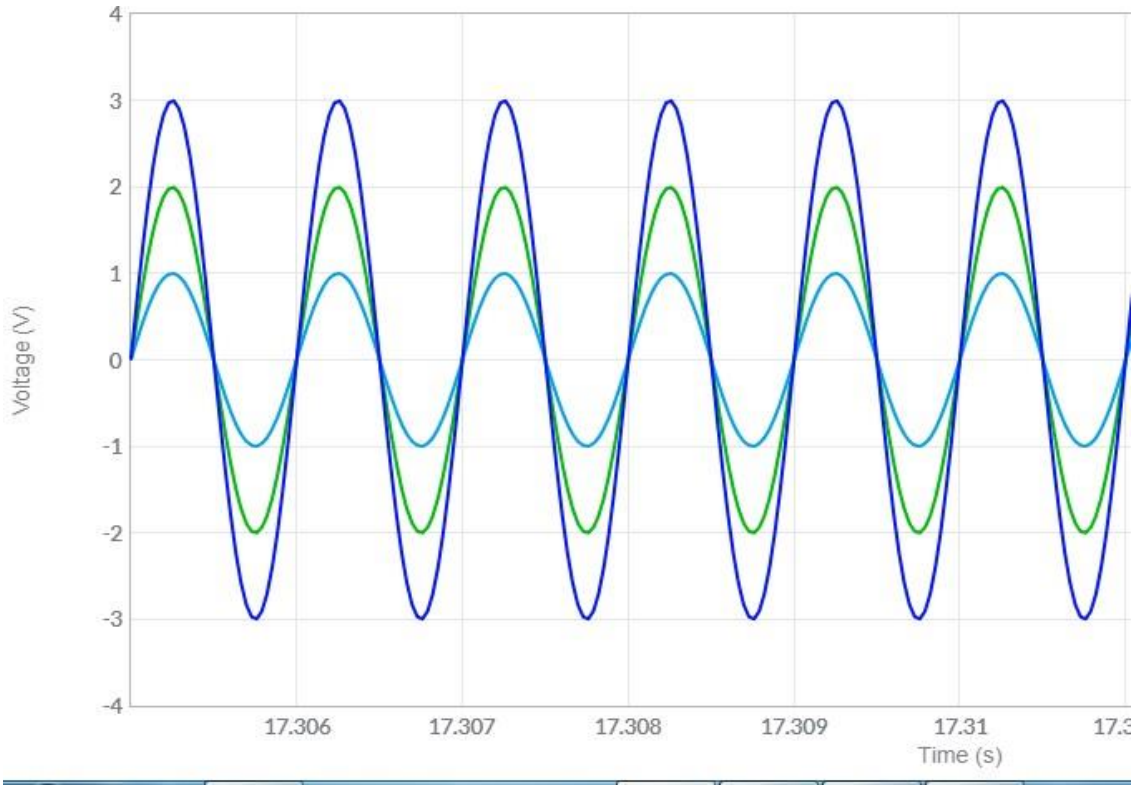
**Observation:**

| S.No | $V_1$ | $V_2$ | Vout | $A_d$ | $A_c$ | CMRR($A_d/A_c$) |
|---|---|---|---|---|---|---|
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |

**Circuit:**




**Output:**




**Result:**

## Exp.No: 2 Integrator and Differentiator

Date:

**Aim:** To design an Integrator and Differentiator circuit using Op-amp.

**Apparatus Required:**

| S.No | Components | Specification | Quantity |
|---|---|---|---|
| 1. | Op-amp | µA741 | |
| 2. | Resistor | | |
| 3. | Capacitor | | |
| 4. | Regulated Power supply | | |
| 5. | Function Generator | | |
| 6. | CRO | | |

## Theory:

## Differentiator:

An op-amp differentiator or a differentiating amplifier is a circuit configuration which produces output voltage amplitude that is proportional to the rate of change of the applied input voltage.A differentiator with only RC network is called a passive differentiator, whereas a differentiator with active circuit components like transistors and operational amplifiers is called an active differentiator. Active differentiators have higher output voltage and much lower output resistance than simple RC differentiators.

An op-amp differentiator is an inverting amplifier, which uses a capacitor in series with the input voltage. Differentiating circuits are usually designed to respond for triangular and rectangular input waveforms. For a sine wave input, the output of a differentiator is also a sine wave, which is out of phase by $180^o$ with respect to the input (cosine wave).

Differentiators have frequency limitations while operating on sine wave inputs; the circuit attenuates all low frequency signal components and allows only high frequency components at the output. In other words, the circuit behaves like a high-pass filter.

**INTEGRATOR:**

In an integrating circuit, the output is the integration of the input voltage with respect to time. A passive integrator is a circuit which does not use any active devices like op-amps or transistors.

An integrator circuit which consists of active devices is called an Active integrator. An active integrator provides a much lower output resistance and higher output voltage than is possible with a simple RC circuit.

Op-amp differentiating and integrating circuits are inverting amplifiers, with appropriately placed capacitors. Integrator circuits are usually designed to produce a triangular wave output from a square wave input. Integrating circuits have frequency limitations while operating on sine wave input signals.

**Design Integrator:**

**Consider the Lossy integrator for the components values.R1=10KΩ ,RF=100 KΩ, CF= 0.01μF.Determine the low frequency limit of integration and study the response for the inputs (i) Sine wave (ii) Square input.**

**Solution:**

**The lower frequency limit of integration $f_a$ is**

$$f_a = \frac{1}{2\pi R_F C_F}$$

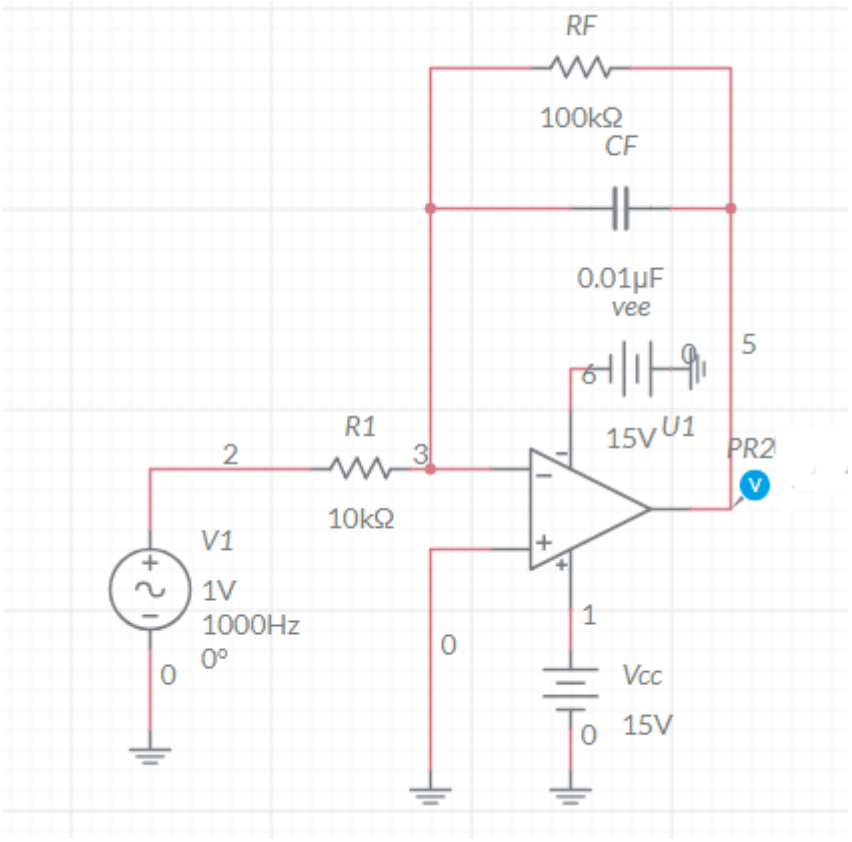
$$f_a = \frac{1}{2\pi \times 100 \times 10^3 \times 0.01 \times 10^{-6}} = \textbf{159 Hz.}$$

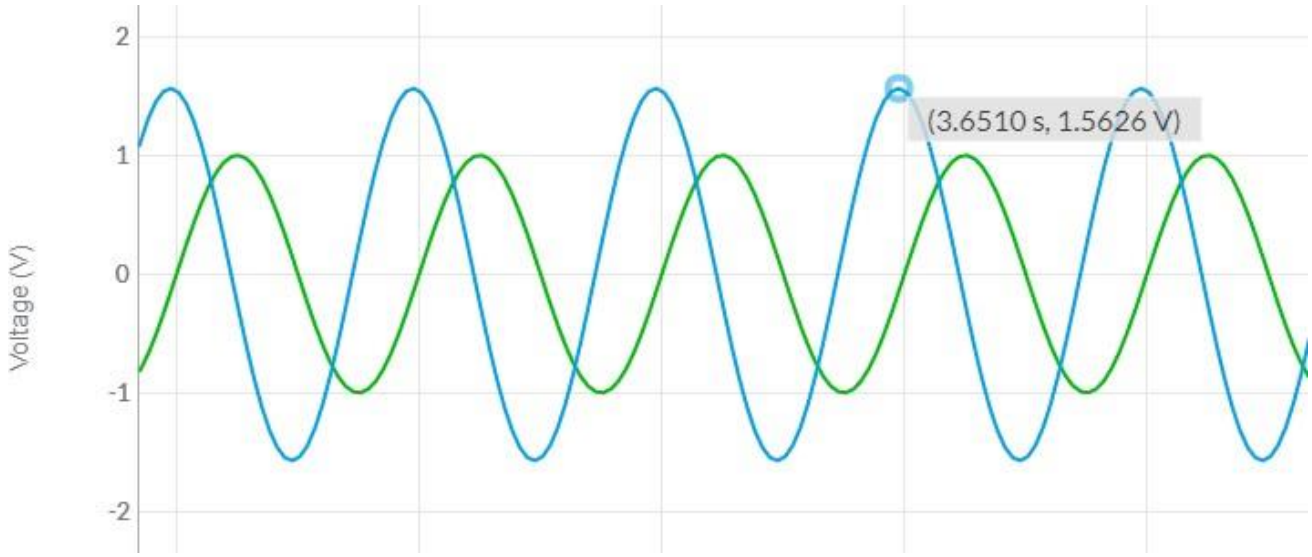
**For 99% accuracy , the input frequency should be at least $10f_a$ .**

**Tabulation :**

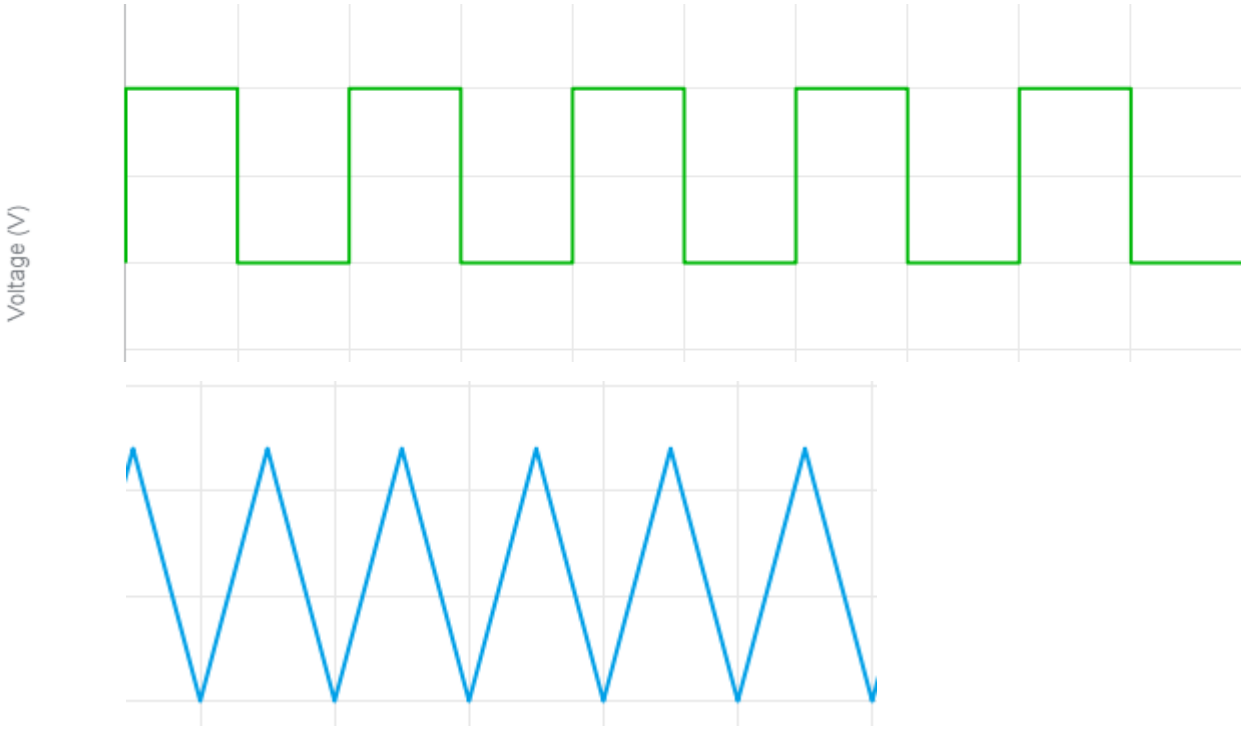
| Input | Amplitude | Frequency | Theoretical | | Practical | |
|---|---|---|---|---|---|---|
| | | | Amplitude | Frequency | Amplitude | Frequency |
| Sine | | | | | | |
| Square | | | | | | |

**(i) Consider Sine wave input 1Vpp and 1000Hz.**



**Square Input:**




**Design Differentiator:**

**Design an Op-amp differentiator that will differentiate an input signal with** $f_{max} = 500Hz$**.**

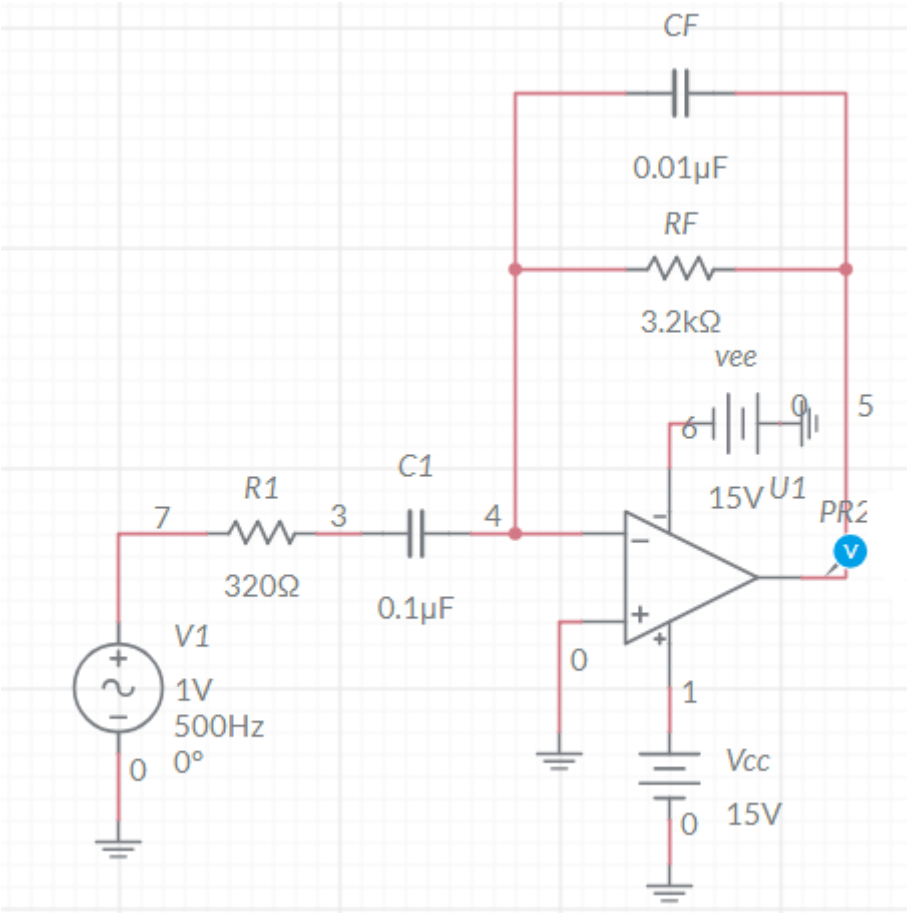
Solution: Select $f_a = f_{max} = 500Hz = \frac{1}{2\pi R_F C_1}$

Let C = 0.1uf

$$f_b = 10f_a = \frac{1}{2\pi R_1 C_1}$$

Differentiator output = $V_0 = -R_F C_1 \frac{dVi}{dt}$

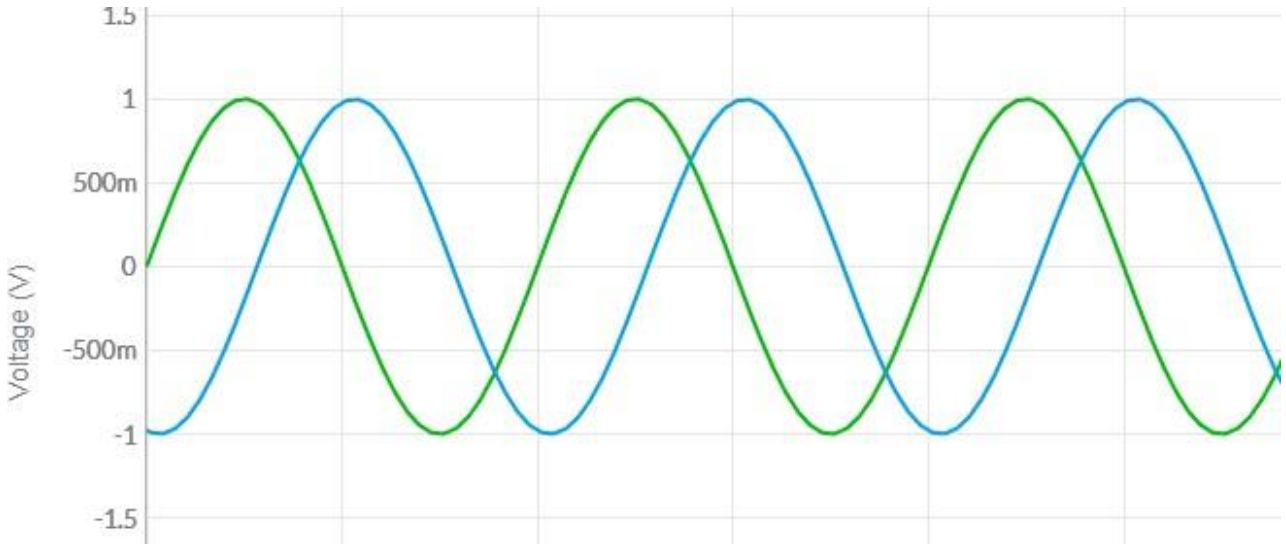
**Differentiator Circuit:**



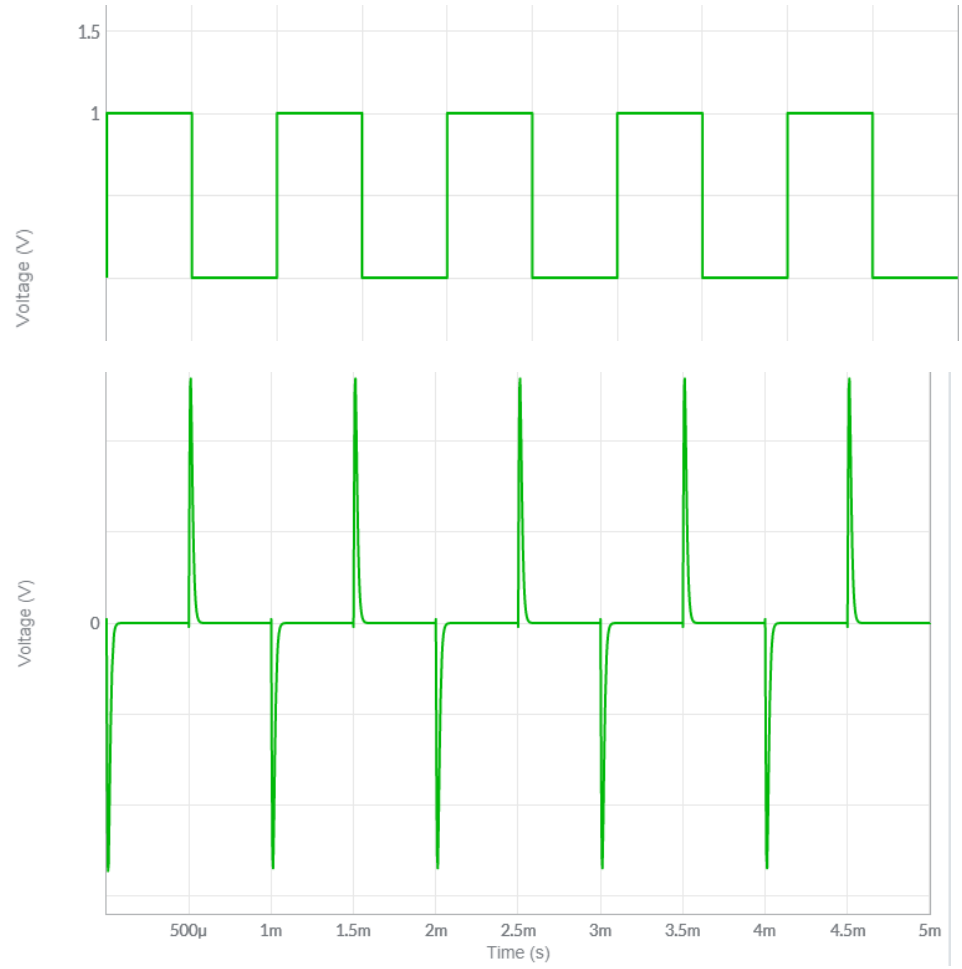

**Tabulation :**

| Input | Amplitude | Frequency | Theoretical | | Practical | |
|---|---|---|---|---|---|---|
| | | | Amplitude | Frequency | Amplitude | Frequency |
| Sine | | | | | | |
| Square | | | | | | |

**Output: input sine wave: Vi= 1sin 2π 500t**




**Output: input Square wave: Vi= 1V and 1KHz**



**Result:**

## Exp.No: 3 Instrumentation Amplifier

Date:

**Aim:** To design an instrumentation amplifier and obtain the output for various gain.

**Apparatus Required:**

| S.No | Components | Specification | Quantity |
|---|---|---|---|
| 1. | Op-amp | µA741 | |
| 2. | Resistor | | |
| 4. | Regulated Power supply | | |
| 5. | Function Generator | | |
| 6. | CRO | | |

## Theory:

Instrumentation amplifier is a kind of differential amplifier with additional input buffer stages. The addition of input buffer stages makes it easy to match (impedance matching) the amplifier with the preceding stage. Instrumentation are commonly used in industrial test and measurement application. The instrumentation amplifier also has some useful features like low offset voltage, high CMRR (Common mode rejection ratio), high input resistance, high gain etc.

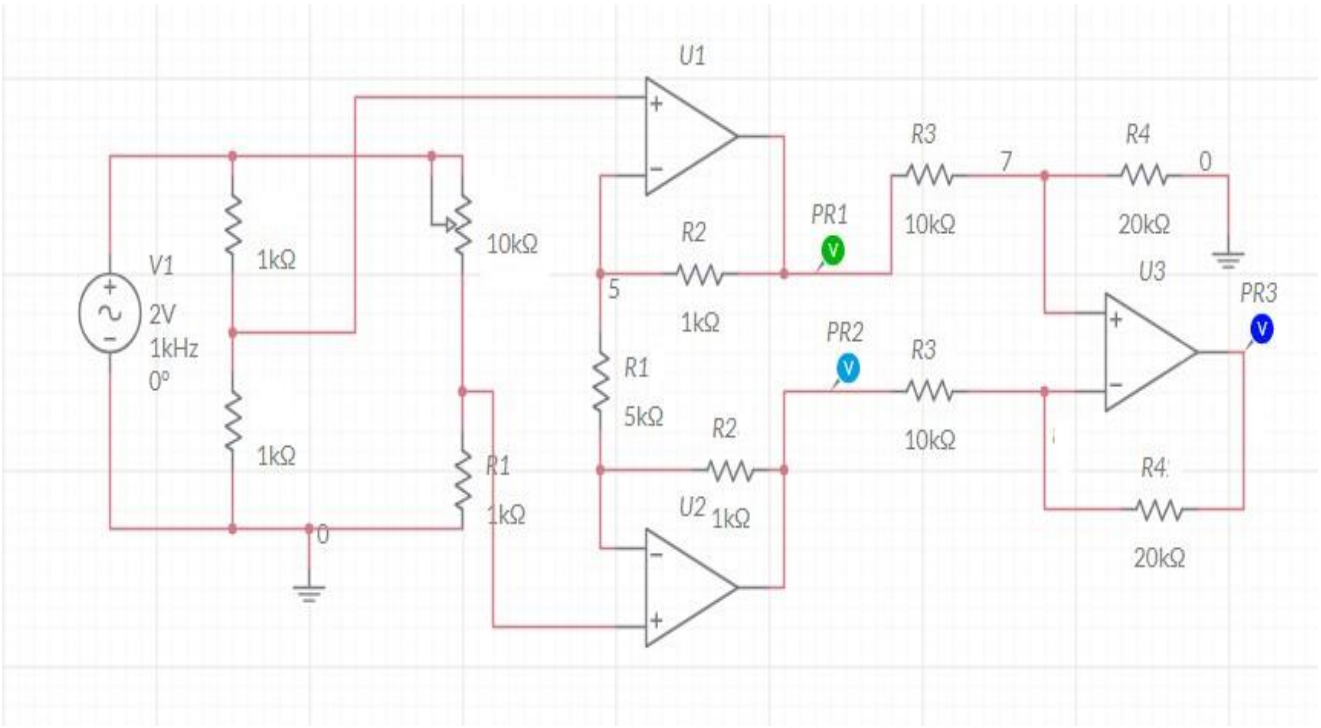
The two non-inverting amplifiers form a differential input stage acting as buffer amplifiers with a gain of 1 + 2R2/R1 for differential input signals and unity gain for common mode input signals. Since amplifiers A1 and A2 are closed loop negative feedback amplifiers, we can expect the voltage at Va to be equal to the input voltage V1. Likewise, the voltage at Vb to be equal to the value at V2.

As the op-amps take no current at their input terminals (virtual earth), the same current must flow through the three resistor network of R2, R1 and R2 connected across the op-amp outputs. This means then that the voltage on the upper end of R1 will be equal to V1and the voltage at the lower end of R1 to be equal to V2.

The voltage output from the differential op-amp A3 acting as a subtractor, is simply the difference between its two inputs ( V2 – V1 ) and which is amplified by the gain of A3which may be one, unity, (assuming that R3 = R4). Then we have a general expression for overall voltage gain of the instrumentation amplifier circuit as:

$$V_{out} = (V_2 - V_1)\left[1 + \frac{2R_2}{R1}\right]\frac{R_4}{R_3}$$

## Instrumentation Amplifier Circuit:




## Procedure:

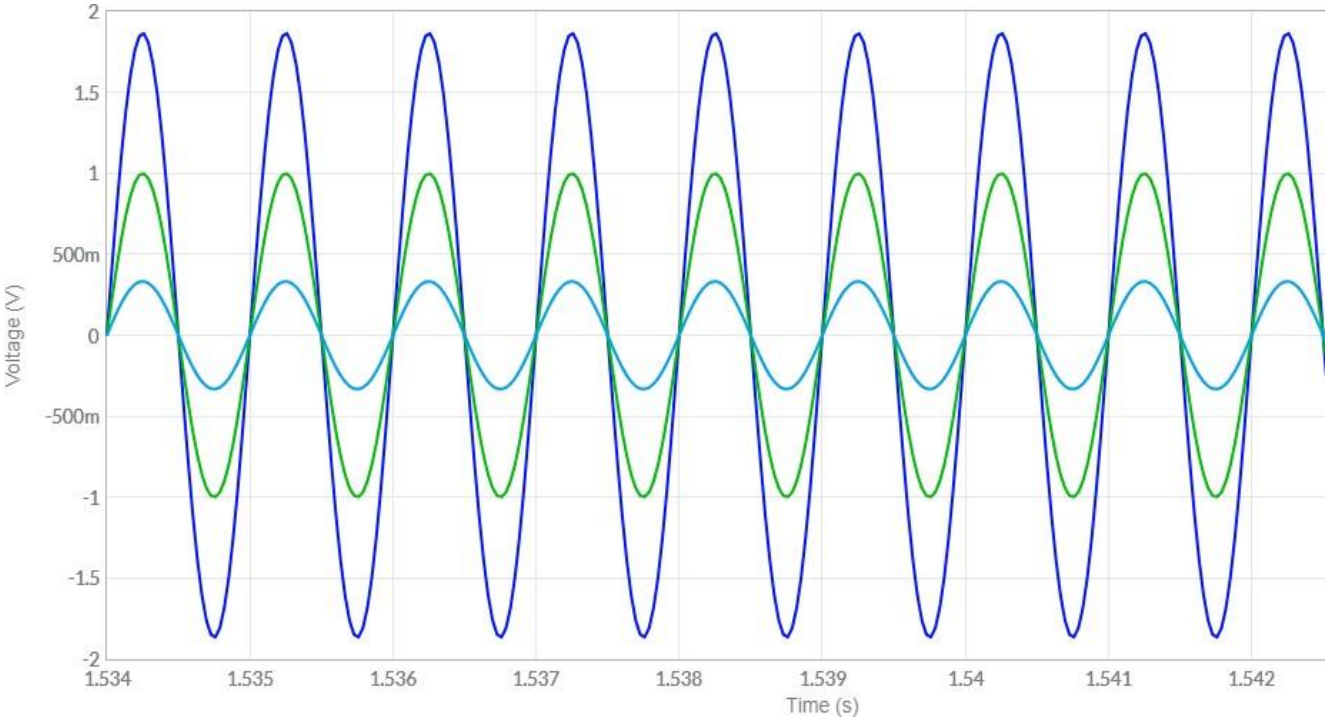
1. Connections are given as per the circuit diagram.
2. Input signal is connected to the circuit from the signal generator.
3. The input and output signals of the circuit observed from the dual channels 1 and 2 of the CRO.
4. Suitable voltage sensitivity and time-base on CRO is selected.
5. Change the gain setting resistor value and observe the output.

## Design:

## Tabulation:

| Input /Output | Theoretical | | | Practical | | |
|---|---|---|---|---|---|---|
| | Amplitude | Time | | | | |
| Input | | | | | | |
| Output | V1 | V2 | Vo | V1 | V2 | Vo |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |

## Output:




## Result:

## Exp.No: 4 Low Pass, High Pass and Band Pass Filters

Date:

**Aim:** To design Low pass, High pass and Band pass active filters using Op-amp and obtain frequency response.

**Apparatus Required:**

| S.No | Components | Specification | Quantity |
|---|---|---|---|
| 1. | Op-amp | µA741 | |
| 2. | Resistor | | |
| 3. | Capacitor | | |
| 4. | Regulated Power supply | | |
| 5. | Function Generator | | |
| 6. | CRO | | |

## Theory:

A filter is often used in electronic circuits to block (or allow) a select frequency to the circuit. An op-amp is used to design a filters, so it is called Active filters. There are Four types active filters like Low pass, High pass, band pass and band stop . A low pass filter is used in circuits that only allow low frequencies to pass through (below the Cutoff frequency). It is often used to block high frequencies and AC current in a circuit.A high pass filter is used in circuits that only require high frequencies to operate (above the cut off frequency). It blocks most low frequencies & DC component.A band pass filter is a combination of a high pass and a low pass filter. It allows only a select range of frequencies to pass through. It is designed such a way that the cut off frequency of the low pass filter is higher than the cut off frequency of the high pass filter, hence allowing only a select range of the frequencies to pass through.

## Procedure:

6. Connections are given as per the circuit diagram.
7. Input signal is connected to the circuit from the signal generator.
8. The input and output signals of the filter channels 1 and 2 of the CRO are connected.
9. Suitable voltage sensitivity and time-base on CRO is selected.
10. The correct polarity is checked.
11. The above steps are repeated for second order filter.

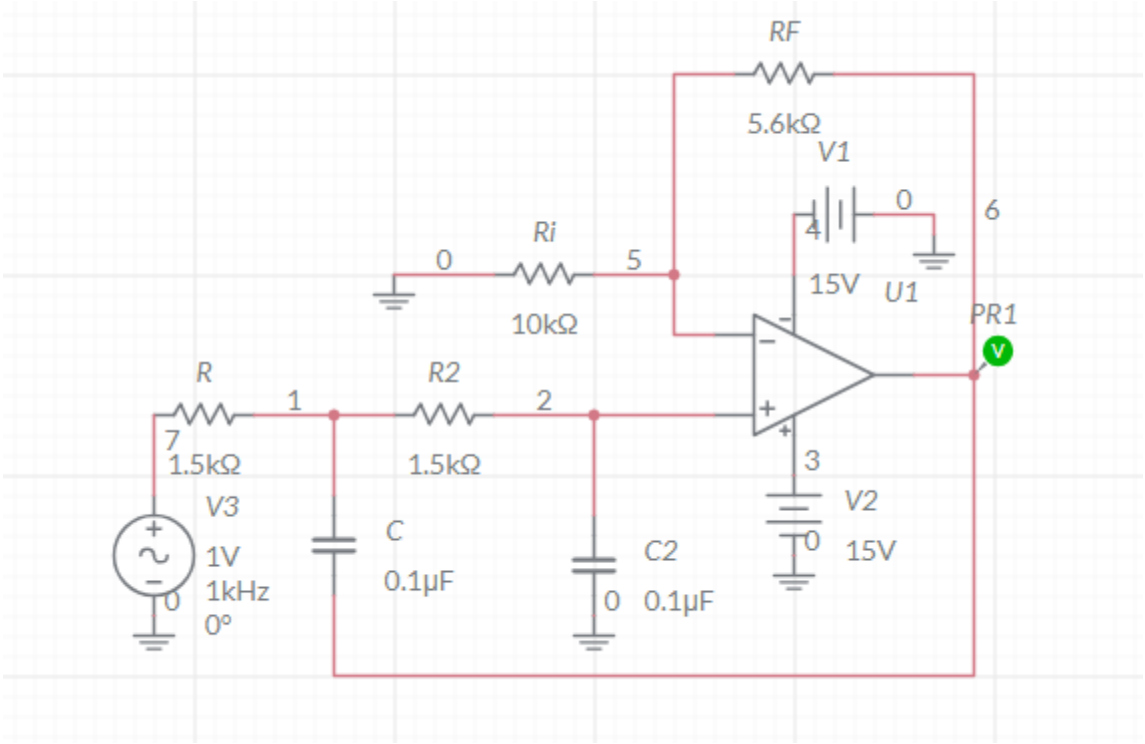
**Design Low Pass Filter:**

**Design Second order Butterworth Low Pass filter having upper cut off frequency 1KHz and determine its frequency response.**

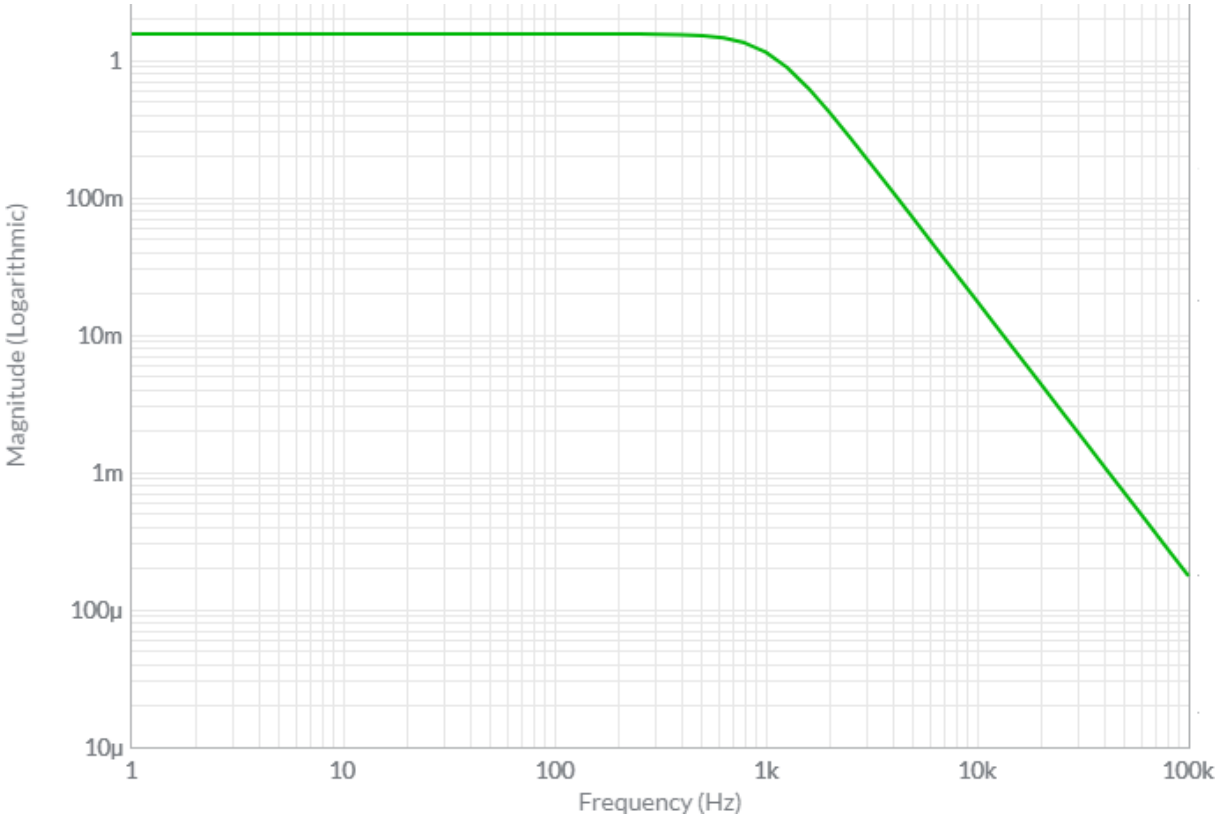
The following steps are used for the design of active LPF.

1. The value of high cut off frequency $f_H$ is chosen.
2. The value of capacitor C is selected such that its value is $\leq 1\mu F$.
3. By knowing the values of $f_H$and C, the value of R can be calculated using $f_H = \frac{1}{2\pi RC}$
4. Finally the values of $R_1$ and $R_f$ are selected depending on the designed pass band gain by using $A = 1 + \left(\frac{R_f}{R_1}\right)$ **Circuit Diagram:-**

## Low Pass filter Circuit:




## Output:



**Low Pass Filter Tabulation:**

| S.No | Frequency (Hz) | O/p voltage(v) | Gain=Vo/Vin | Gain=20log(Vo/Vin) |
|---|---|---|---|---|
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |

**Second order High Pass Filter:**

The high pass filter is the complement of the low pass filter. Thus the high pass filter can be obtained by interchanging R and C in the circuit of low pass configuration. A high pass filter allows only frequencies above a certain bread point to pass through and at terminates the low frequency components. The range of frequencies beyond its lower cut off frequency $f_L$ is called stop band.

**Design:-**

$$f_L = 1\mathbf{K}HZ, C = 0.1\mu F, Gain,\ Av = 2$$

$$f_L = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}}$$

$$Let\ \ R_2 = R_3 = R$$
$$C_2 = C_3 = C$$

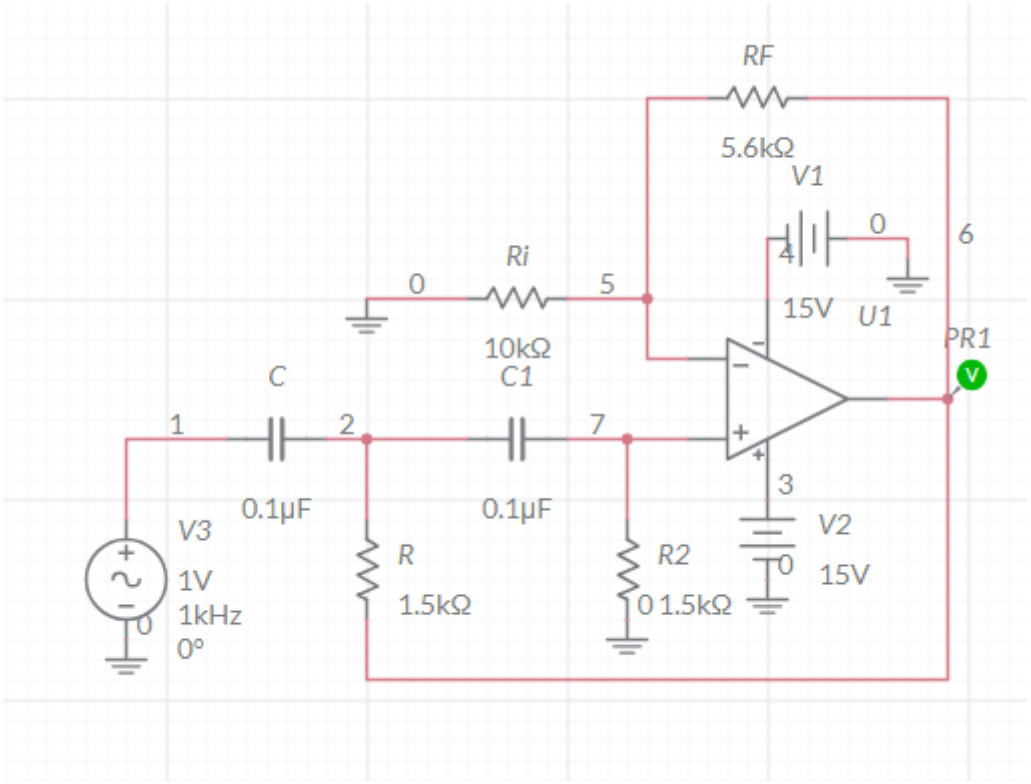
$$R_2 = R_3 = \frac{1}{2\pi fLC}$$

$$R_2 = R_3 = 1.5k\Omega$$

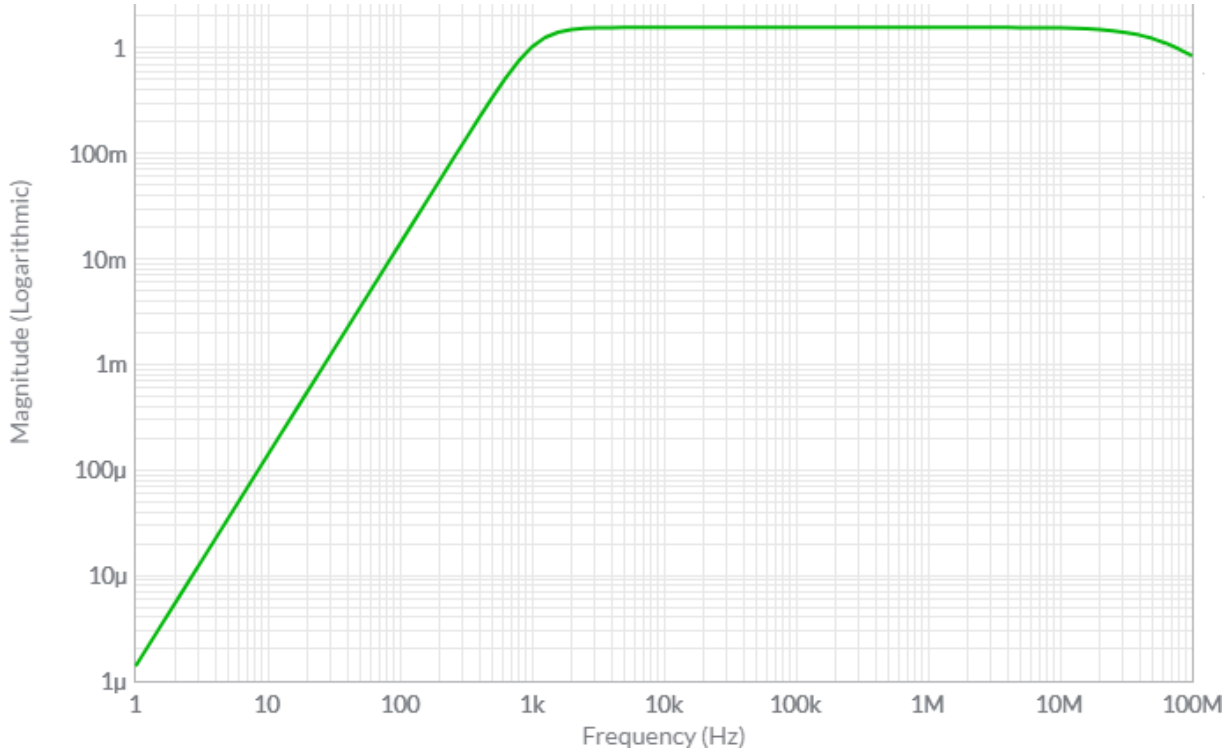
$$A = 1 + \frac{R_f}{R_1} = 2$$

$$\therefore R_f = R_1 = 10k\Omega(given)$$

**Second order High Pass Filter Circuit:**




**Output:**



**High Pass Filter Tabulation:**

| S.No | Frequency (Hz) | O/p voltage(v) | Gain=Vo/Vin | Gain=20log(Vo/Vin) |
|---|---|---|---|---|
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |

**BPF:-**

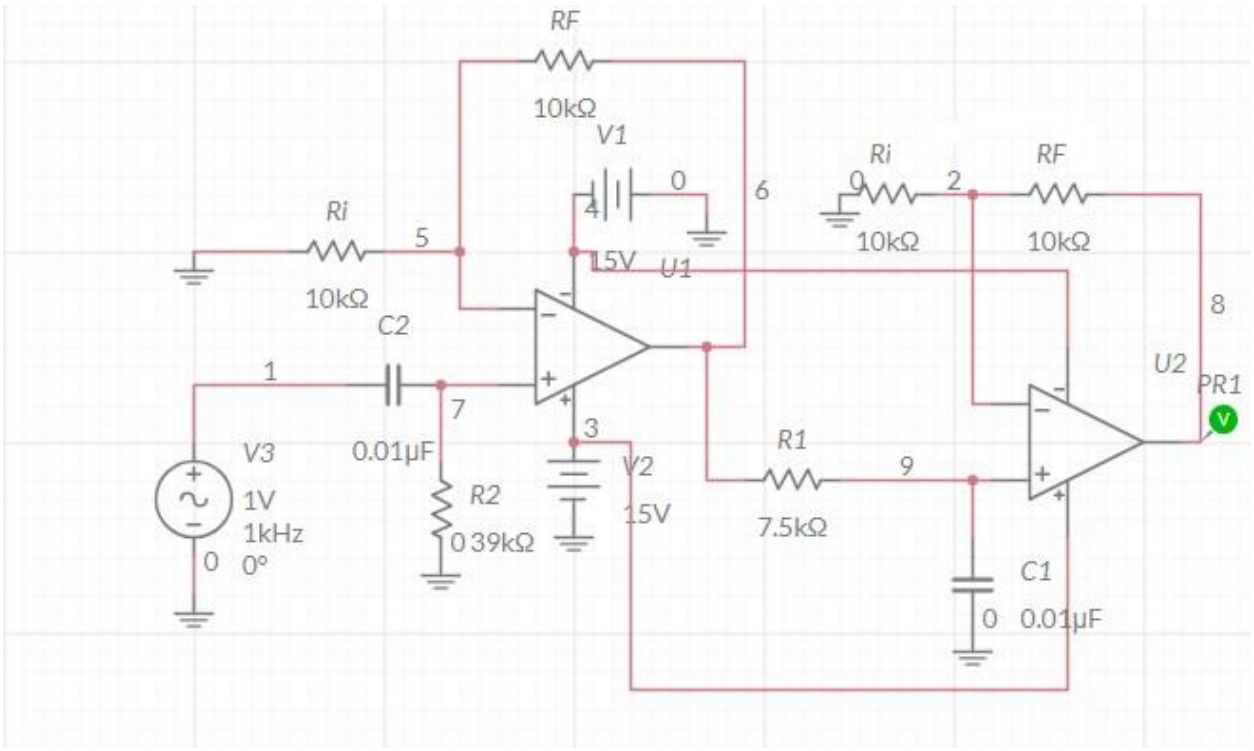
The BPF is the combination of high and low pass filters and this allows a specified range of frequencies to pass through. It has two stop bands in range of frequencies between 0 to $f_L$ and beyond $f_H$. The band b/w $f_L$ and $f_H$is called pass band. Hence its bandwidth is ($f_L$-$f_H$). This filter has a maximum gain at the resonant frequency ($f_{r)}$ which is defined as

$$f_r = \sqrt{f_H f_L}$$

The figure of merit (or) quality factor Q is given by

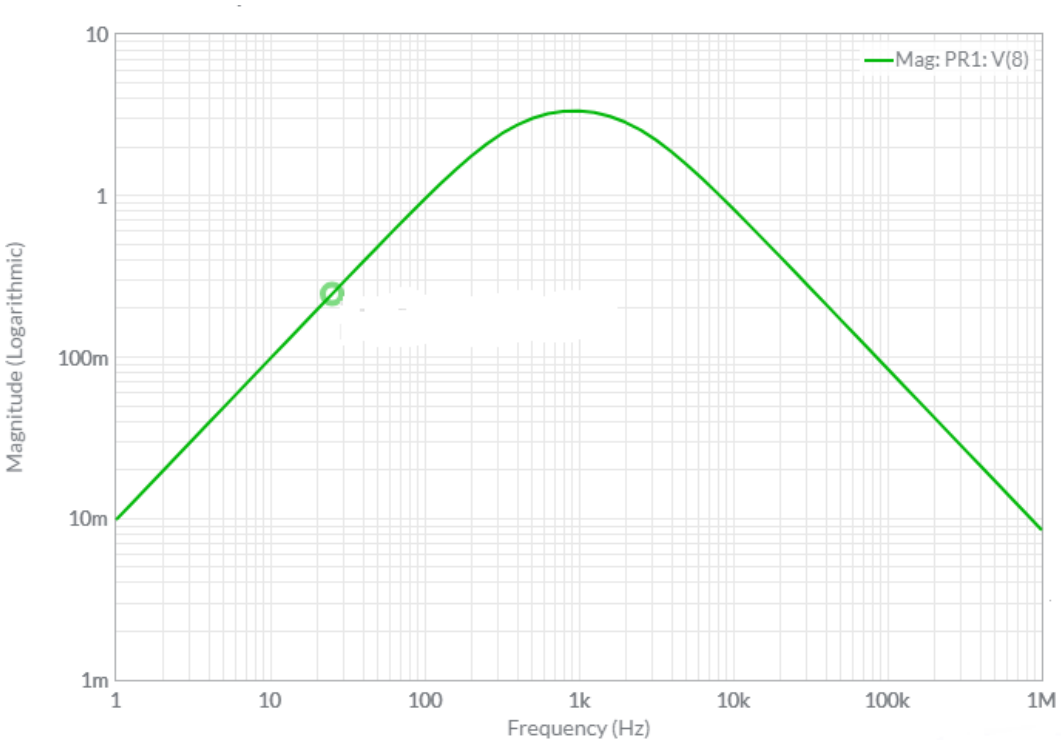
$$Q = \frac{f_r}{f_H - f_L} = \frac{f_r}{BW}$$

**Band Pass Filter Circuit:**




**HPF** **LPF**

**Output:**




**Result:**

## Exp.No: 5 Astable and MonostableMultivibrators using op-amp

Date:

**Aim:** To design Astable and Monostablemultivibrators using Op-amp and obtain duty cycle of the output.

**Apparatus Required:**

| S.No | Components | Specification | Quantity |
|---|---|---|---|
| 1. | Op-amp | µA741 | |
| 2. | Resistor | | |
| 3. | Capacitor | | |
| 4. | Regulated Power supply | | |
| 5. | Function Generator | | |
| 6. | CRO | | |
| | | | |
| | | | |

**Theory:**

**AstableMultivibrator**: The **Op-amp Multivibrator** is an astable oscillator circuit that generates a rectangular output waveform using an RC timing network connected to the inverting input of the operational amplifier and a voltage divider network connected to the other non-inverting input.

Unlike the monostable or bistable, the astablemultivibrator has two states, neither of which are stable as it is constantly switching between these two states with the time spent in each state controlled by the charging or discharging of the capacitor through a resistor.

However, because the open-loop op-amp comparator is very sensitive to the voltage changes on its inputs, the output can switch uncontrollably between its positive, +V(sat)and negative, -V(sat) supply rails whenever the input voltage being measured is near to the reference voltage, $V_{REF}$.

**Op-amp MonostableMultivibrator** (one-shot multivibrator) circuits are positive-feedback (or regenerative) switching circuits that have only one stable state, producing an output pulse of a specified duration T.

An external trigger signal is applied for it to change state and after a set period of time, either in microseconds, milliseconds or seconds, a time period which is determined by RC components, the

monostable circuit then returns back to its original stable state were it remains until the next trigger input signal arrives.

**Procedure:**

1. Make the connections as shown in the circuit diagram
2. Keep the CRO channel switch in ground and adjust the horizontal line on the x axis so that it coincides with the central line.
3. Select the suitable voltage sensitivity and time base on the CRO.
4. Check for the correct polarity of the supply voltage to op-amp and switch on power supply to the circuit.
5. Observe the waveform at the output and across the capacitor. Measure the frequency of oscillation and the amplitude. Compare with the designed value.
6. Plot the Waveform on the graph.

**Astable Multivibrator:**

**Design a square wave oscillator for $f_0$= 5 KHz .use a 741 Op-amp and DC supply voltage ±15V.**

$T = 2RC$

$R_1 = 1.16\ R_2$

Given $f_O$=_____KHz

Frequency of Oscillation fo = 1 / 2 RC if $R_1 = 1.16R_2$

Let $R_2 = 10\ K\Omega$

$R_1 = 10 * 1.16 = 11.6K\Omega$

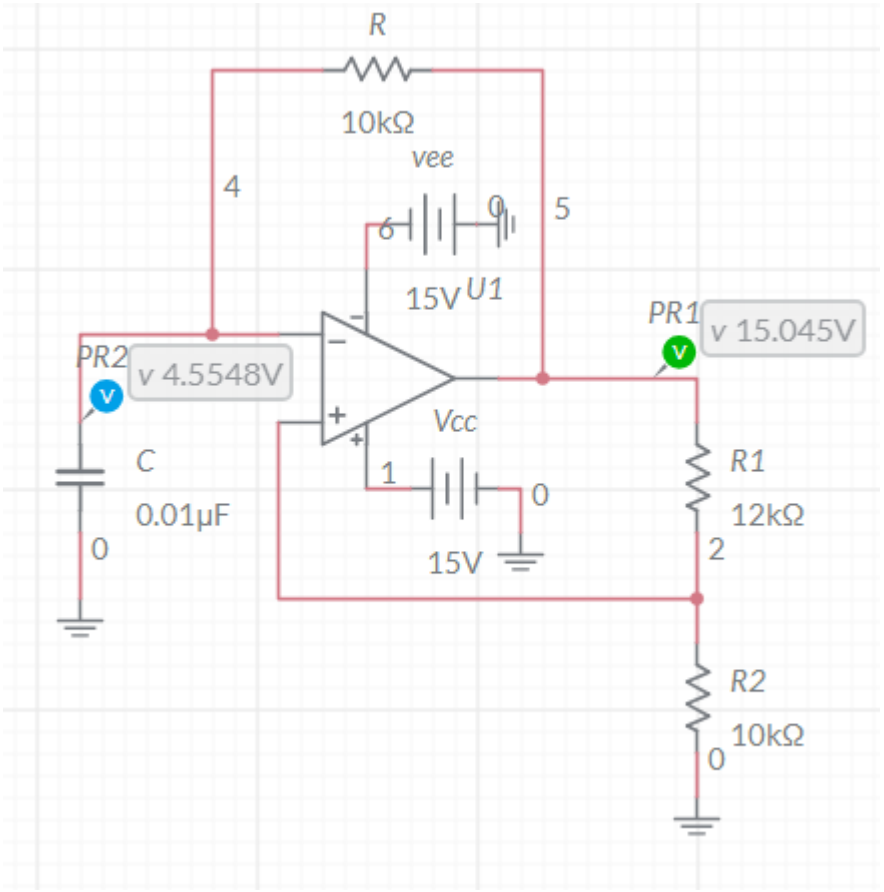
Let C = 0.01 μF

R = 1 / 2 fC =

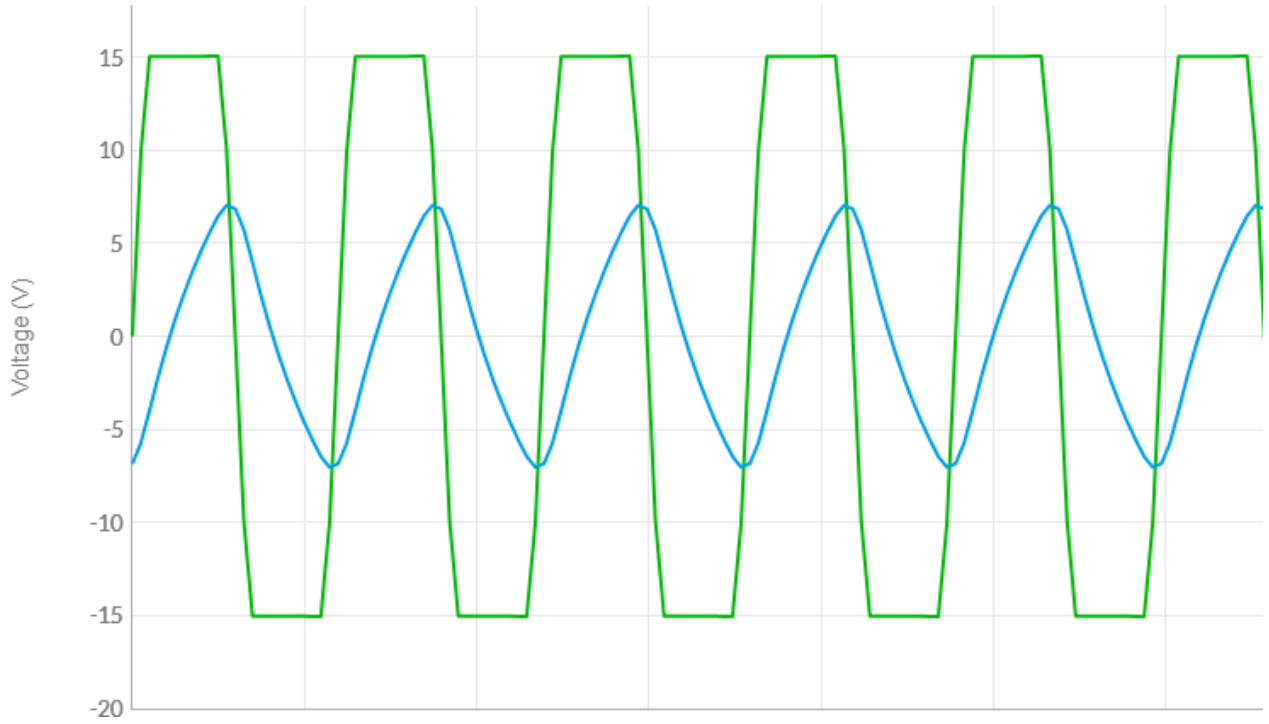
**Tabulation:**

| Output | Amplitude | Time | Frequency |
|---|---|---|---|
| **Square wave** | | | |
| **Voltage across capacitor** | | | |

**Astable Multivibrator Circuit:**



**Output:**




**Monostable Multivibrator:**

$\beta = R_2/R_1+R_2$ [$\beta = 0.5$ & $R_1 = 10$ K,]

Find $R_2$ = ; R = 5K; Rt = 1K;

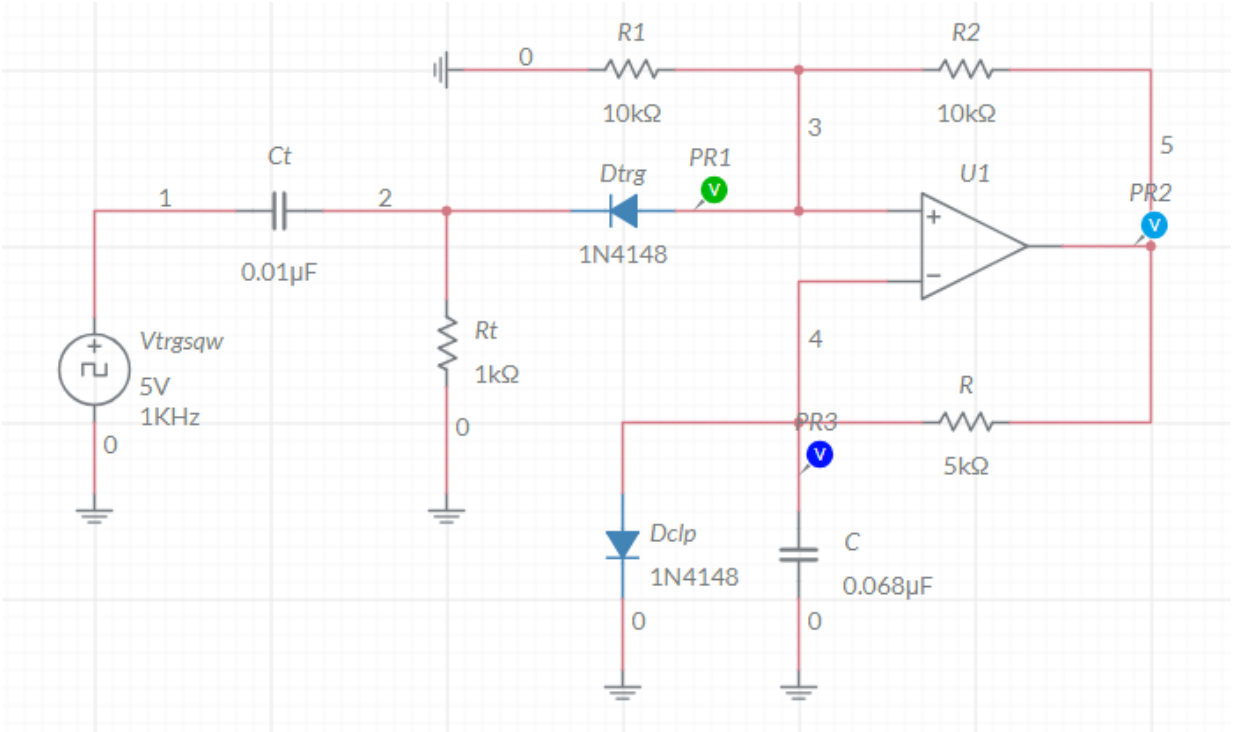
Let F =_____KHz ; C= 0.1µf; Ct = 0.01µf

Pulse width, T = 0.69RC

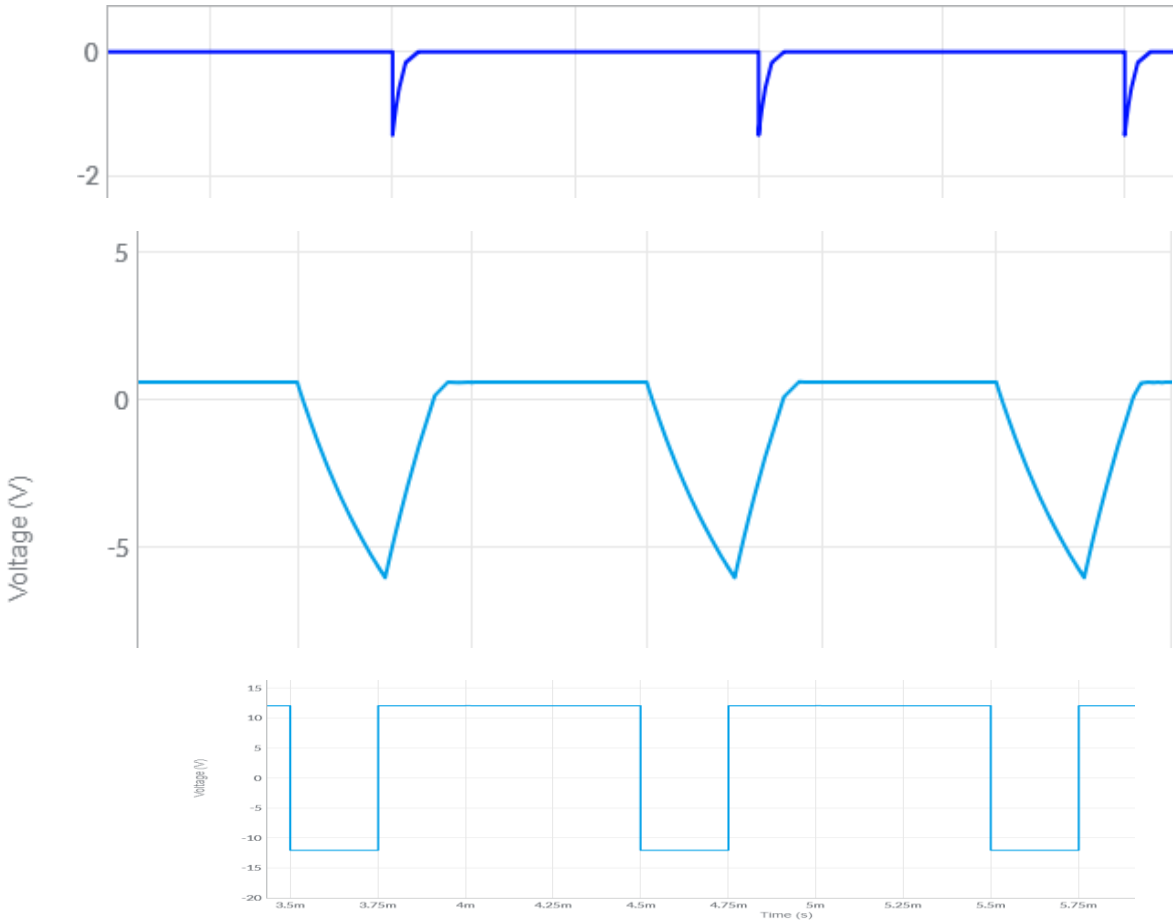
Find R =

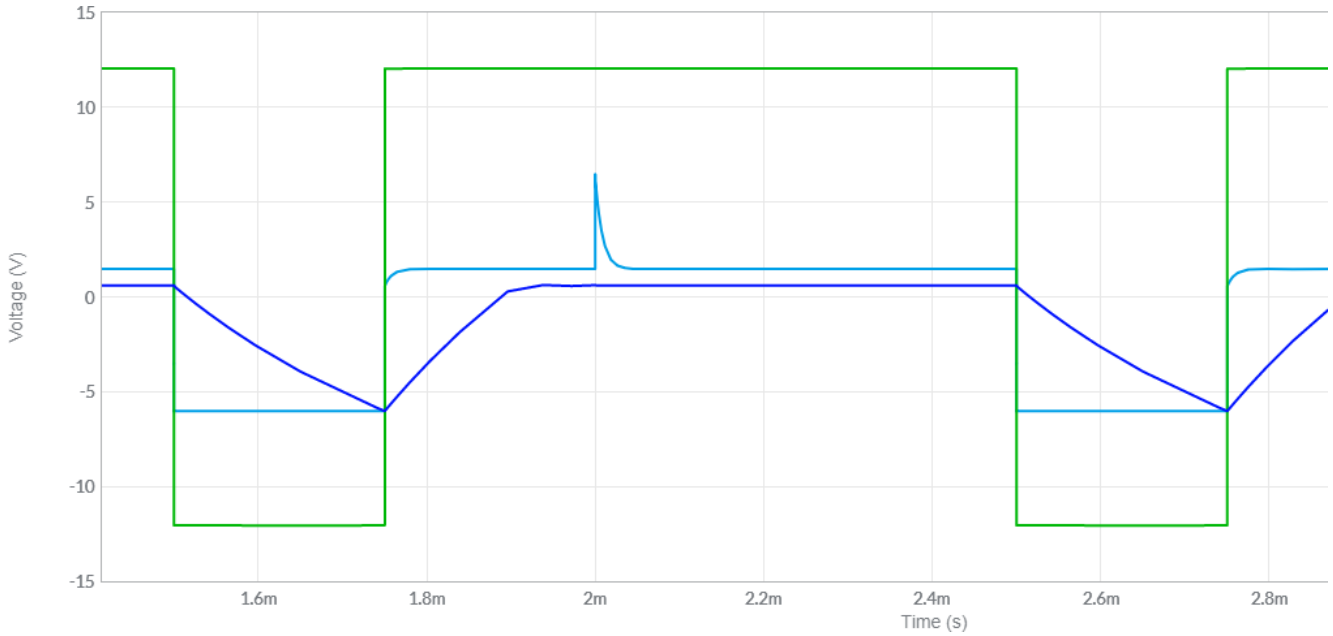
| Output | Amplitude | Time | Frequency |
|---|---|---|---|
| **Trigger Input** | | | |
| **Square wave** | | | |
| **Voltage across capacitor** | | | |

**Monostable Multivibrator Circuit:**



**Output :**




**Result:**

**Ex.No: 6** **Schmitt Trigger Using Op-amp**

**Date:**

**Aim: To design Schmitt trigger using Op-amp and analyze the output.**

**Apparatus Required:**

| S.No | Components | Specification | Quantity |
|---|---|---|---|
| 1. | Op-amp | µA741 | |
| 2. | Resistor | | |
| 3. | Capacitor | | |
| 4. | Regulated Power supply | | |
| 5. | Function Generator | | |
| 6. | CRO | | |
| | | | |

**Theory:**

If the input to a comparator contains noise, the output may be erratic ,when $v_{in}$ is near a trip point. For instance, with a zero crossing, the output is low when $v_{in}$ is positive and high when $v_{in}$ is negative. If the input contains a noise voltage with a peak of 1mV or more, then the comparator will detect the zero crossing produced by the noise. This can be avoided by using a Schmitt trigger, circuit which is basically a comparator with positive feedback. Because of the voltage divider circuit, there is a positive feedback voltage. When OPAMP is positively saturated, a positive voltage is feedback to the non-inverting input, this positive voltage holds the output in high stage. ($v_{in}<v_f$). If $V_{in}$ is less than $V_{ref}$ output will remain $+V_{sat}$. When input $v_{in}$ exceeds $V_{ref} = +V_{sat}$ the output switches from $+V_{sat}$ to $-V_{sat}$. Then the reference voltage is given by When the output voltage is negatively saturated, a negative voltage feedback to the inverting input, holding the output in low state. If $v_{in} <V_{ref}$ i.e. $v_{in}$ becomes more negative than $-V_{sat}$ then again output switches to $+V_{sat}$ and so on.

**Procedure:**

1. Connect the circuit as shown in the circuit
2. Set the input voltage as 5V (p-p) at 1KHz. (Input should be always less than $V_{cc}$)
3. Note down the output voltage at CRO
4. To observe the phase difference between the input and the output, set the CRO in dual Mode and switch the trigger source in CRO to CHI.
5. Plot the input and output waveforms on the graph.

**Design Problem:**

**To design a Schmitt trigger for $V_{UT}$ =+0.5V and $V_{LT}$= -0.5V and show it square wave output for input Vi = 2 $V_{PP}$ sine wave at 1 KHz.**

**Solution:**

**Assume $V_{ref}$ = 0 , Vsat = ±14V.**

$$V_{UT} = \frac{V_{Ref} R_1}{R_1 + R_2} + \frac{2\ V_{sat}}{R_1 + R_2}$$

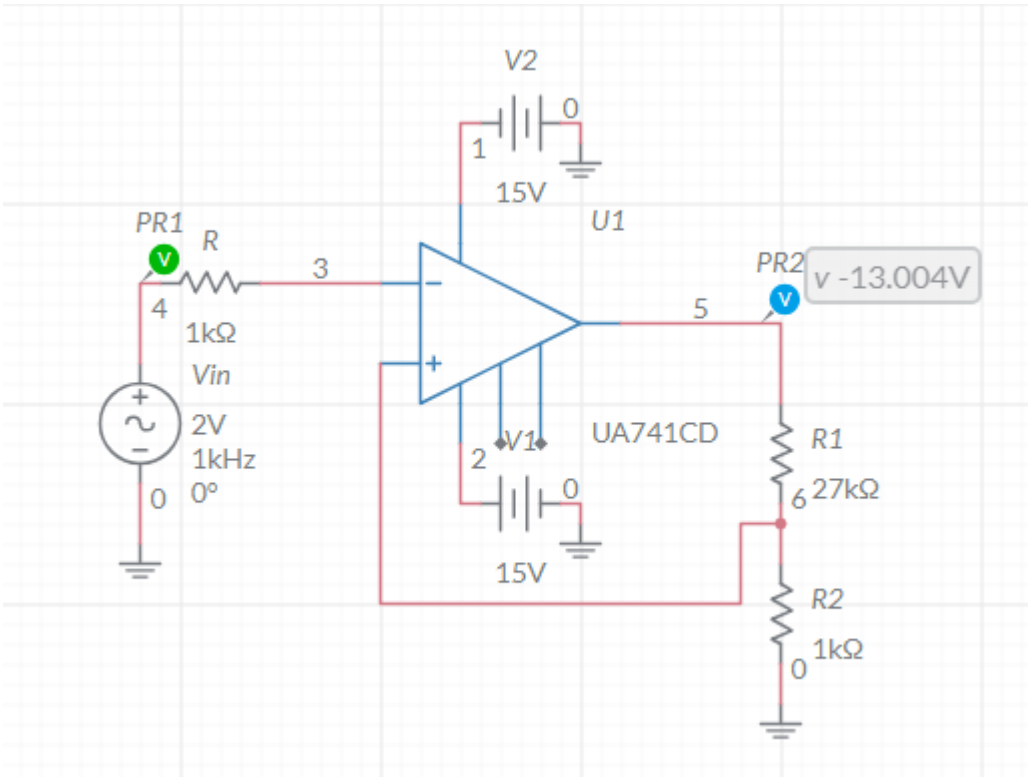
$$V_{LT} = \frac{V_{Ref} R_1}{R_1 + R_2} - \frac{2\ V_{sat}}{R_1 + R_2}$$

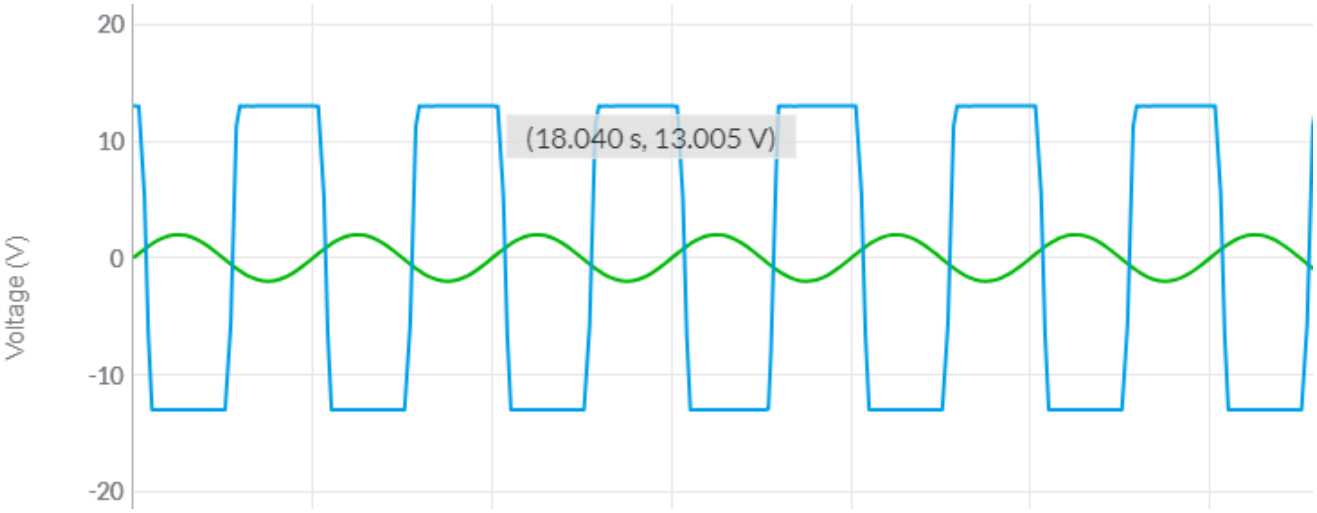
**$V_H$** = $V_{UT} - V_{LT}$

**Tabulation:**

| Input /Output | Amplitude | Frequency | Theoretical | | Practical | |
|---|---|---|---|---|---|---|
| | | | Amplitude | Frequency | Amplitude | Frequency |
| Sine | | | | | | |
| Square | | | | | | |

**Schmitt Trigger Circuit:**




**Result:**

**Ex.No: 7** **RC Phase shift and Wien Bridge Oscillators Using Op-amp**

**Date:**

**Aim: To design RC Phase shift and Wien Bridge Oscillators Using Op-amp.**

**Apparatus Required:**

| S.No | Components | Specification | Quantity |
|---|---|---|---|
| 1. | Op-amp | µA741 | |
| 2. | Resistor | | |
| 3. | Capacitor | | |
| 4. | Regulated Power supply | | |
| 5. | Function Generator | | |
| 6. | CRO | | |
| | | | |

**Theory:**

**RC Phase shift oscillator:**

The frequency at which a sinusoidal oscillator will operate is the frequency for which the total phase shift introduced, as the signal proceeds form the input terminals, through the amplifier and feed back network and back again to the input is precisely zero or an integral multiple of $2\pi$. Thus the frequency of oscillation is determined by the condition that the loop phase shift is zero and closed loop gain $A\beta \leq 1$. The above conditions are called Barkhausen criterion.

This op-amp is operated in inverting mode and hence the output signal of the op-amp is shifted by 180 degrees to the input signal appeared at inverting terminal. And an additional 180 degrees phase shift is provided by the RC feedback network and hence the condition for obtaining the oscillations.

The **Wien Bridge Oscillator** is so called because the circuit is based on a frequency-selective form of the Wheatstone bridge circuit. The Wien Bridge oscillator is a two-stage RC coupled amplifier circuit that has good stability at its resonant frequency, low distortion and is very easy to tune making it a popular circuit as an audio frequency oscillator but the phase shift of the output signal is considerably different from the previous phase shift **RC Oscillator**.

The **Wien Bridge Oscillator** uses a feedback circuit consisting of a series RC circuit connected with a parallel RC of the same component values producing a phase delay or phase advance circuit depending upon the frequency. At the resonant frequency $f$r the phase shift is $0^o$

**Procedure:**

1. Connect the circuits as shown in the circuit.
2. Switch on the power supply.
3. Note down the output voltage on the CRO.
4. Plot the output waveforms on the graph.
5. Redesign the circuit to generate the sine wave of 1 KHz.
6. Plot the output waveform on the graph.
7. Compare the practical value of the frequency with the theoretical value.

**Problem:**

**Design RC Phase shift oscillator to produce sine wave at 2 KHz.**

**Solution:**

**For RC Phase shift oscillator**

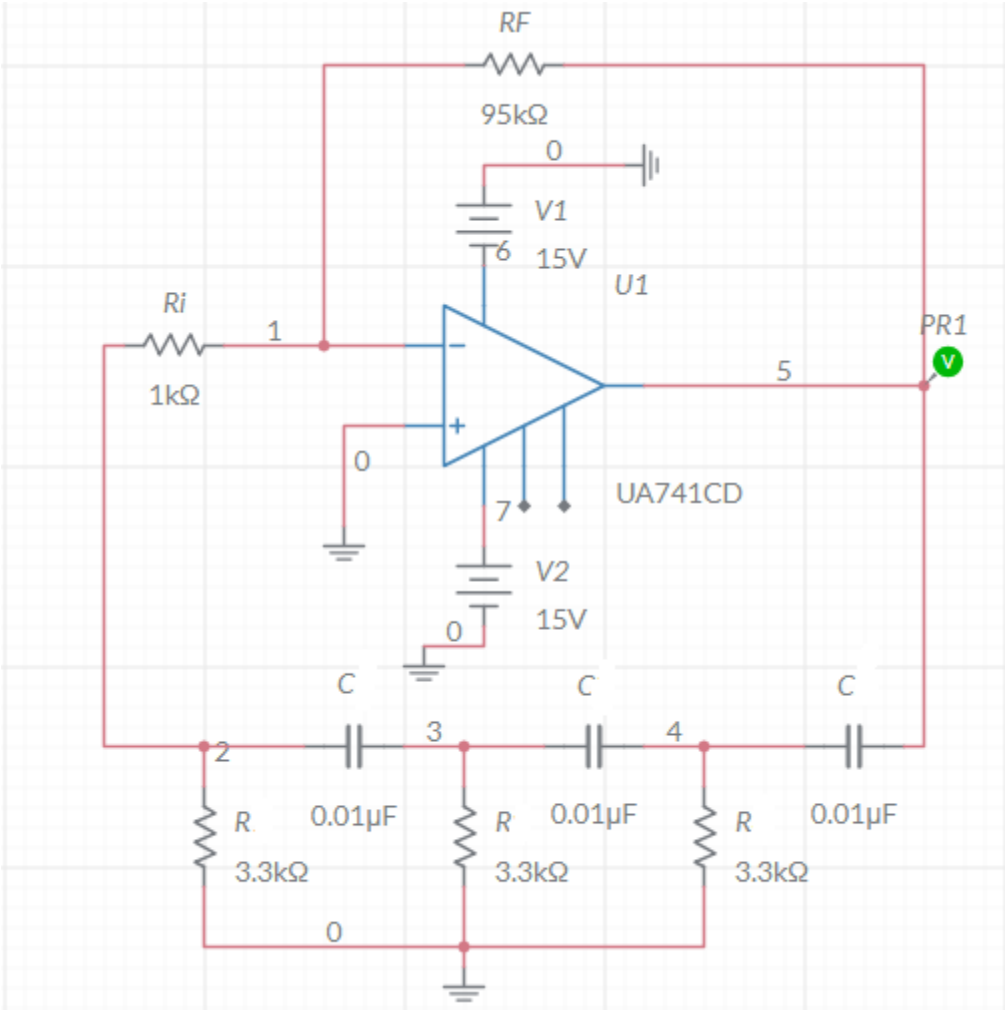
$$f_o = \frac{1}{2\pi RC\sqrt{2N}}$$

- Where:
- $f_o$ is the Output Frequency in Hertz
- R is the Resistance in Ohms
- C is the Capacitance in Farads
- N is the number of RC stages. (N = 3)

$$f_o = \frac{1}{2\pi RC\sqrt{6}}$$

**Choose C=0.01µF ,** $ain = A_V = \frac{F}{R}$ **and** $A_V \geq 29$

**RC Phase Shift Oscillator Circuit:**




**Output:**

**Problem:Design Wien bridge oscillator for generate 5KHz sine wave.**

**Design:**

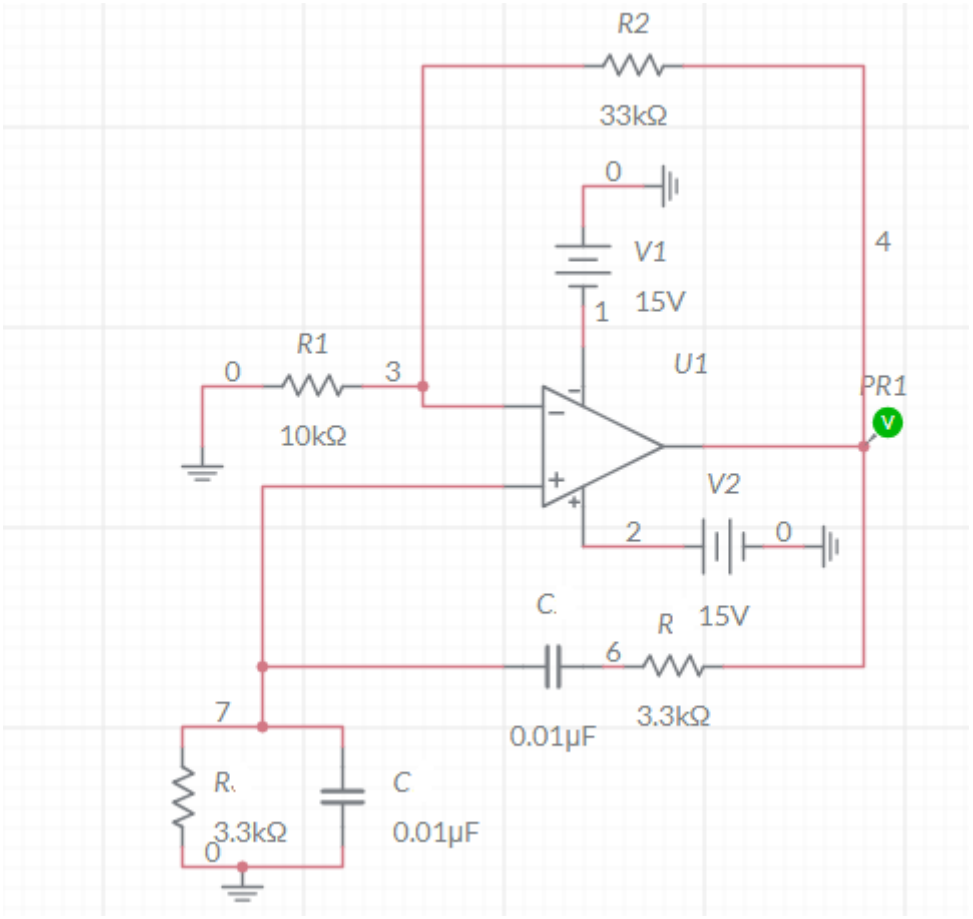
Gain required for sustained oscillation is $A_v = 1/\beta = 3$

(PASS BAND GAIN) (i.e.) $1+R_f/R_1 = 3$

$\therefore R_f = 2R_1$

Frequency of Oscillation $f_o = 1/2\pi$ R C, Let C=0.01 $\mu$F

**Wien Bridge oscillator Circuit:**




**Output:**


**Result:**

**Ex.No: 8** **Astable and Monostble Multivibrator using IC555**

**Date:**

**Aim: To design Astable and Monostable multivibrator using 555 timer.**

**Apparatus Required:**

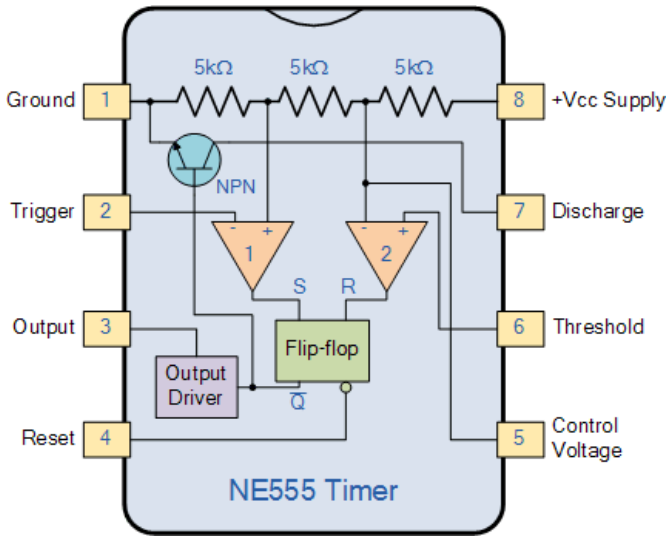
| S.No | Components | Specification | Quantity |
|---|---|---|---|
| 1. | Timer IC | IC555 | |
| 2. | Resistor | | |
| 3. | Capacitor | | |
| 4. | Regulated Power supply | | |
| 5. | Function Generator | | |
| 6. | CRO | | |
| | | | |

**Theory: IC 555 Timer**

The basic **555 timer** gets its name from the fact that there are three internally connected 5kΩ resistors which it uses to generate the two comparators reference voltages. The 555 timer IC is a very cheap, popular and useful precision timing device which can act as either a simple timer to generate single pulses or long time delays, or as a relaxation oscillator producing a string of stabilised waveforms of varying duty cycles from 50 to 100%.

The 555 timer chip is extremely robust and stable 8-pin device that can be operated either as a very accurate Monostable, Bistable or AstableMultivibrator to produce a variety of applications such as one-shot or delay timers, pulse generation, LED and lamp flashers, alarms and tone generation, logic clocks, frequency division, power supplies and converters etc,

### 555 Timer Block Diagram



**Design Astable Multivibrator for $R_A$=2.2KΩ,$R_B$=3.9KΩ and C=0.1μF.Determine the positive pulse width $t_c$, negative pulse width $t_d$ and free running frequency $f_o$.**

**Solution:**

The capacitor is periodically charged and discharged between 2/3 $V_{cc}$ and 1/3 $V_{cc}$ respectively. The time during which the capacitor charges form 1/3 $V_{cc}$ to 2/3 $V_{cc}$ is equal to the time the output is high and is given by

$$\mathbf{T_c = 0.69(R_A+R_B)C}$$

Where $R_A$ and $R_B$ are in Ohms and C is in farads. Similarly the time during which the capacitor discharges from 2/3 $V_{cc}$ to 1/3 $V_{cc}$ is equal to the time the output is low and is given by

$$\mathbf{T_d = 0.69\ R_BC}$$

The total period of the output waveform is

$$\mathbf{T = T_c + T_d = 0.69\ (R_A + 2R_B)\ C}$$

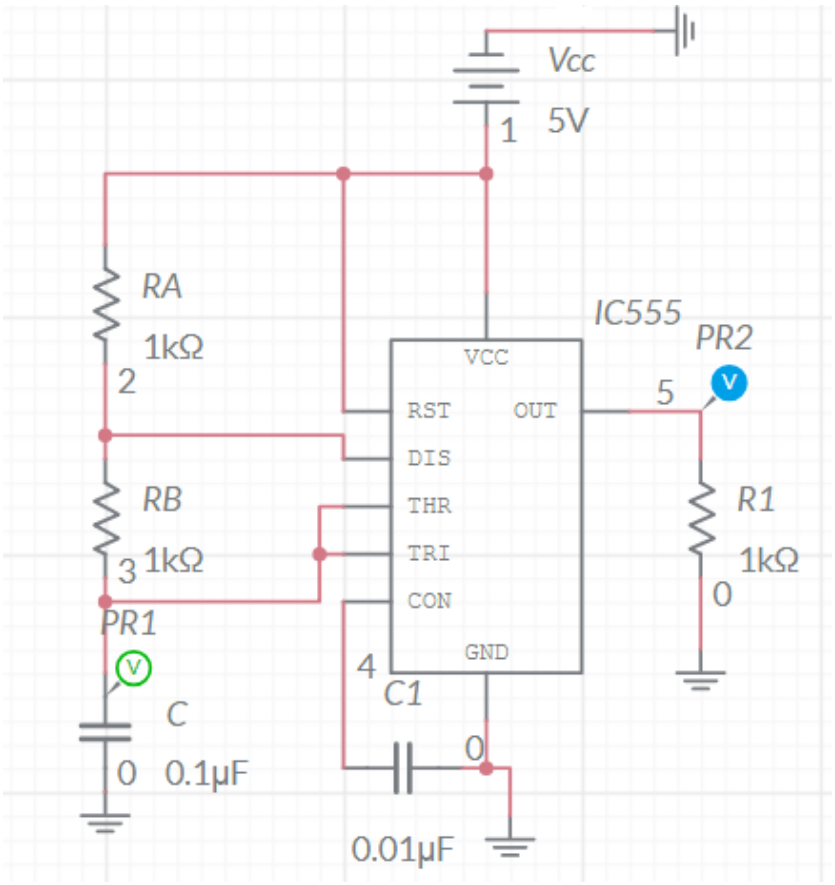
The frequency of oscillation

$$f_o = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C} \times 100$$

$$\%of\ Duty\ Cycle = \frac{t_c}{T} \times 100$$

$$= \frac{_A + R_B}{R_A + 2R_B} \times 100$$

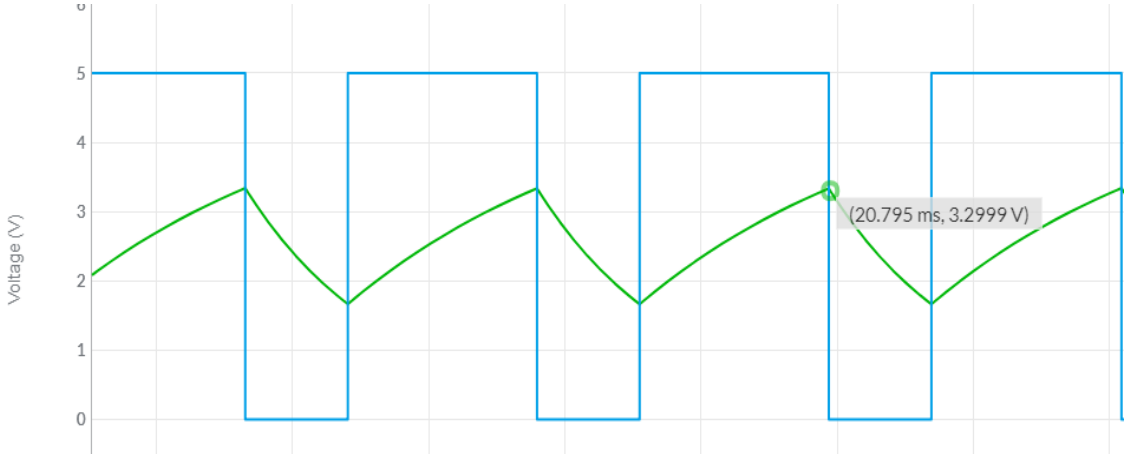
**Astable Multivibrator Circuit:**




**Tabulation:**

| | Amplitude | Time | Frequency |
|---|---|---|---|
| **Output** | | | |
| **Capacitor Voltage** | | | |

**Output:**

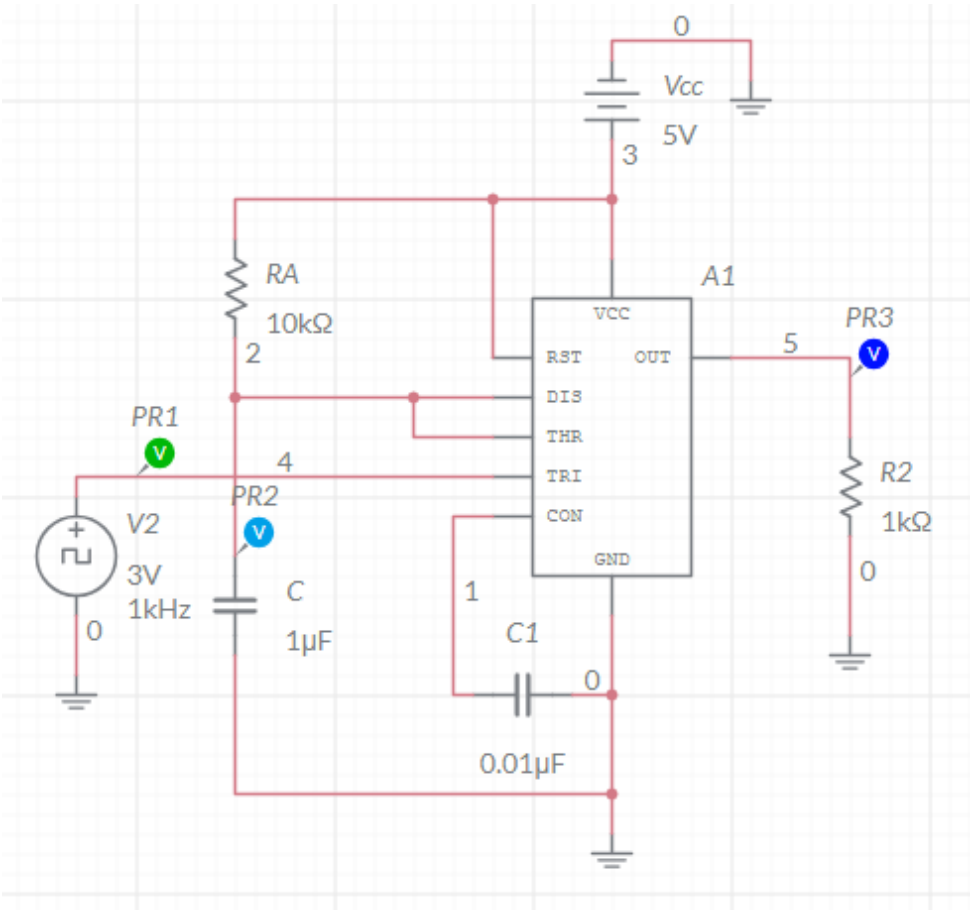


**Design Monostable multivibrator for $R_A$=10KΩ and the output pulse width $t_p$=10ms.Find C.**

The pulse width of the trigger input must be smaller than the expected pulse width of the output. The trigger pulse must be of negative going signal with amplitude larger than 1/3 Vcc. The width of the output pulse is given by,

$$t_p = 1.1\ R_A C$$

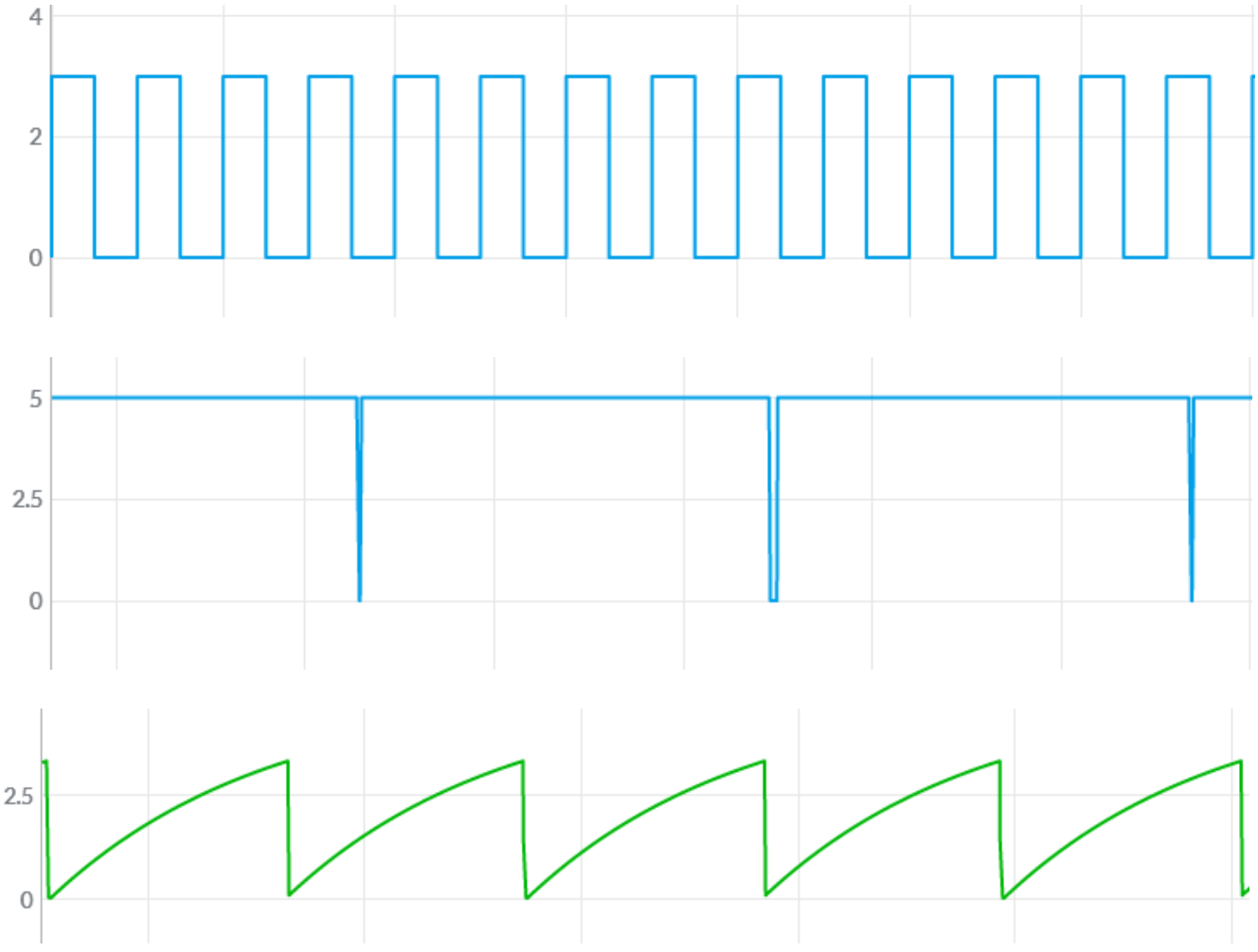
**Monostable Multivibrator Circuit:**

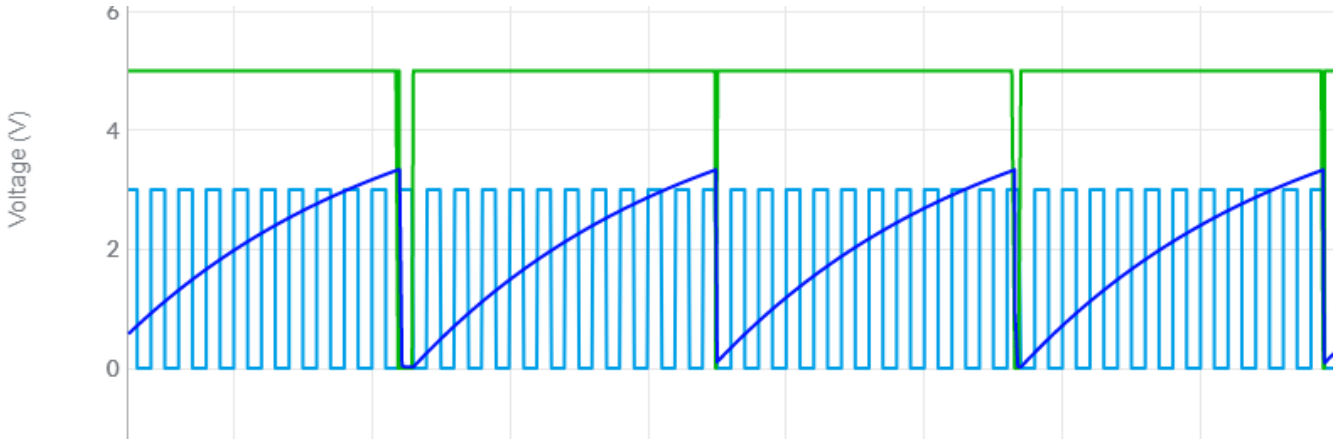


**Tabulation:**

| | Amplitude | Time | Frequency |
|---|---|---|---|
| **Trigger Input** | | | |
| **Output** | | | |
| **Capacitor Voltage** | | | |

**Output:**






**Result:**

**Ex.No: 9 PLL characteristics and its use as Frequency Multiplier, Clock synchronization.**

**Date:**

**Aim:**

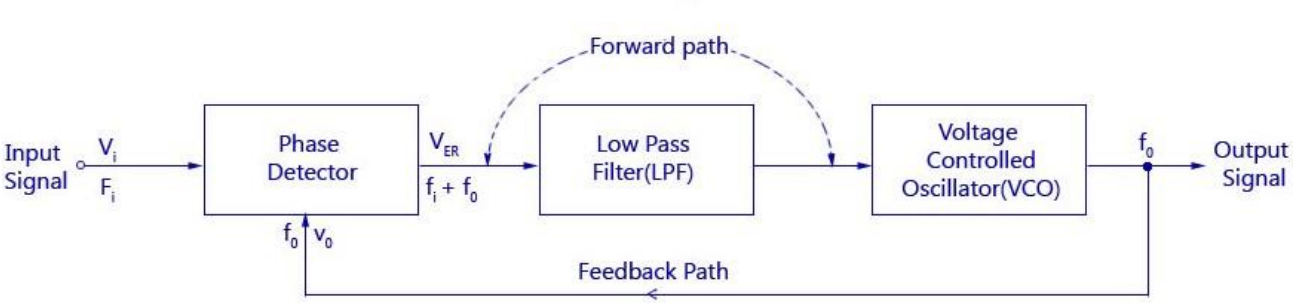
1. **To study the PLL characteristics.**
2. **To use PLL as frequency multiplier and clock synchronization.**

**Apparatus Required:**

| S.No | Components | Specification | Quantity |
|---|---|---|---|
| 1. | PLL | IC565 | |
| 2. | Resistor | | |
| 3. | Capacitor | | |
| 4. | Regulated Power supply | | |
| 5. | Function Generator | | |
| 6. | CRO | | |
| | | | |

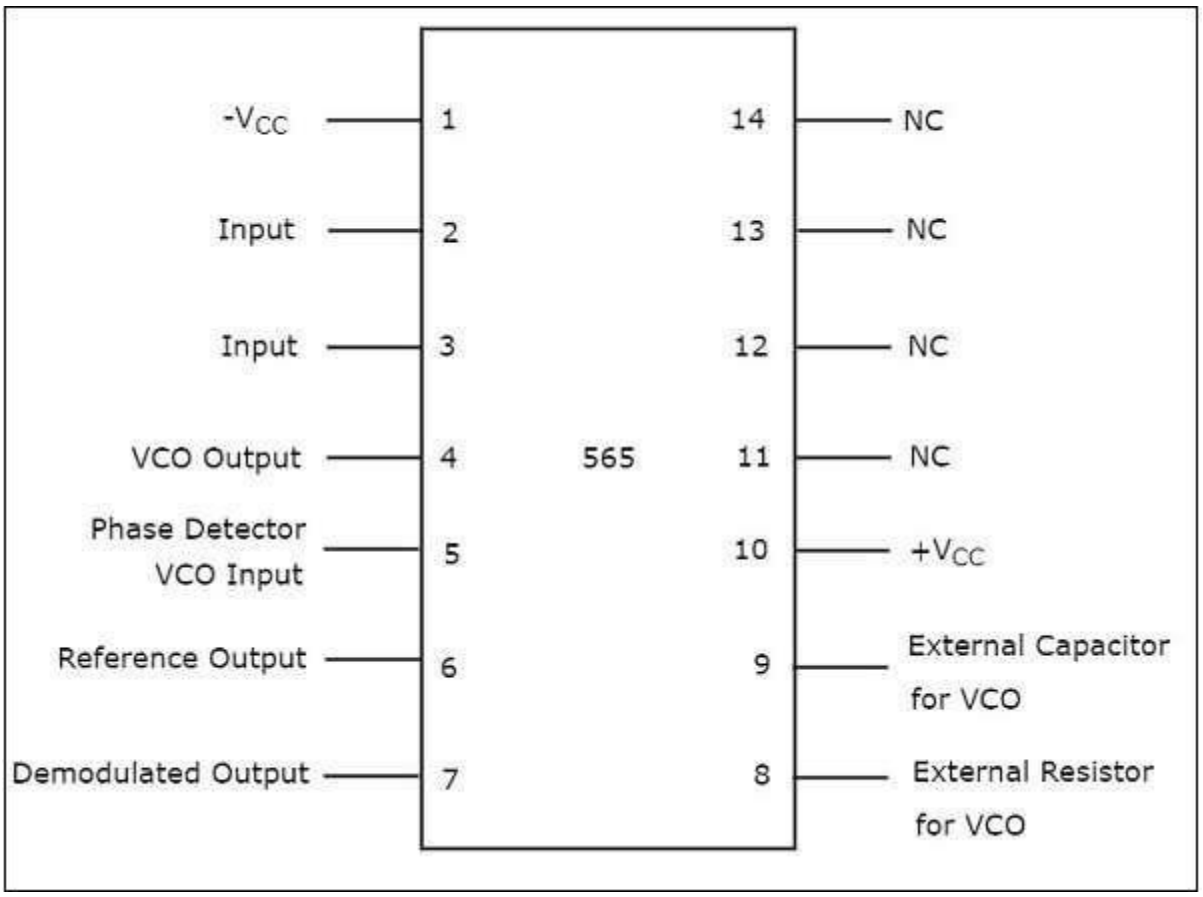
**Theory:**

The PLL IC 565 is usable over the frequency range 0.1 Hz to 500 kHz. It has highly stable centre frequency and is able to achieve a very linear FM detection. The output of VCO is capable of producing TTL compatible square wave. The dual supply is in the range of ±6V to ±12V. The IC can also be operated from single supply in the range 12V to 24V.




The phase locked loop consists of a phase detector, a voltage control oscillator and, in between them, a low pass filter is fixed. The input signal „Vi" with an input frequency „Fi" is conceded by a phase detector. Basically the phase detector is a comparator which compares the input frequency fi through the feedback frequency fo. The output of the phase detector is (fi+fo) which is a DC voltage. The out of the phase detector, i.e., DC voltage is input to the low pass filter (LPF); it removes the high frequency noise and produces a steady DC level, i.e., Fi-Fo. The Vf is also a dynamic characteristic of the PLL.

The following figure shows the pin-out and the internal block schematic of PLL IC LM 565.




**Design:**

Center frequency or VCO frequency

$$f_{out} = \frac{1.2}{4R_1C_1} \text{ Hz}$$

$$Lock\ in\ range = f_L = \pm 8\frac{f_{out}}{V} \quad ; \quad V = V^+ - (V^-)$$

$$Capture\ range = f_C = \pm\left[\frac{f_L}{2\pi \times 3.6 \times 10^3 \times C_2}\right]^{\frac{1}{2}}$$

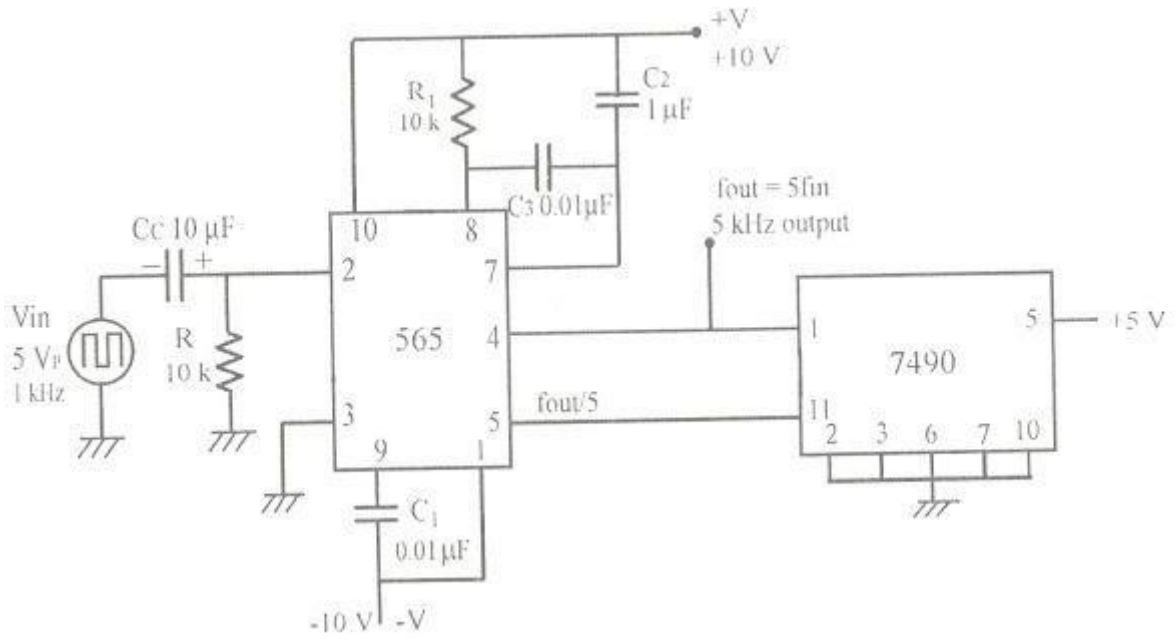
**PLL Characteristics Circuit:**

**PLL characteristics:**

**PLL used as Frequency Multiplier:**

## Design:

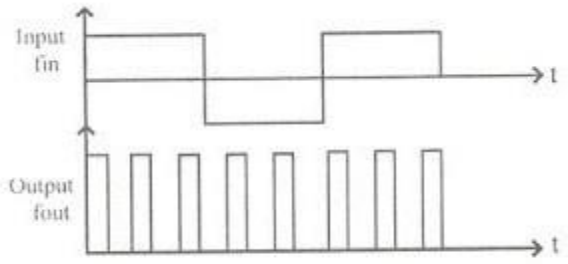
Let V+ =10 V and V- = -10
Let the input frequency be 1 Khz, and the output frequency 5 Khz,
VCO should run at 5 Khz frequency , fo=(1.2/4*R1*C1)=5Khz
Take C1=0.01µF Then R1=6K
Take C2=10µF and C3=0.001µF
use Cc=10µF and R=10k for ac coupling of input signal



## Procedure:

- Check the component using multi meter
- setup the circuit stage by stage on the breadboard
- verify the working of circuit separately.
- complete the circuit and apply 5V p-p ,1Khz square wave
- observe the multiplied frequency output on the CRO
- plot the output wave form on the graph sheet

## Output waveform:




**Result:**

**Ex.No: 10** **R-2R Ladder Type D- A Converter using Op-amp.**

**Aim:**

**To design R-2R Ladder Type D- A Converter using Op-amp and observe the output.**

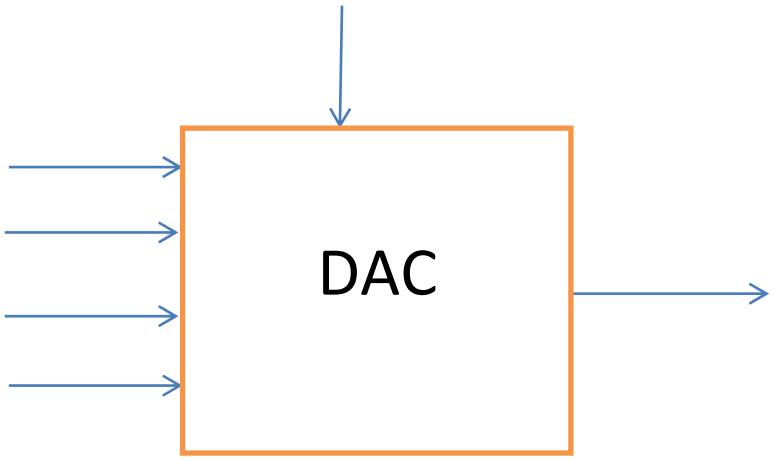
**Apparatus required:**

| S.No | Components | Specification | Quantity |
|---|---|---|---|
| 1. | Op-amp | | |
| 2. | Resistor | | |
| 3. | Regulated Power supply | | |
| 4. | DC power supply | | |
| 5. | Multimeter | | |
| | | | |

**Theory:**

A digital-to-analog converter (DAC, D/A, D2A or D-to-A) is a circuit that converts digital data (usually binary) into an analog signal (current or voltage). One important specification of a DAC is its resolution. It can be defined by the numbers of bits or its step size. Wide range of resistors used Weighted Resistor type DAC. This can be avoided by using R-2R ladder type DAC where only two values of resistors are required.

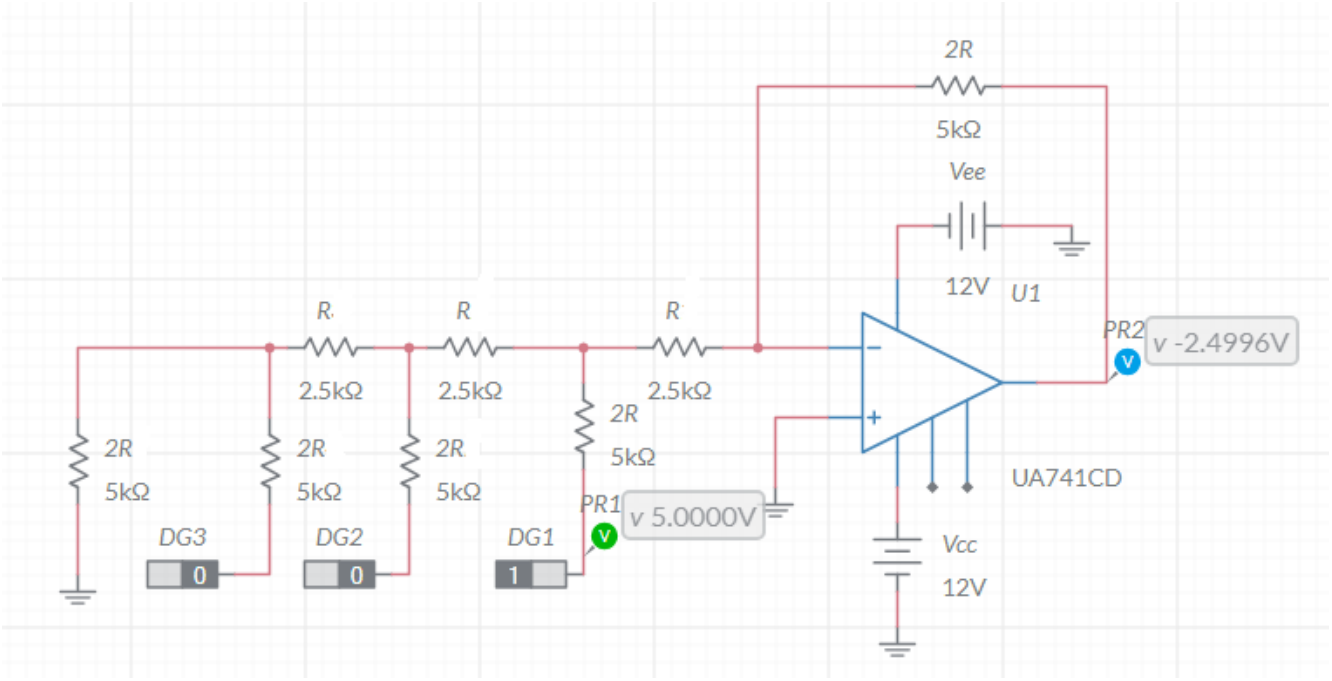
Basic Block diagram of DAC.




The output voltage of DAC;

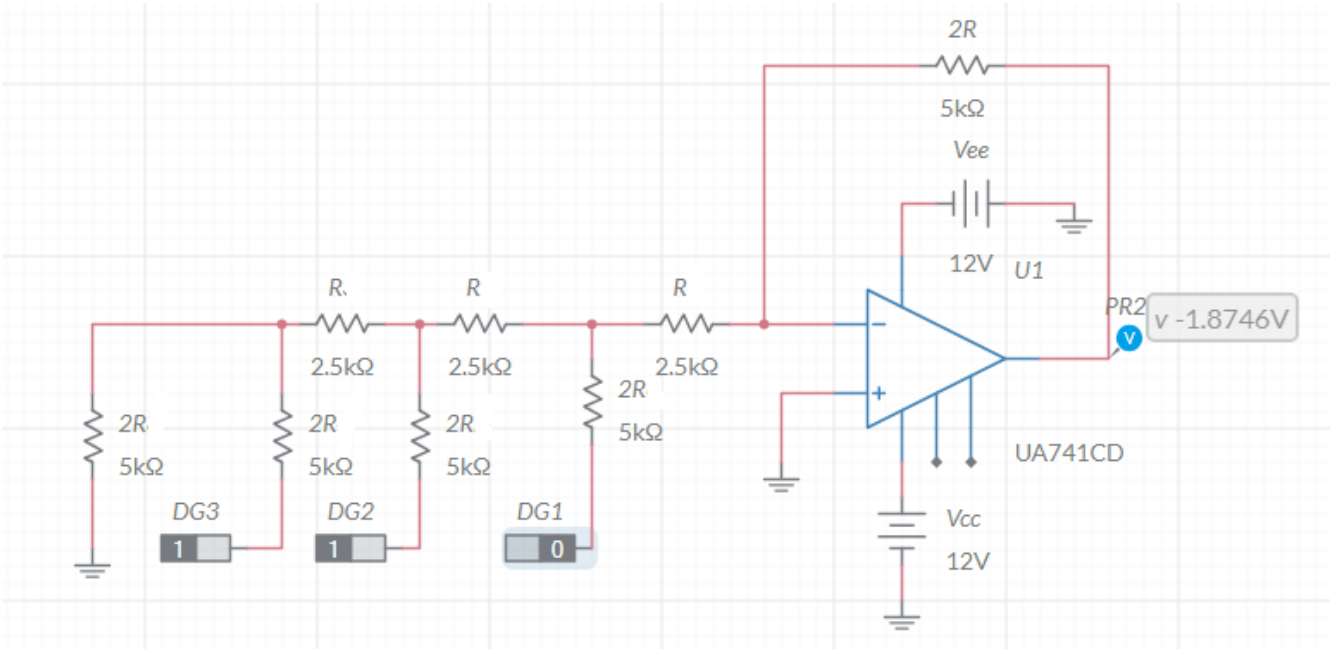
$$V_0 = KV_F(d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n})$$

**To design 3 bit R-2R Digital to Analog converter to convert analog voltage of binary bit 100.**




**Theoretical Calculation:**

**If binary bit 011 :**




**Tabulation:**

**Vref = -5V**

| d1 | d2 | d3 | Theoretical V0 | Practical V0 |
|---|---|---|---|---|
| 0 | 0 | 0 | | |
| 0 | 0 | 1 | | |
| 0 | 1 | 1 | | |
| 0 | 1 | 1 | | |
| 1 | 0 | 0 | | |
| 1 | 0 | 1 | | |
| 1 | 1 | 0 | | |
| 1 | 1 | 1 | | |

## Procedure:

- Check the component using multi meter.
- Setup the circuit stage by stage on the breadboard
- Verify the working of circuit separately.
- Complete the circuit and apply -5V ref if bit=1.
- Observe the output using multimeter.
- Plot the output wave form on the graph sheet.

## Result:

**Ex.No: 11** **DC power supply using LM317 and LM723.**

**Aim:**

**To design DC power supply using LM 317 and LM 723.**

**Apparatus required:**

| S.No | Components | Specification | Quantity |
|---|---|---|---|
| 1. | Voltage regulator IC | | |
| 2. | Resistor | | |
| 3. | Capacitor | | |
| 4. | Regulated Power supply | | |
| 5. | Multimeter | | |
| | | | |

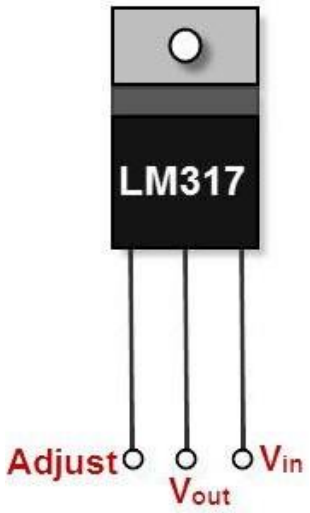
**Theory:**

The power supply received at the load end or consumer end has fluctuations in the voltage levels due to irregular loads or based condition of the local power grid. These voltage fluctuationsmay lead to the reduction of lifespan ofthe electrical and electronic appliances of the consumer or damage to the loads. So, it is required to protect loads from over and under voltages or need to provide a constant voltage to the loads and to maintain stability in system voltage using regulation technique. Voltage regulation can be defined as maintaining constant voltage or maintaining the voltage level of a system within acceptable limits over a wide range of load conditions and thus, voltage regulators are used for voltage regulation. For linear voltage regulation, occasionally adjustable LM317 voltage regulators are used wherein non-standard voltage is intended.

**Voltage Regulator**

## LM317 Voltage Regulator

It is a type of positive-linear-voltage regulators used for voltage regulation, which is invented by Robert C. Dobkin and Robert J. Widlar while they worked at National Semiconductor in 1970. It is a three-terminal-adjustable-voltage regulator and is easy to use because to set the output voltage it requires only two external resistors in LM317 voltage regulator circuit. It is majorly used for local and on card regulation. If we connect a fixed resistor between the output and adjustment of LM317 regulator, then the LM317 circuit can be used as a precise current regulator.

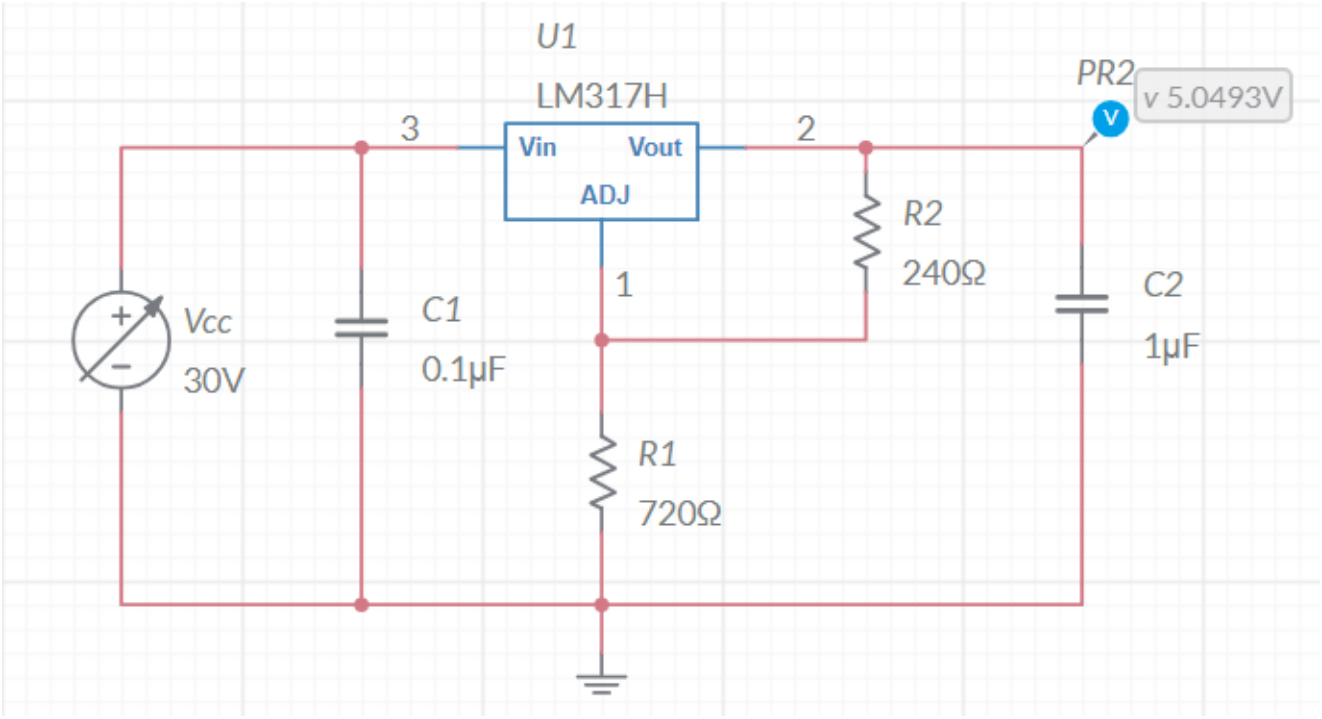



The three terminals are input pin, output pin and adjustment pin. The LM317 circuit is shown in the below figure is a typical configuration of the LM317 voltage regulator circuit diagram including the decoupling capacitors. This LM317 circuit is capable to provide variable DC power supply with output of 1A and can be adjusted up to 30V.

**Design a DC power supply for a constant output voltage 5V using LM317.**

$$V_{out} = 1.25(1 + \frac{R_2}{R_1}) + I_{adj}R_2$$

**LM317 Voltage Regulator Circuit:**




**Tabulation:**

| **Line Regulator** | | **Load Regulator** | |
|---|---|---|---|
| **Vin** | **Vo** | **$R_{adj}$** | **Vo** |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

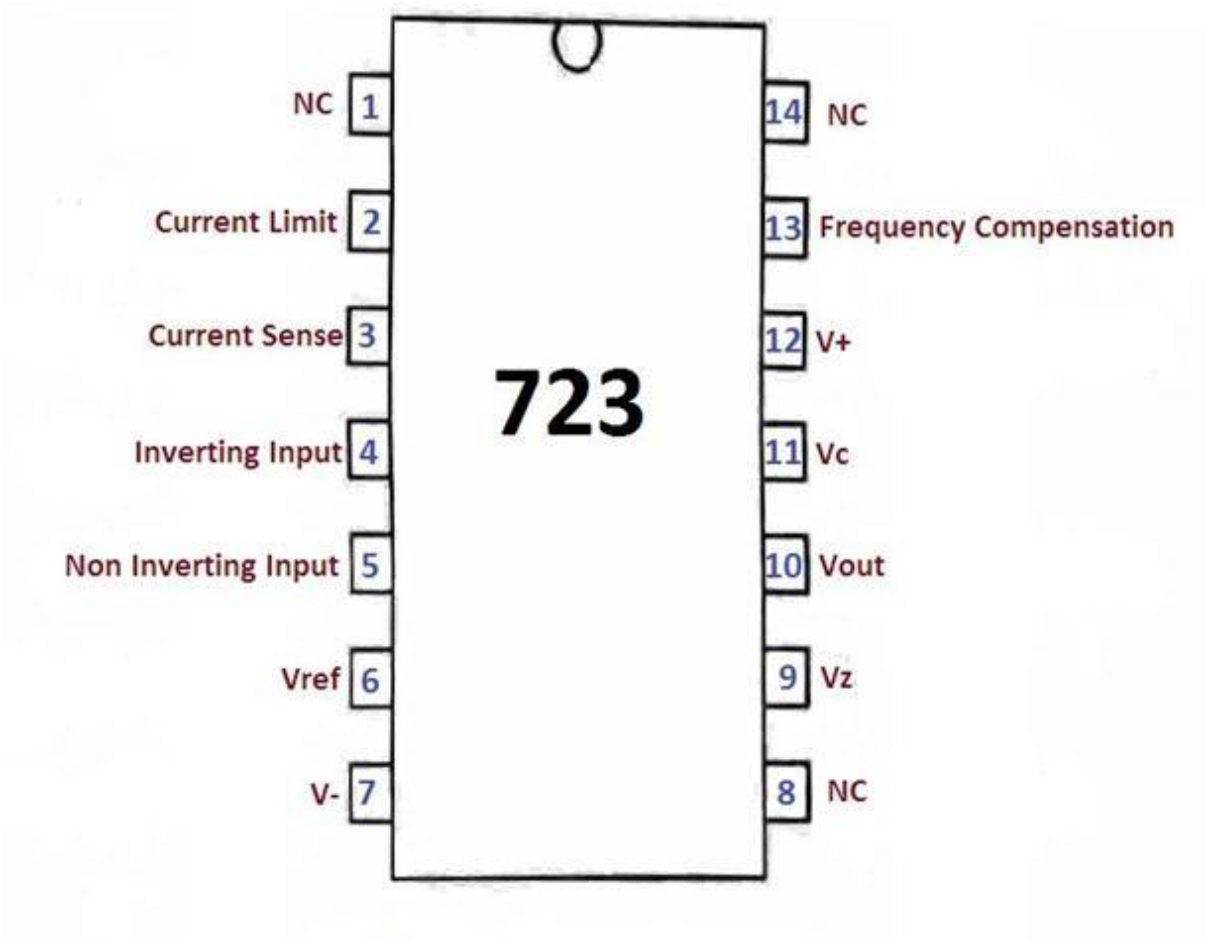
## IC723 Voltage regulator:

The 723 voltage regulator is commonly used for series voltage regulator applications. It can be used as both positive and negative voltage regulator. It has an ability to provide up to 150 mA of current to the load, but this can be increased more than 10A by using power transistors. It also comes with comparatively low standby current drain, and provision is made for either linear or fold-back current limiting. LM723 IC can also be used as a temperature controller, current regulator or shunt regulator and it is available in both Dual-In-Line and Metal Can packages. The input voltage ranges from 9.5 to 40V and it can regulate voltage from 2V to 37V.

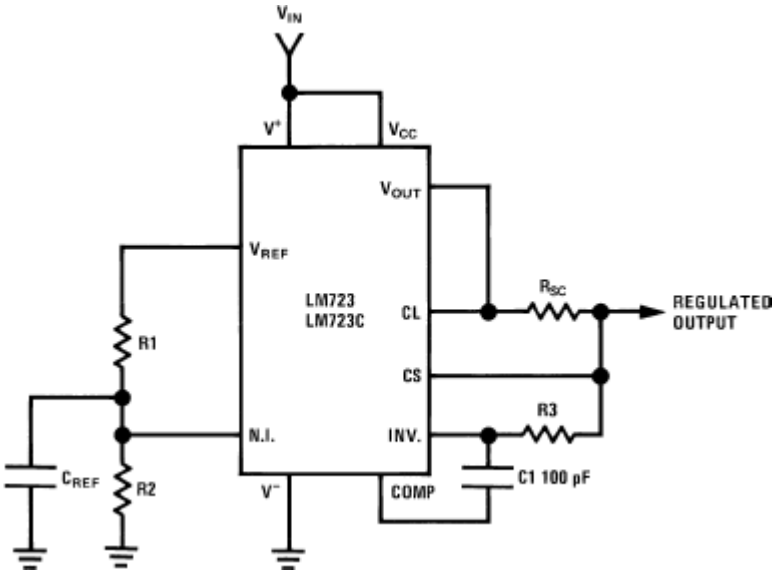
### Features of 723 Voltage Regulator

- 150 mA output current without external pass transistor
- Output currents in excess of 10A possible by adding external transistors
- Input voltage 40V max
- Output voltage adjustable from 2V to 37V
- Can be used as either a linear or a switching regulator

### PIN Layout



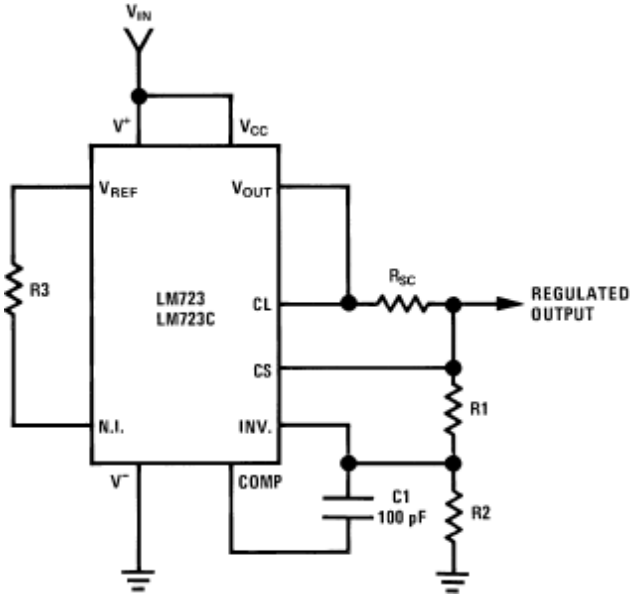
**LM723 Low Voltage Regulator:**




**Note:** $R_3 = \frac{R_1 R_2}{R_1 + R_2}$

**Regulated Output Voltage 2 to 7 V.**

## IC723 High Voltage Regulator:



**Tabulation:**

| Line Regulator | | Load Regulator | |
|---|---|---|---|
| **Vin** | **Vo** | **$R_{adj}$** | **Vo** |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

**Result:**

**Ex.No: 12** **Study of SMPS**

**Aim:**

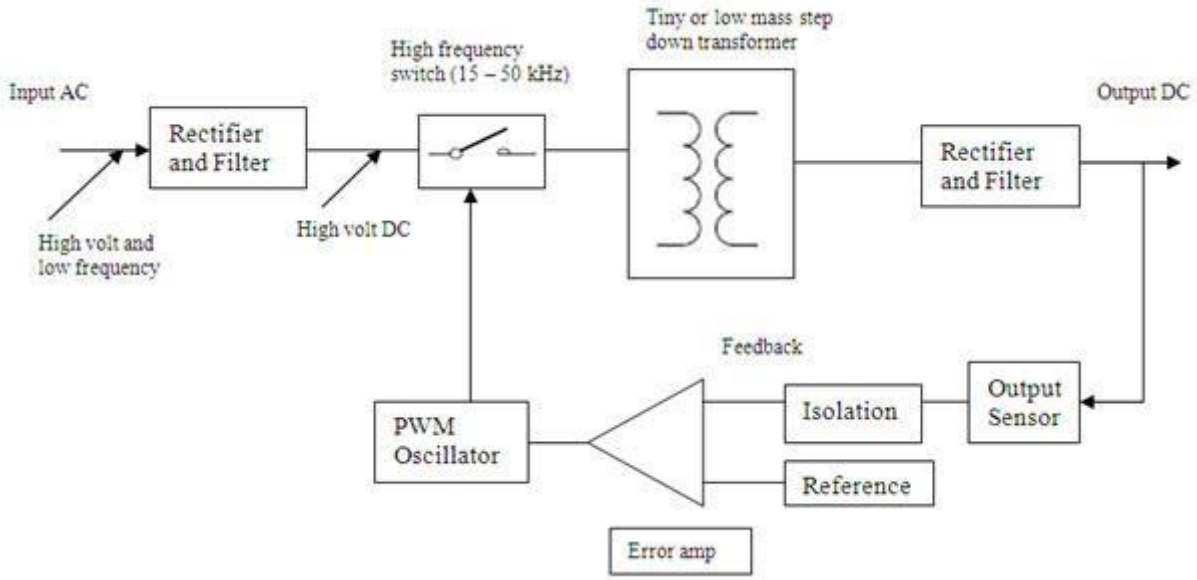
**To study the working of Switched mode power supply (SMPS) .**

**Theory of SMPS:**

Switched Mode Power Supply (SMPS) Like a linear power supply, the switched mode power supply too converts the available unregulated ac or dc input voltage to a regulated dc output voltage. However in case of SMPS with input supply drawn from the ac mains, the input voltage is first rectified and filtered using a capacitor at the rectifier output. The unregulated dc voltage across the capacitor is then fed to a high frequency dc-to-dc converter. Most of the dc-to-dc converters used in SMPS circuits have an intermediate high frequency ac conversion stage to facilitate the use of a high frequency transformer for voltage scaling and isolation. In contrast, in linear power supplies with input voltage drawn from ac mains, the mains voltage is first stepped down (and isolated) to the desired magnitude using a mains frequency transformer, followed by rectification and filtering. The high frequency transformer used in a SMPS circuit is much smaller in size and weight compared to the low frequency transformer of the linear power supply circuit.

The „Switched Mode Power Supply" owes its name to the dc-to-dc switching converter for conversion from unregulated dc input voltage to regulated dc output voltage. The switch employed is turned „ON" and „OFF" (referred as switching) at a high frequency. During „ON" mode the switch is in saturation mode with negligible voltage drop across the collector and emitter terminals of the switch where as in „OFF" mode the switch is in cut-off mode with negligible current through the collector and emitter terminals. On the contrary the voltage regulating switch, in a linear regulator circuit, always remains in the active region.

**Block Diagram of DC-DC Converter SMPS:**




**Result:**

# SIMULATION USING SPICE

**AIM:**

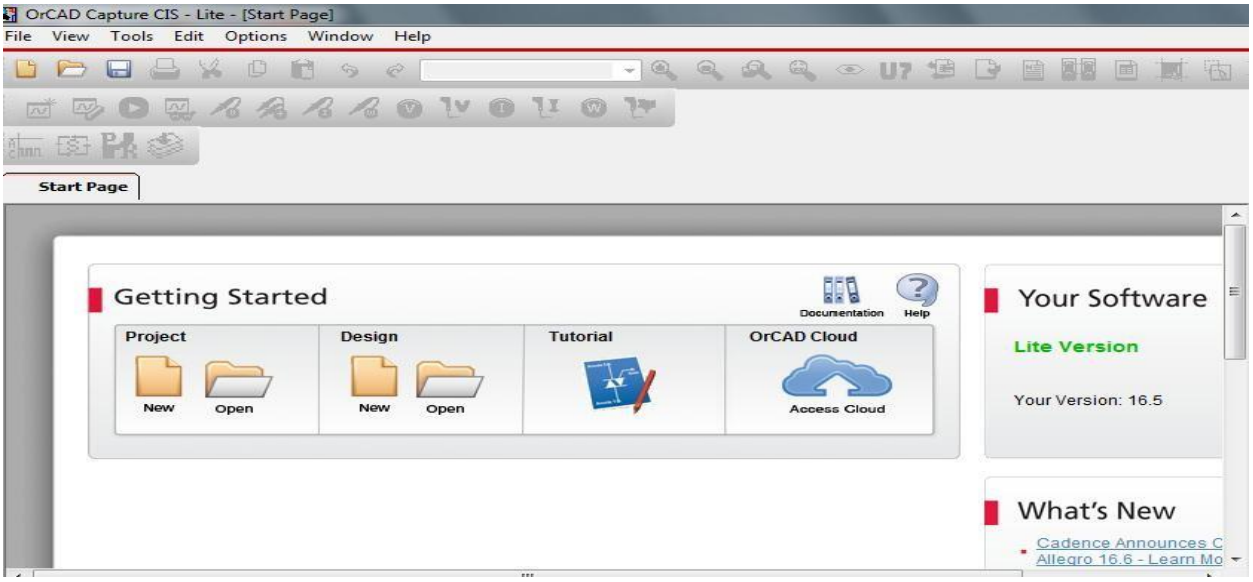
**To simulate the following circuits using PSPICE.**

**SOFTWARE REQUIRED:**

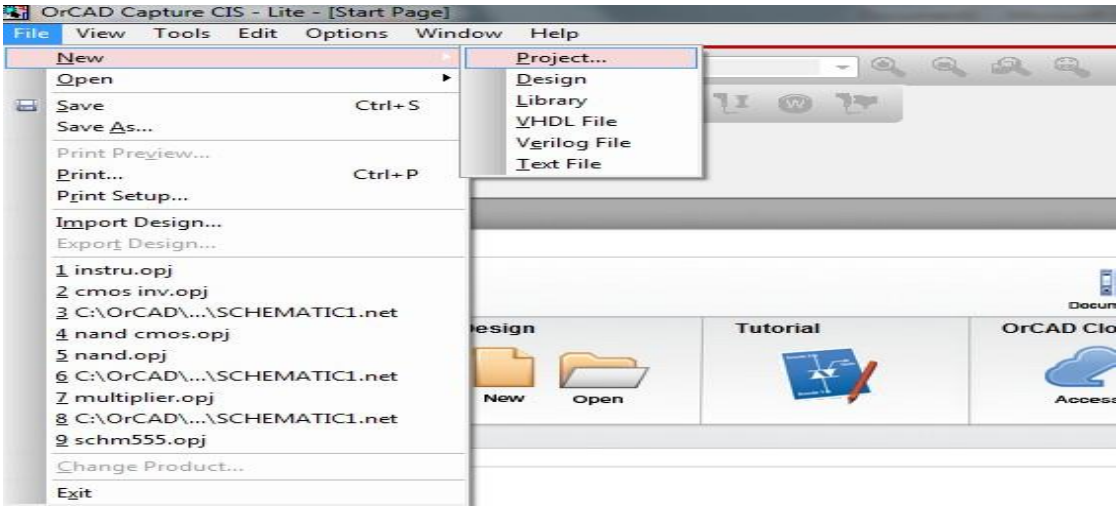
**ORCAD CAPTURE CIS LITE 16.5**

**PROCEDURE:**

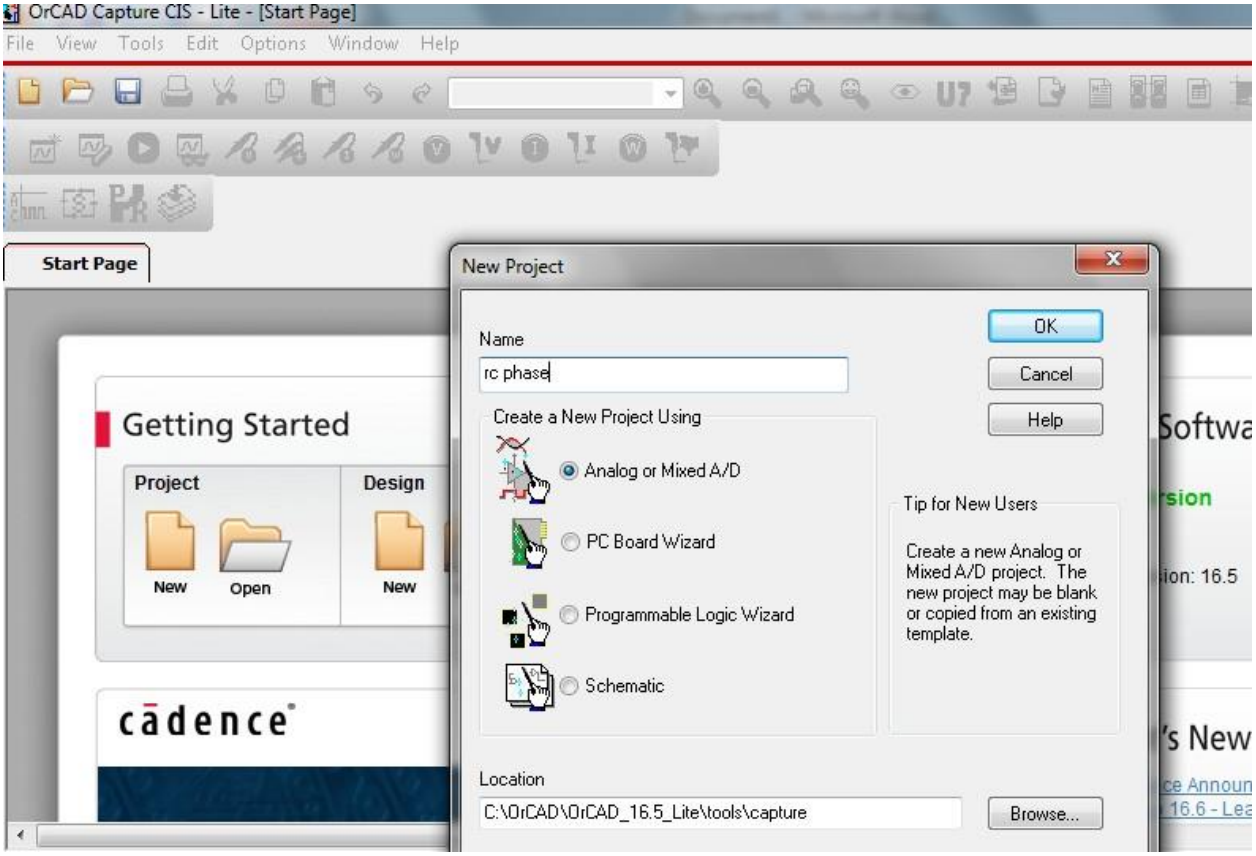
1. **Double Click the software icon the following window will appear.**



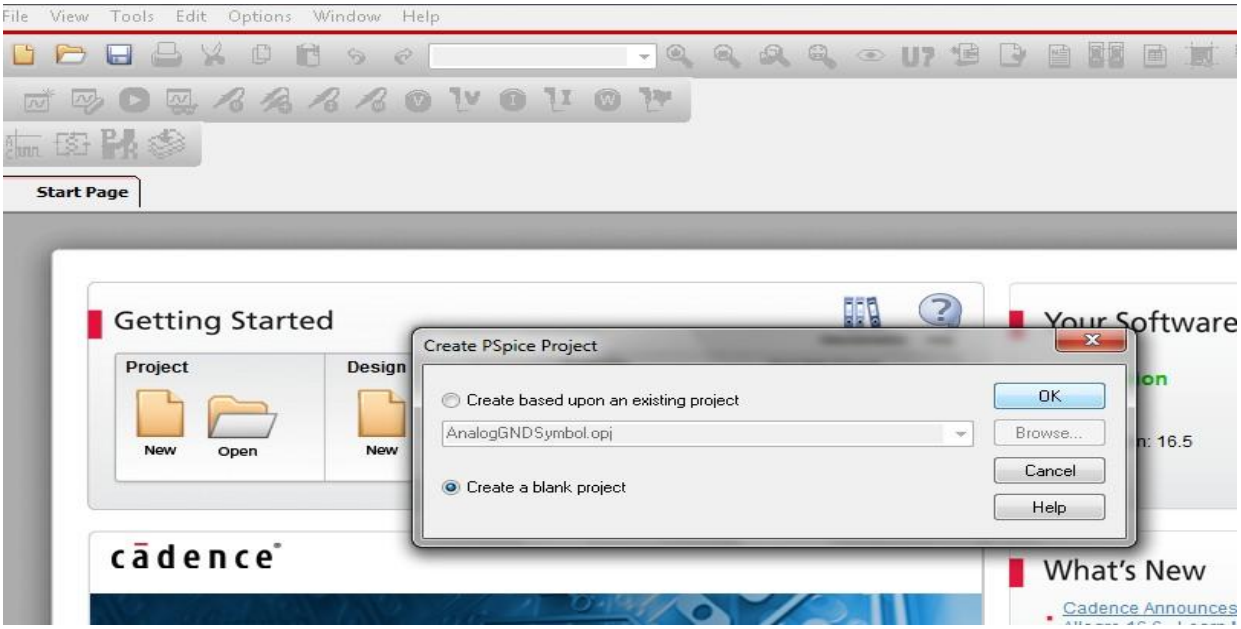

2. **Open your project**



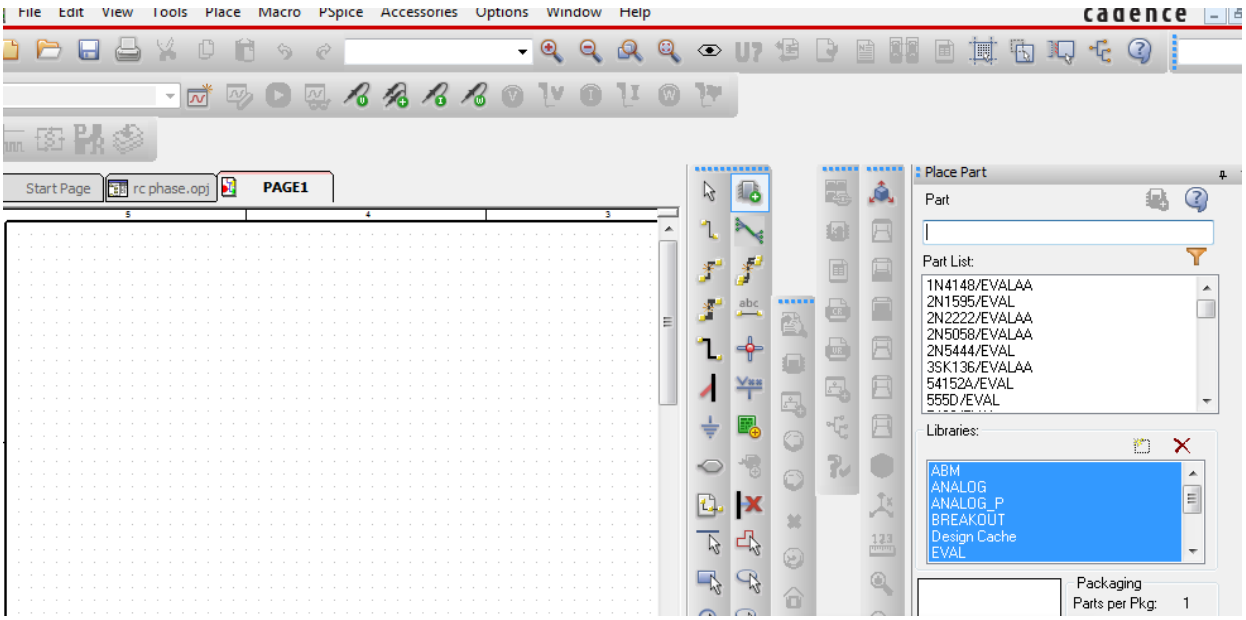
3. **Enter your project name.**



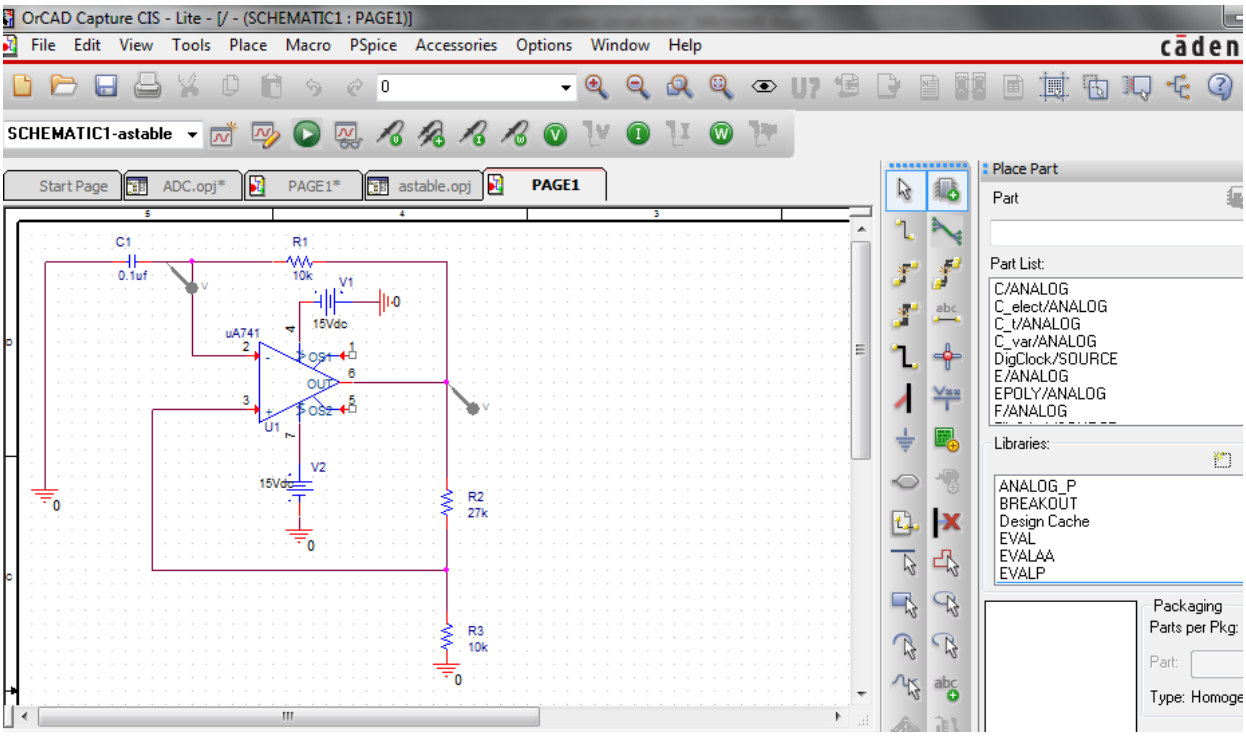

4. **Create blank project**



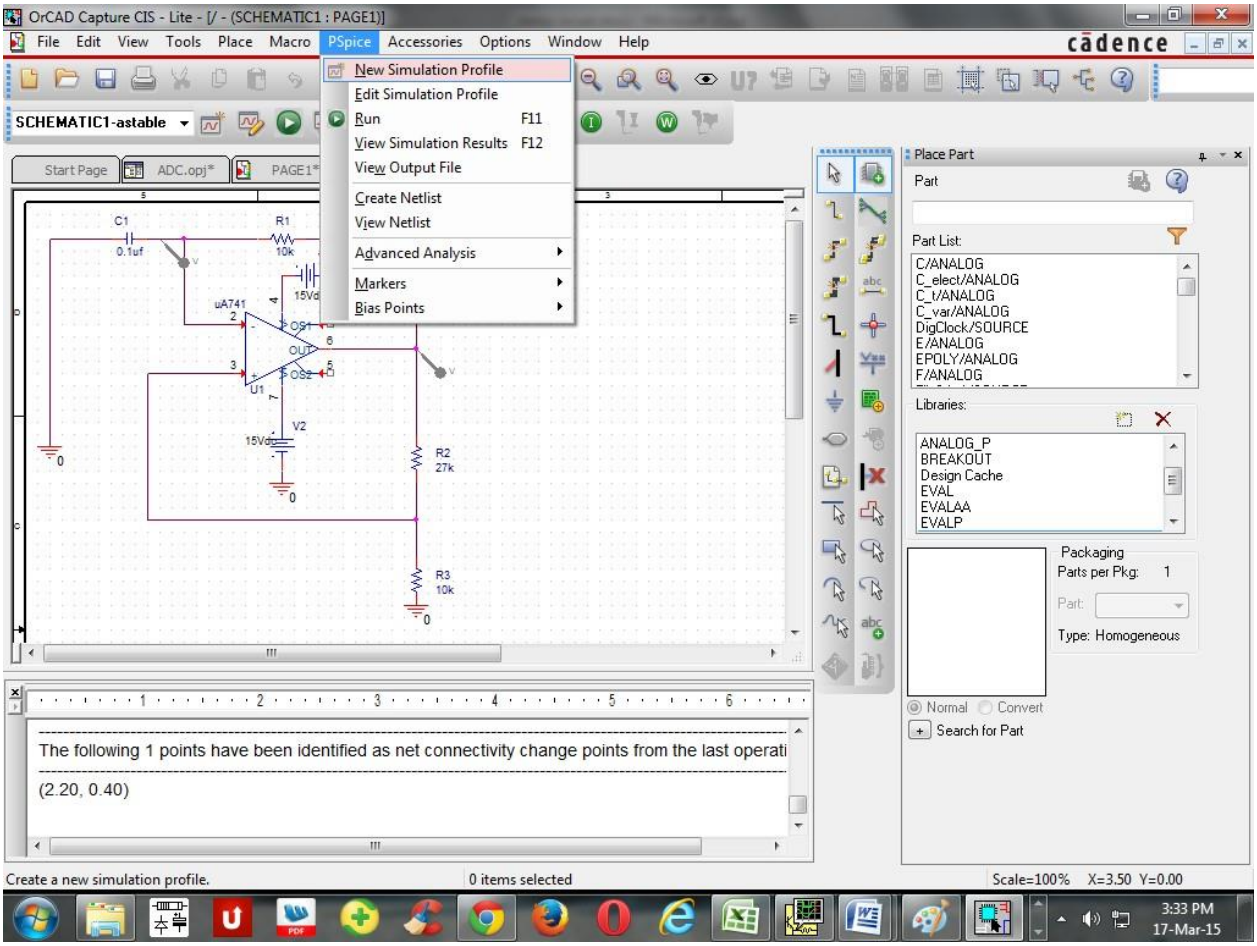
**5. Schematic window will be open, draw your project circuit by choosing the components from place part.**



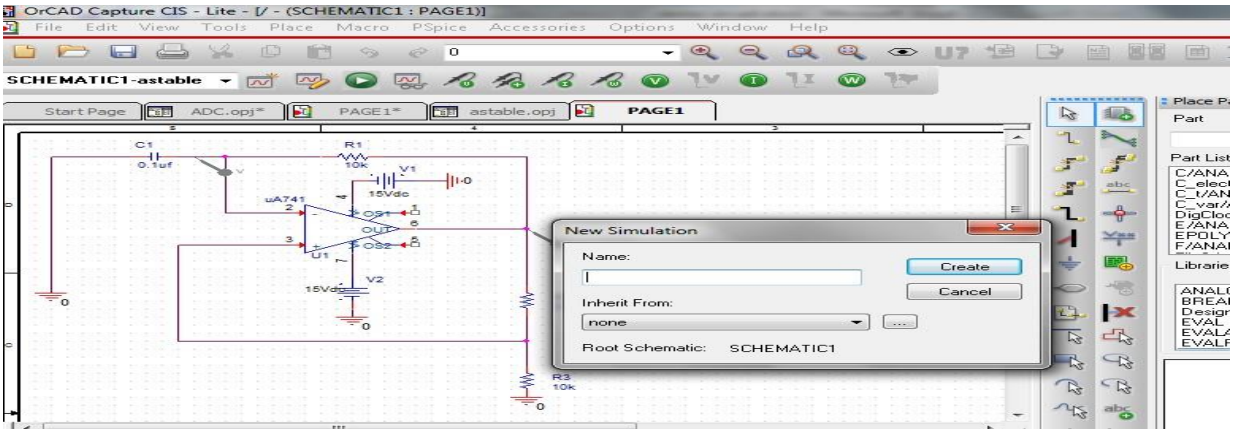

**6. Finish your circuit and save your project.**



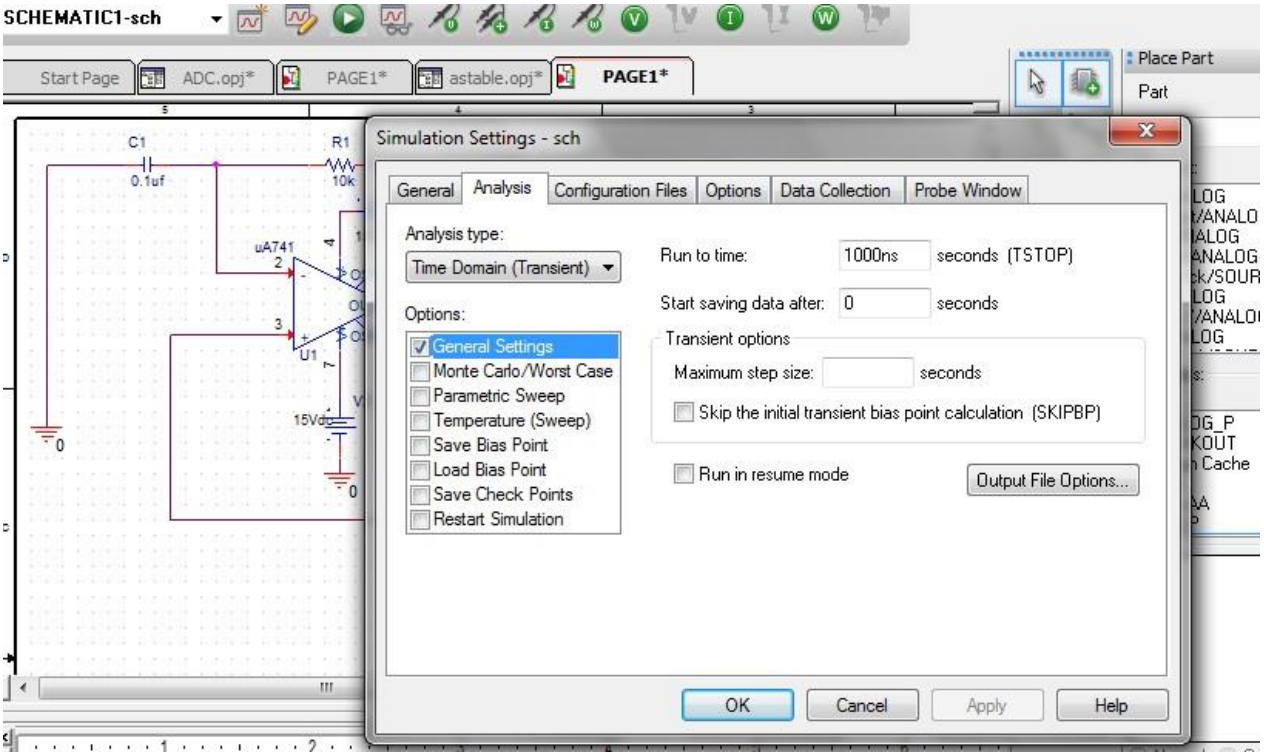
## 7. Create new simulation profile.



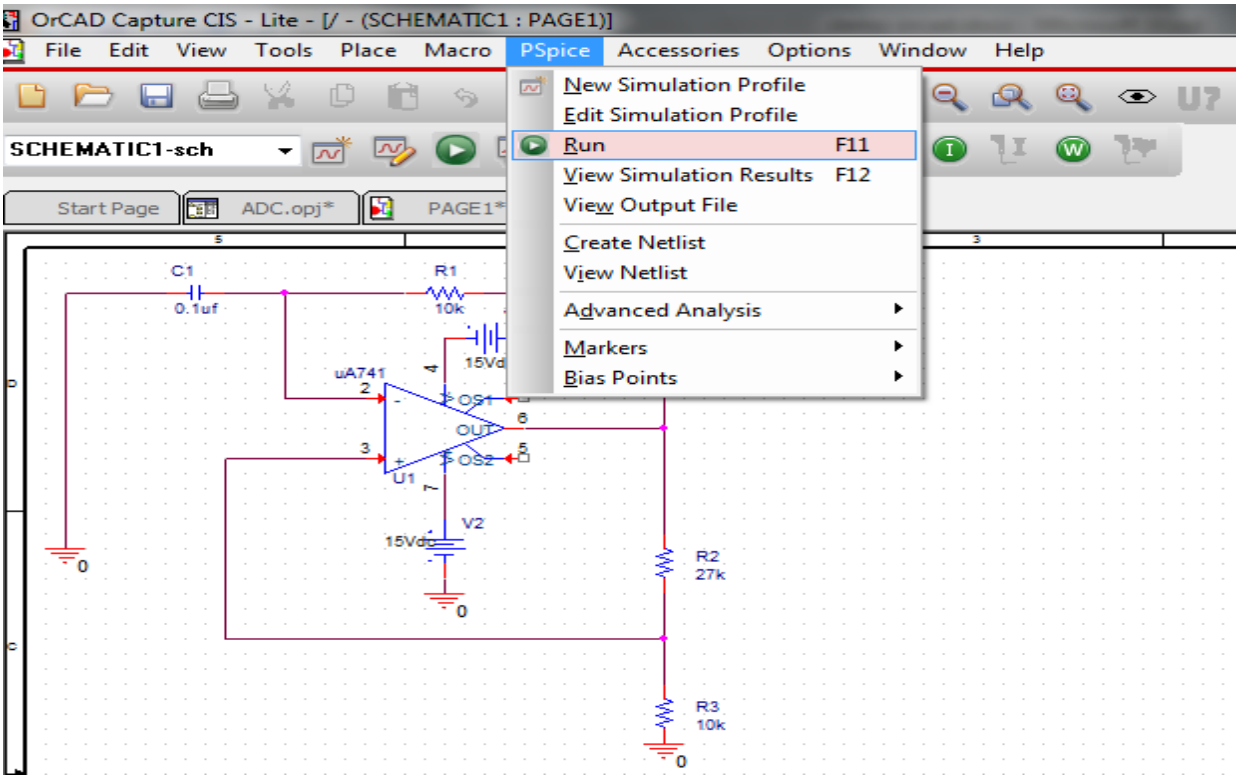

## 8. Give simulation file name.



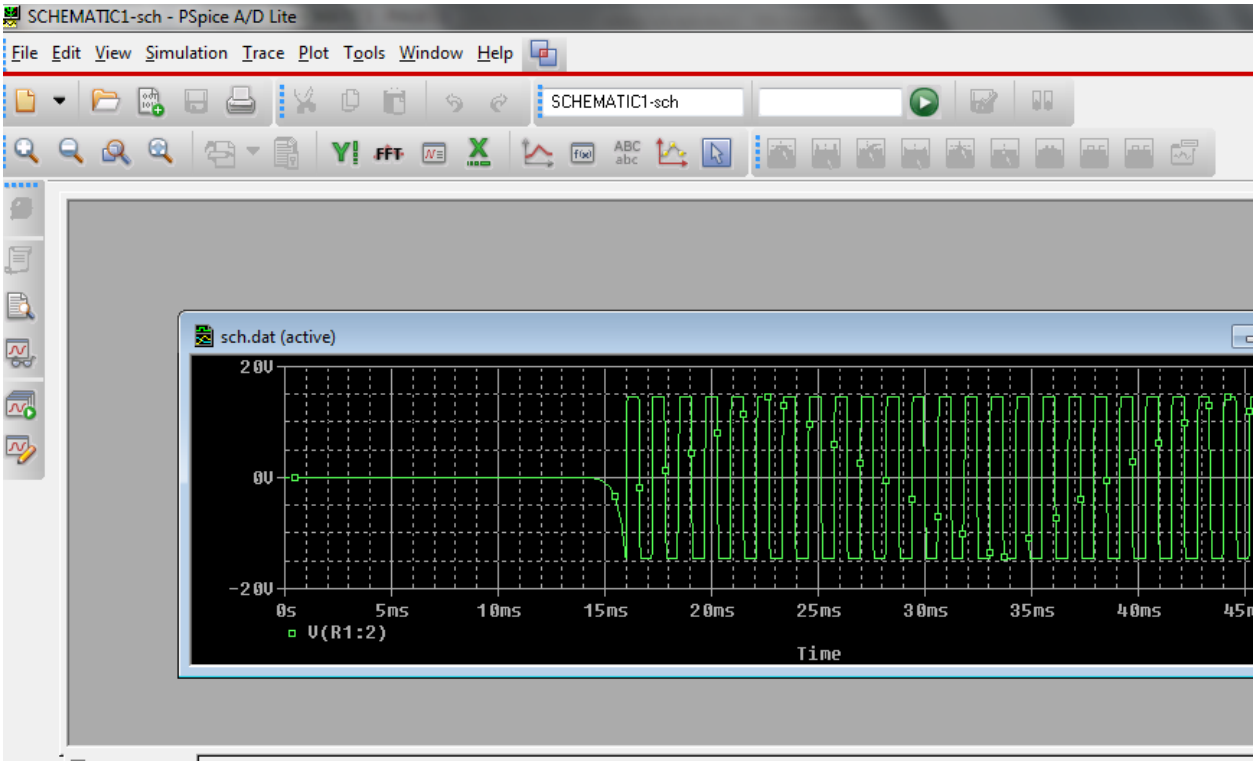
**9. Simulation settings window will be open, give the appropriate settings and click ok.**




**10. set the output probe and Click run**



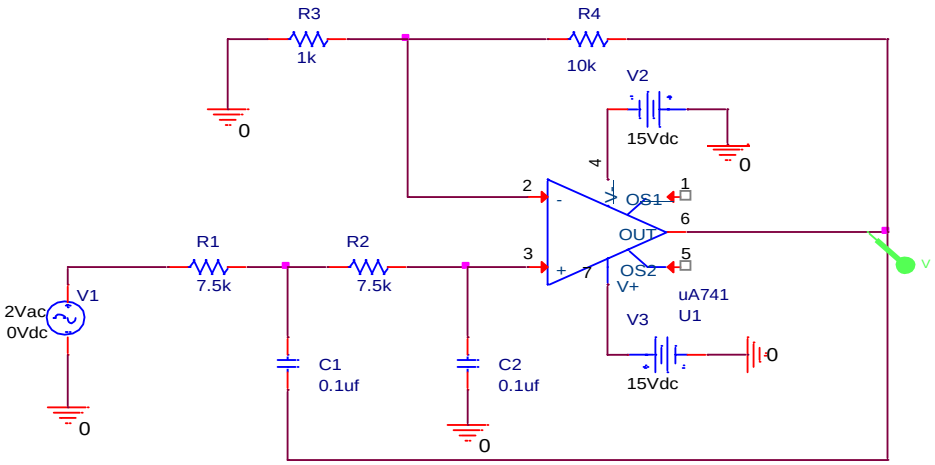
**11.Simulated output window will open. check your output.**




**12.Enter exit project.**

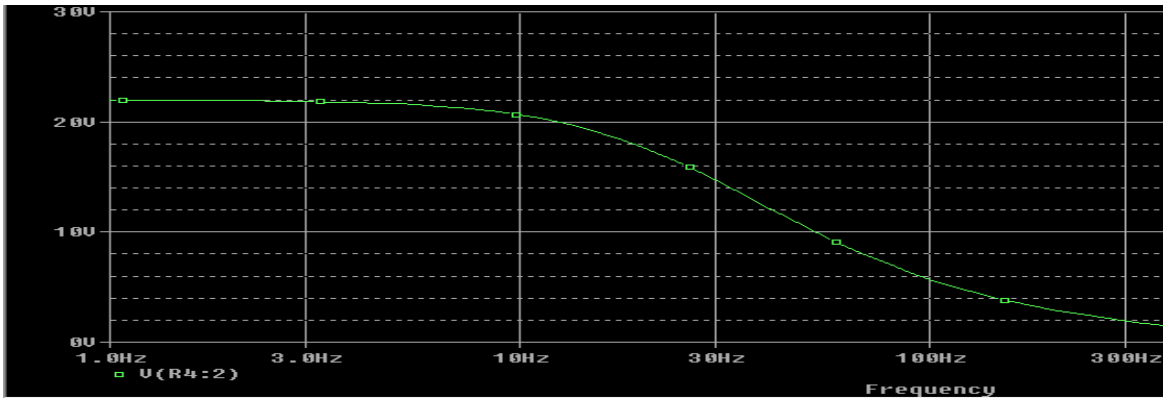
## 1. (A) LOW PASS FILTER

**CIRCUIT**

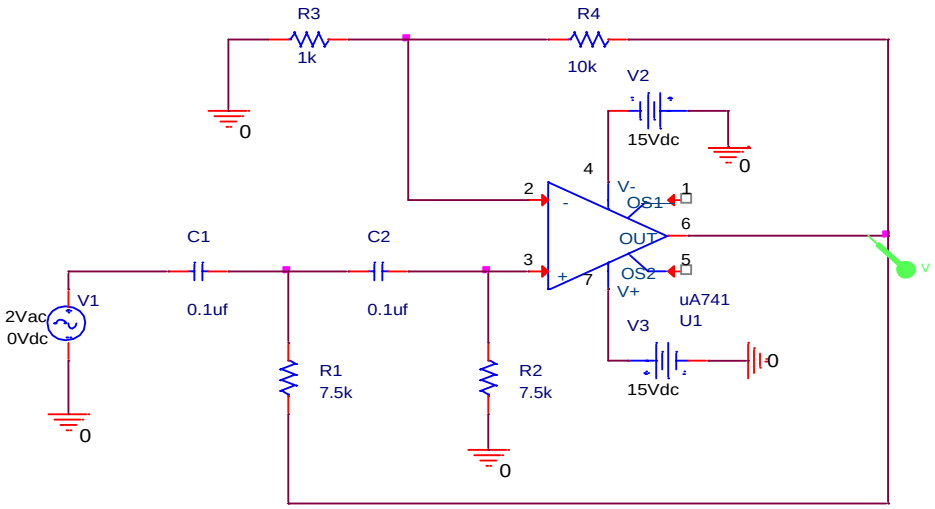


* source LOWPASS
V_V1 N00311 0 DC 0Vdc AC 2Vac
X_U1 N00322 N00444 N00386 N00374 N00400 uA741
R_R1 N00311 N00318 7.5k TC=0,0
R_R2 N00318 N00322 7.5k TC=0,0
R_R3 0 N00444 1k TC=0,0
R_R4 N00444 N00400 10k TC=0,0
C_C1 N00400 N00318 0.1uf TC=0,0
C_C2 0 N00322 0.1uf TC=0,0
V_V2 0 N00374 15Vdc
V_V3 N00386 0 15Vdc

AC/SWEEP NOISE- LOGARTHMIC 1HZ to 10 Khz / 20 decade



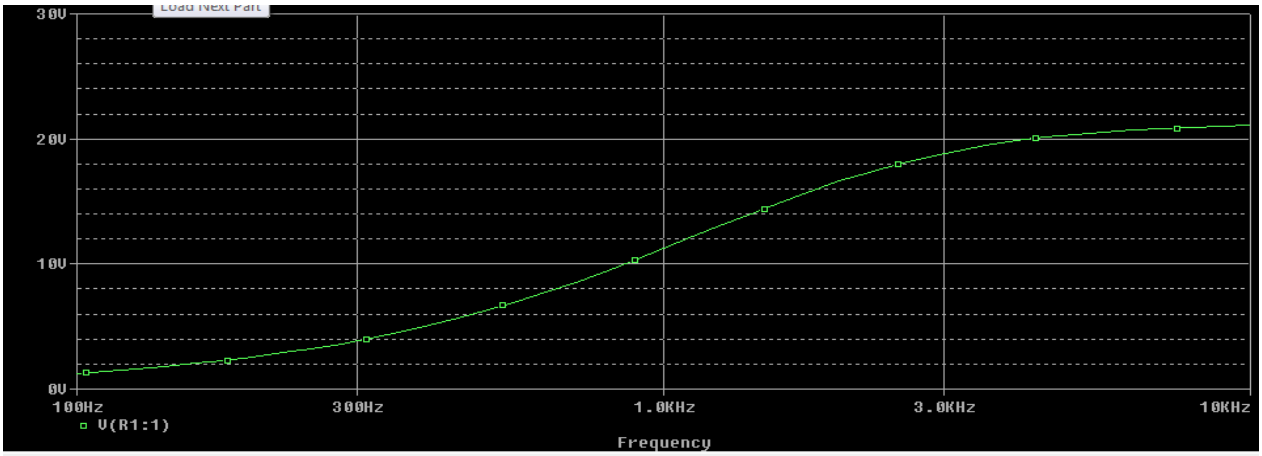

## 1 (B) HIGHPASS FILTER



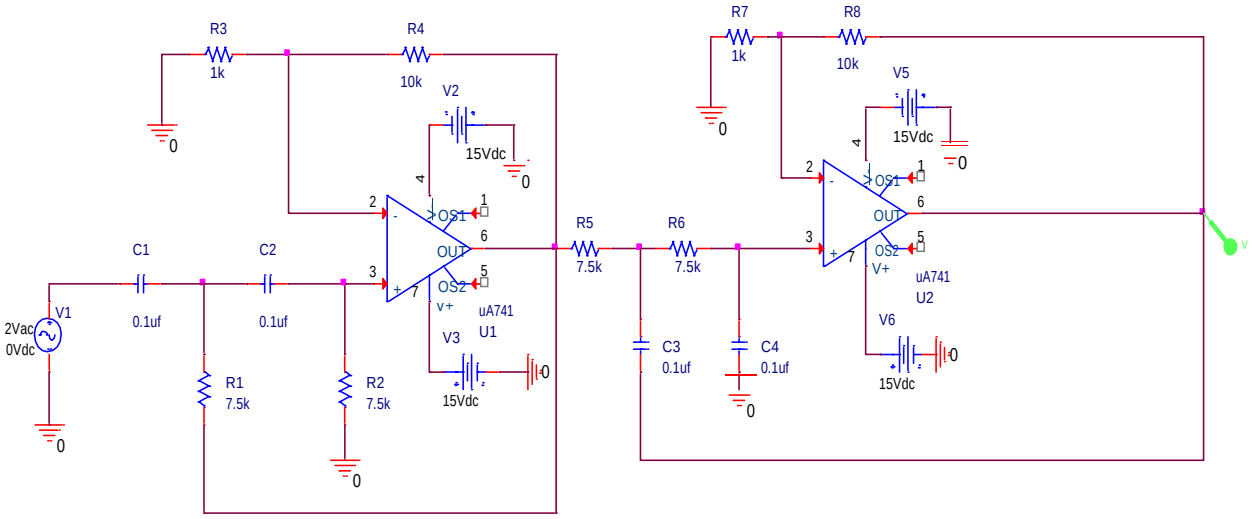
* source HIGH PASS

C_C1 N01234 N00999 0.1uf TC=0,0
R_R3 0 N01107 1k TC=0,0
R_R1 N01083 N01234 7.5k TC=0,0
X_U1 N01248 N01107 N01067 N01051 N01083 uA741
V_V1 N00999 0 DC 0Vdc AC 2Vac
V_V2 0 N01051 15Vdc
V_V3 N01067 0 15Vdc
R_R2 0 N01248 7.5k TC=0,0
R_R4 N01107 N01083 10k TC=0,0
C_C2 N01248 N01234 0.1uf TC=0,0

AC/SWEEP NOISE- LOGARTHMIC 1HZ to 10 Khz / 20 decade




## 1(C ) BAND PASS FILTER




HPF LPF

* source BAND PASS

R_R2 0 N01937 7.5k TC=0,0

V_V2 0 N01825 15Vdc

V_V1 N01815 0 DC 0Vdc AC 2Vac

C_C2 N01937 N01923 0.1uf TC=0,0

R_R1 N01957 N01923 7.5k TC=0,0

R_R3 0 N01873 1k TC=0,0

C_C1 N01923 N01815 0.1uf TC=0,0

V_V3 N01849 0 15Vdc

X_U1 N01937 N01873 N01849 N01825 N01957 uA741

R_R4 N01873 N01957 10k TC=0,0

V_V5 0 N03185 15Vdc

R_R6 N02635 N02639 7.5k TC=0,0

R_R8 N02733 N02709 10k TC=0,0

C_C4 0 N02639 0.1uf TC=0,0

C_C3 N02709 N02635 0.1uf TC=0,0

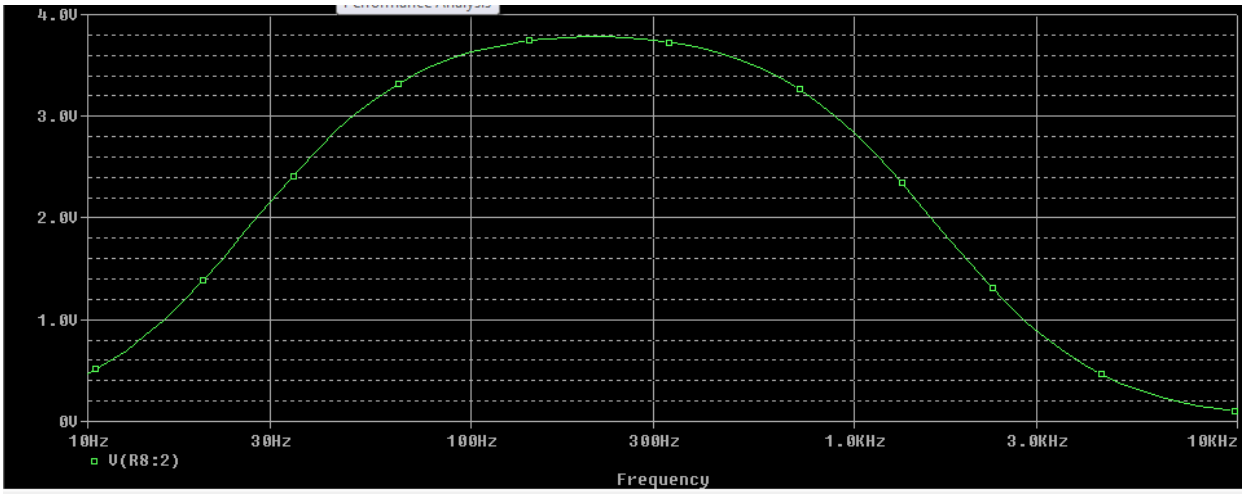
V_V6 N02693 0 15Vdc

R_R7 0 N02733 1k TC=0,0

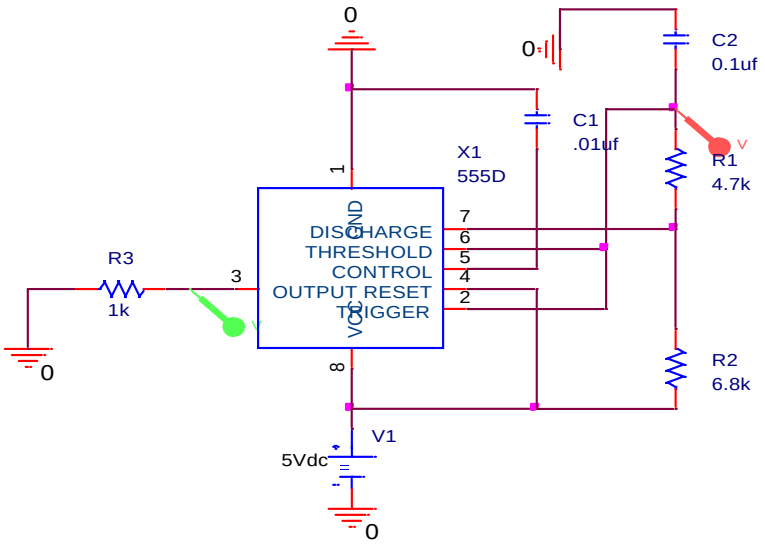
R_R5 N01957 N02635 7.5k TC=0,0

X_U2 N02639 N02733 N02693 N03185 N02709 uA741

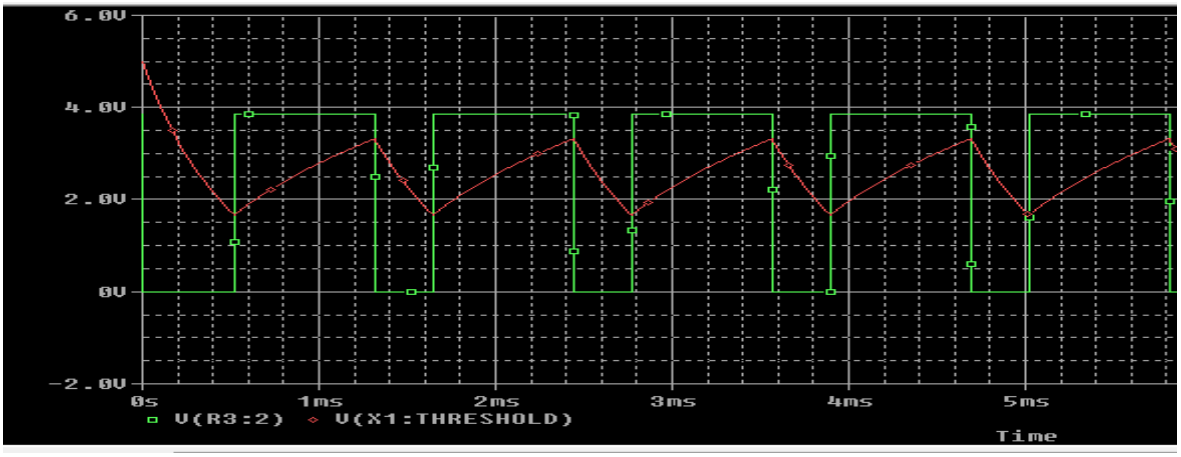
AC/SWEEP NOISE- LOGARTHMIC 1HZ to 10 Khz / 20 decade



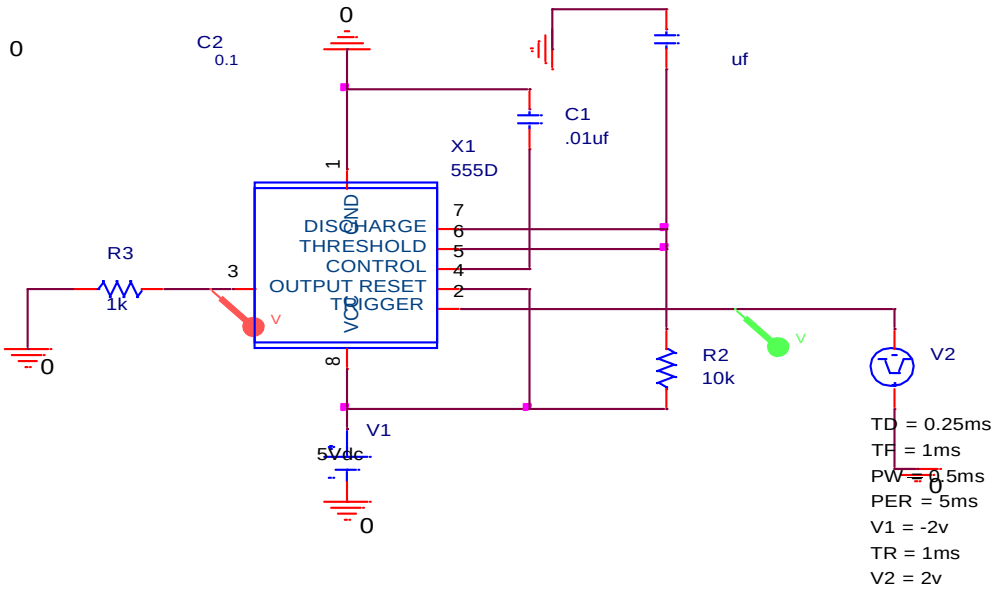

## 2 (A) ASTABLE MULTIVIBRATOR USING 555 TIMER



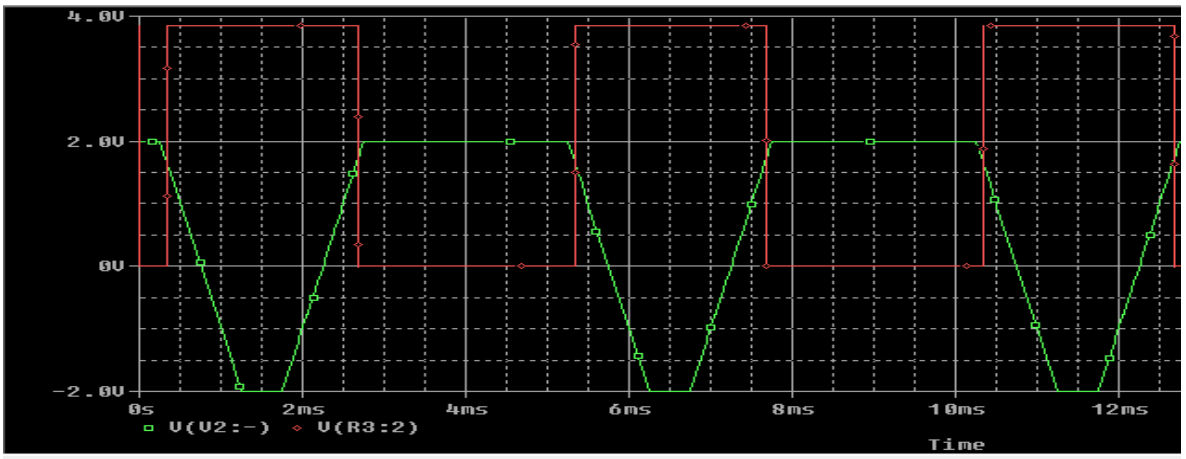

```
* source 555ASTABLE
X_X1       0 N00262 N00580 N00251 N00208 N00262 N00258 N00251 555D PARAMS:
+  MAXFREQ=3E6
V_V1       N00251 0 5Vdc
R_R1       N00258 N00262 4.7k TC=0,0
R_R2       N00251 N00258 6.8k TC=0,0
C_C1       N00208 0  .01uf  TC=0,0
C_C2       N00262 0  0.1uf  TC=0,0
R_R3       0 N00580  1k TC=0,0                    Run time 10 ms
```



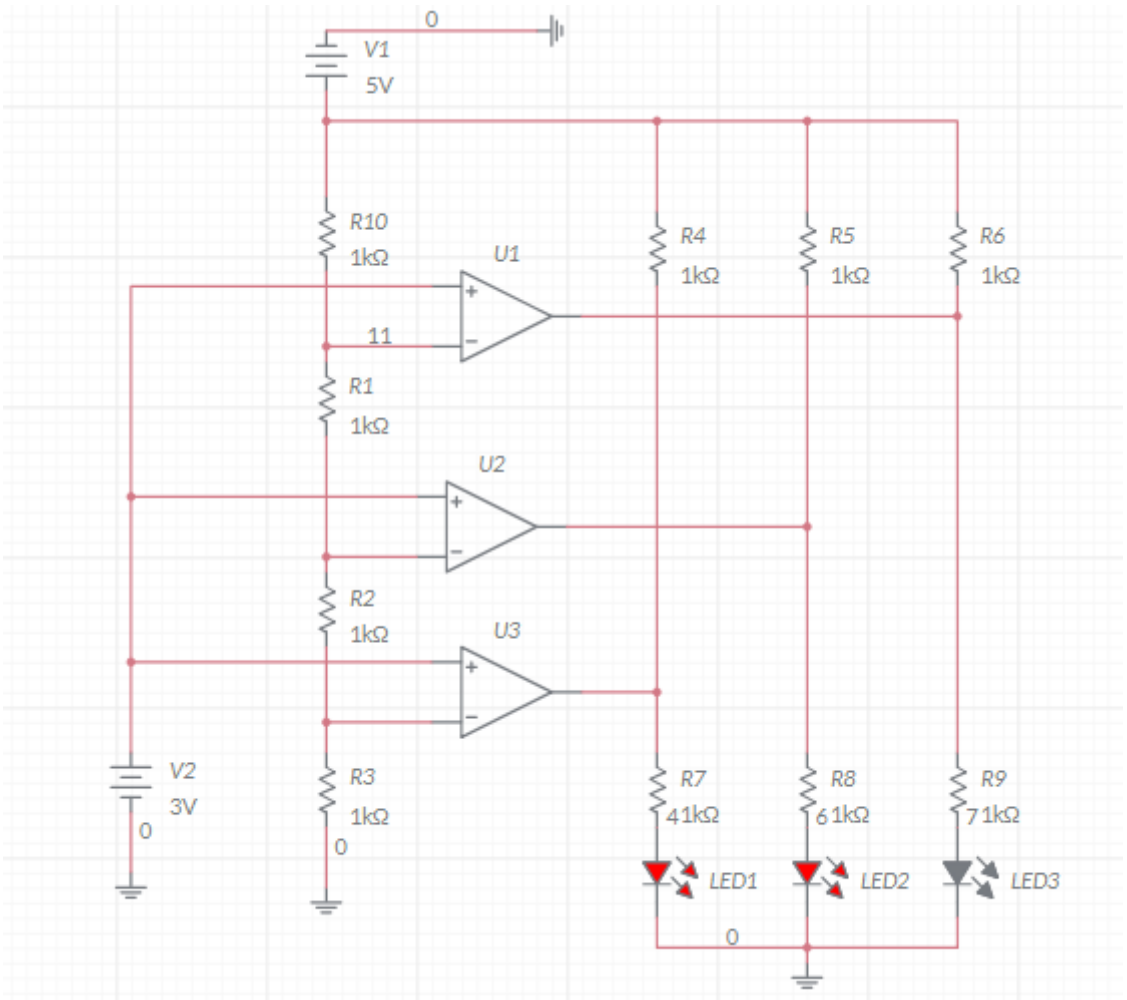

## 2(b) MONO STABLE MULTIVIBRATOR USING 555 TIMER



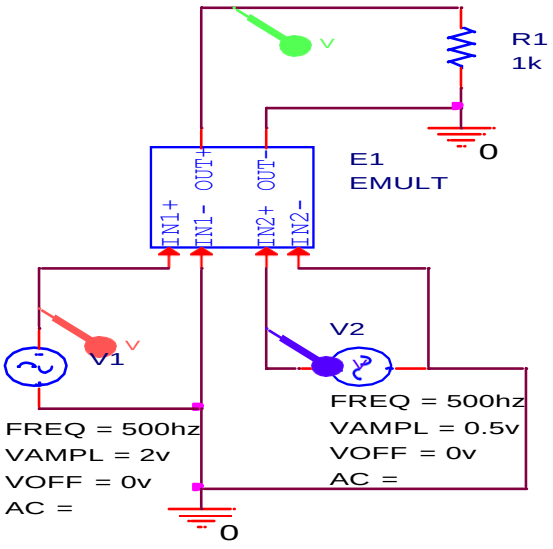

* source MONO555
R_R2 N01006 N01034 10k TC=0,0
C_C1 N00988 0 .01uf TC=0,0
R_R3 0 N01124 1k TC=0,0
X_X1 0 N01321 N01124 N01006 N00988 N01034 N01034 N01006 555D PARAMS:
+ MAXFREQ=3E6
C_C2 N01034 0 0.1uf TC=0,0
V_V1 N01006 0 5Vdc
V_V2 0 N01321
+PULSE -2v 2v 0.25ms 1ms 1ms 0.5ms 5ms Run time 20ms




## 3. A/D CONVERTER



# 4. ANLOG MULTIPLIER




```
* source MULTIPLIER
E_E1        N00944 0 VALUE {V(N00158,0)*V(N00182,0)}
V_V1        0 N00158
+SIN 0v 2v 500hz 0 0 0
V_V2        0 N00182
+SIN 0v 0.5v 500hz 0 0 0
R_R1        0 N00944  1k TC=0,0
```