Project Report:

Design and Implementation of a 4-bit ALU

1. Introduction

An **Arithmetic Logic Unit (ALU)** is a key part of a CPU that performs arithmetic and logical operations. This project involves designing and simulating a **4-bit ALU** in Logisim, supporting:

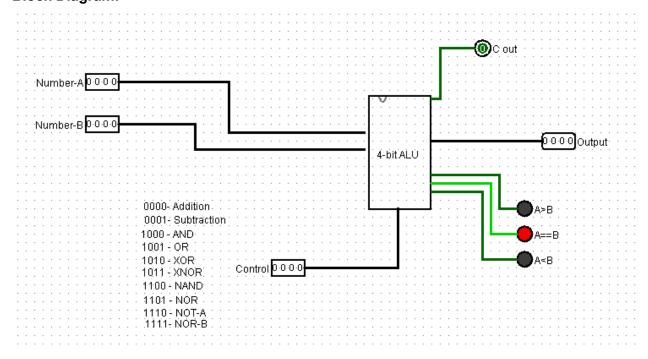
- > Arithmetic Operations: Addition, Subtraction
- Logical Operations: AND, OR, XOR, NOT
- > Comparison Operations: Equality, Greater Than, Less Than

2. ALU Design Overview

Key Components:

Input Registers (A, B) – Two 4-bit inputs
Control Unit – Decodes operation selection
Arithmetic Unit – Handles addition/subtraction
Logic Unit – Performs AND/OR/XOR/NOT
Comparison Unit – Checks A vs B
Multiplexer (MUX) – Selects output based on control signal

Block Diagram:

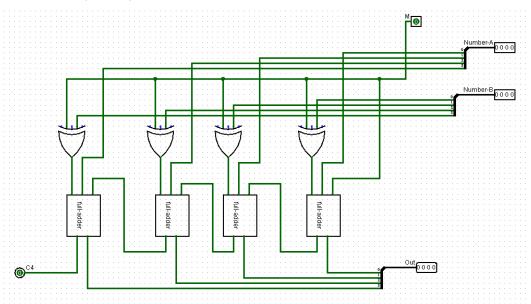


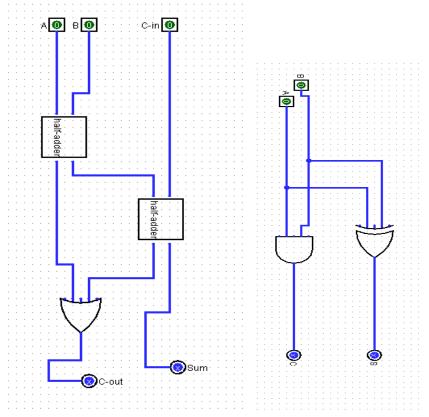
3. Functional Description

3.1 Arithmetic Operations

Addition (A + B): 4-bit ripple-carry adder

Subtraction (A - B): 2's complement method





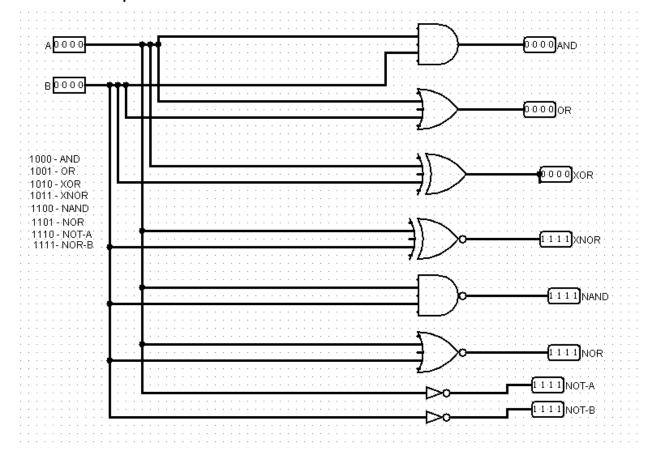
Full- Adder

Half-Adder

3.2 Logical Operations

AND, OR, XOR: Bitwise operations

NOT: Inverts input A

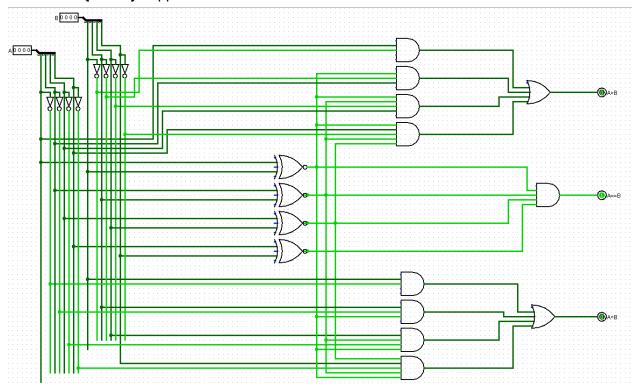


3.3 Comparison Operations

Equality (A == B): XOR gates check bits

Greater Than (A \rightarrow B): Checks subtraction sign

Less Than (A < B): Opposite of Greater Than



4. Logisim Implementation

4.1 Control Signal Encoding

0000- Addition 0001- Subtraction 1000 - AND 1001 - OR 1010 - XOR 1011 - XNOR 1100 - NAND 1101 - NOR 1110 - NOR-B

4.2 Circuit Components

Basic Logic Gates (AND, OR, XOR, NOT) 4-bit Adder/Subtractor Multiplexers (MUX) for operation selection Output LEDs/Displays

5. Simulation Results

Α	В	Operation	Result	Pass?
0101	0011	ADD (0000)	1000 (8)	✓
0110	0010	SUB (0001)	0100 (4)	✓
1100	1010	AND (0010)	1000 (8)	✓
1100	1010	OR (0011)	1110 (14)	✓
1100	1010	XOR (0100)	0110 (6)	✓
1100		NOT (0101)	0011 (3)	✓
0101	0101	EQ (0110)	1 (True)	✓
0111	0011	GT (0111)	1 (True)	✓
0101	1011	LS (0000)	1 (True)	✓
_	1100	NOT (1001)	0011 (3)	✓
1100	1010	XOR (0100)	0110 (6)	✓

6. Conclusion

- Successfully designed a **4-bit ALU** in Logisim.
- Verified all operations via simulation.