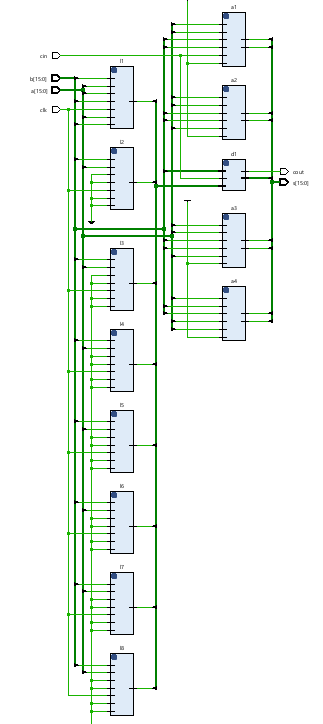
**LOW ERROR EFFICIENT APPROXIMATE**

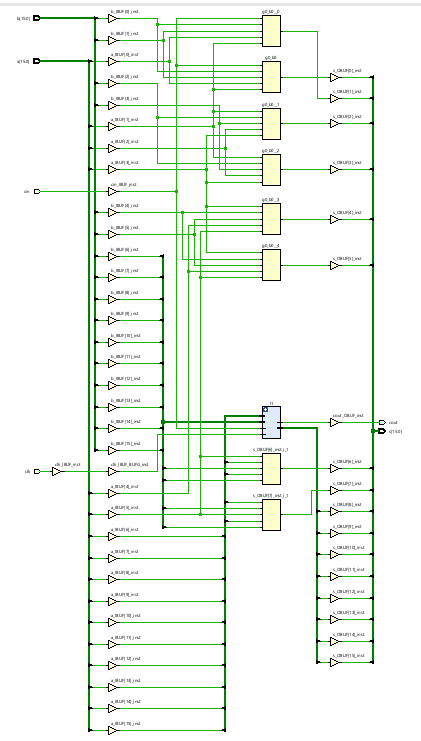
**ADDERS FOR FPGAs**

**LEADx:**

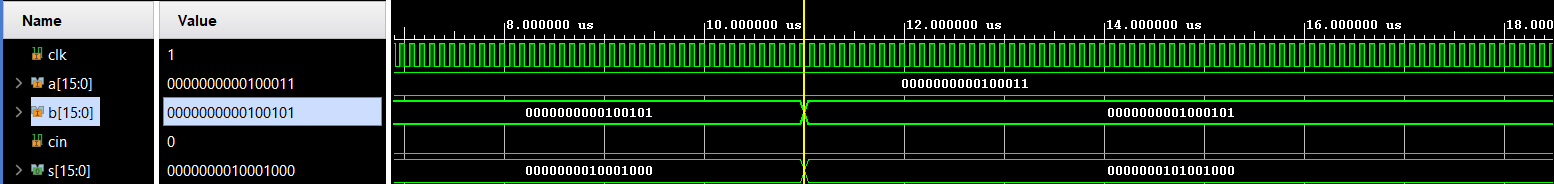
**RTL schematic:**

****

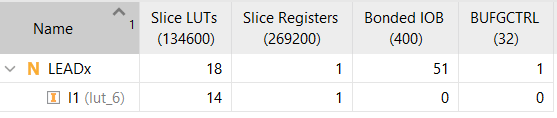
**Technology Schematic:**

****

**Simulation results:**

****

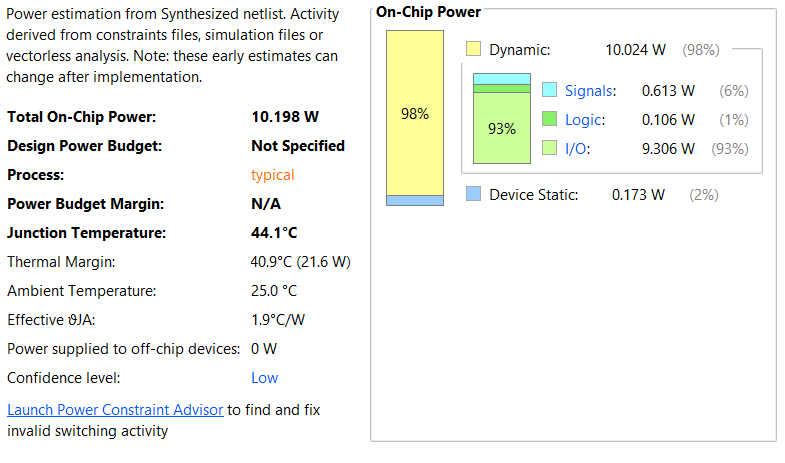
**Area:**

****

**Delay:**

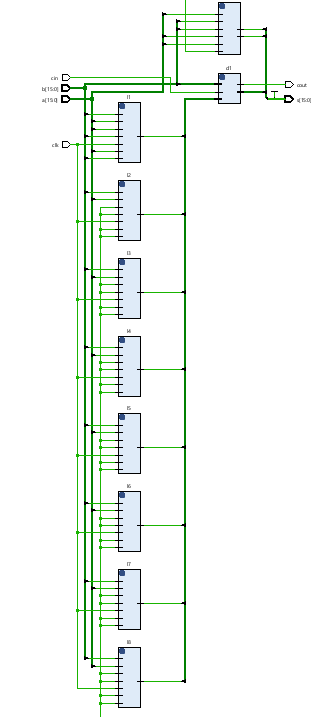
****

**Power:**

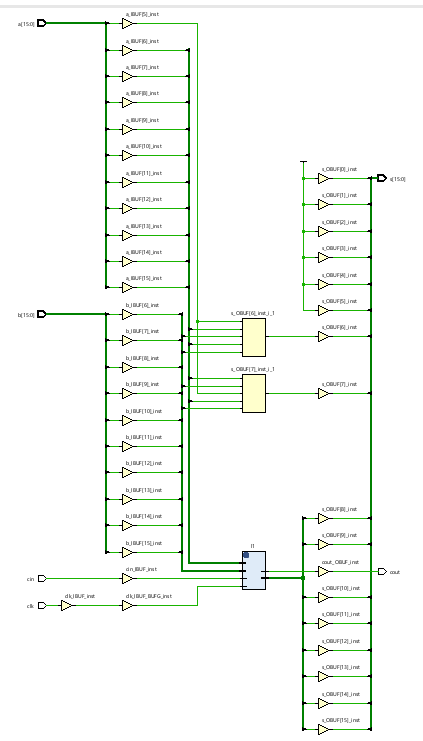
****

**APEx:**

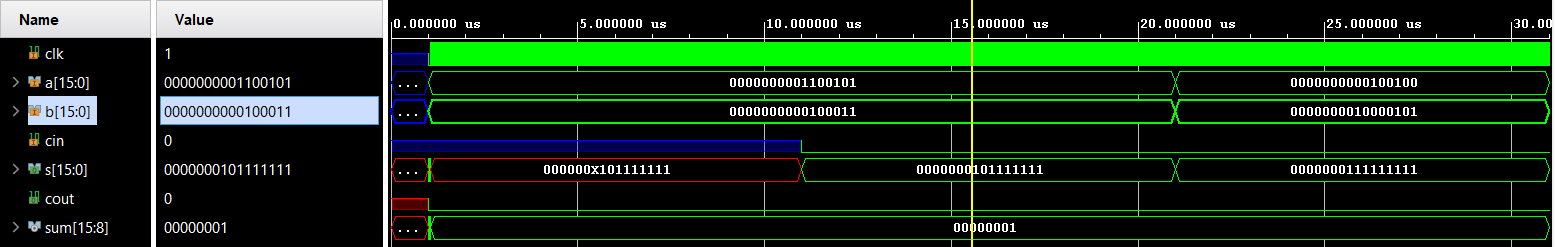
**RTL schematic:**

****

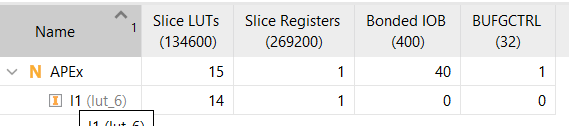
**Technology Schematic:**

****

**Simulation results:**

****

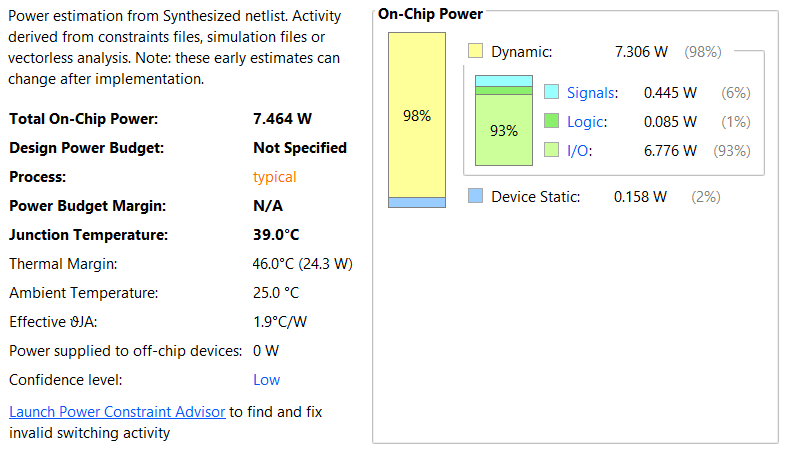
**Area:**

****

**Delay:**

****

**POWER:**

****

**Evaluation table:**

|  |  |  |  |
| --- | --- | --- | --- |
|  | **Area (LUT’s)** | **POWER** | **Delay (ns)** |
| **LEADx** | 18 | 10.198 | 6.511 |
| **APEx** | 15 | 7.464 | 6.511 |