EAST WEST UNIVERSITY

Project – 1

Project Title: 2's complementor

Course: CSE345

Title: Digital Logic Design

Section: 02

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Submitted To:

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- **Problem Statement:** Objective of project 1 is to create a 2's Complementor which will take 4-bit binary number as input and in output section it will generate 4 bit 2's complement of given input.

- **Design details:** Truth table has been constructed according to the 2's complement of each binary number. After that Expressions of each output has been constructed using K-map method. Using these expressions of output P, Q, R, S diagram of the circuit has been constructed.

  - ✓ **Truth Table:**

Value	**Binary**				**2's Complement**			
	A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	1	1	1
2	0	0	1	0	1	1	1	0
3	0	0	1	1	1	1	0	1
4	0	1	0	0	1	1	0	0
5	0	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	0
7	0	1	1	1	1	0	0	1
8	1	0	0	0	1	0	0	0
9	1	0	0	1	0	1	1	1
10	1	0	1	0	0	1	1	0
11	1	0	1	1	0	1	0	1
12	1	1	0	0	0	1	0	0
13	1	1	0	1	0	0	1	1
14	1	1	1	0	0	0	1	0
15	1	1	1	1	0	0	0	1

Table 1: Truth Table for 2's Complementor.

✓ **K-map for output P:**

	C D			
A B	0 0	0 1	1 1	1 0
0 0	0	1	1	1
0 1	1	1	1	1
1 1	0	0	0	0
1 0	1	0	0	0

Table 2: Representation of truth table on k-map for output P.

Expression of P = A'D+A'C+A'B+AB'C'D'

= A'(B+C+D) + A(B+C+D)'

= A $\oplus$ (B+C+D)

✓ **K-map for output Q:**

	C D			
A B	0 0	0 1	1 1	1 0
0 0	0	1	1	1
0 1	1	0	0	0
1 1	1	0	0	0
1 0	0	1	1	1

Table 3: Representation of truth table on k-map for output Q.

Expression of Q = BC'D' + B'D + B'C

= B(C+D)'+B'(C+D)

= B $\oplus$ (C+D)

✓ **K-map for output R:**

	C D			
A B	0 0	0 1	1 1	1 0
0 0	0	1	0	1
0 1	0	1	0	1
1 1	0	1	0	1
1 0	0	1	0	1

Table 4: Representation of truth table on k-map for output R.

Expression of R = C'D + CD'

= C ⊕ D

✓ **K-map for output S:**

	C D			
A B	0 0	0 1	1 1	1 0
0 0	0	1	1	0
0 1	0	1	1	0
1 1	0	1	1	0
1 0	0	1	1	0

Table 5: Representation of truth table on k-map for output S.

Expression of S = D

❖ **Circuit Diagram:**

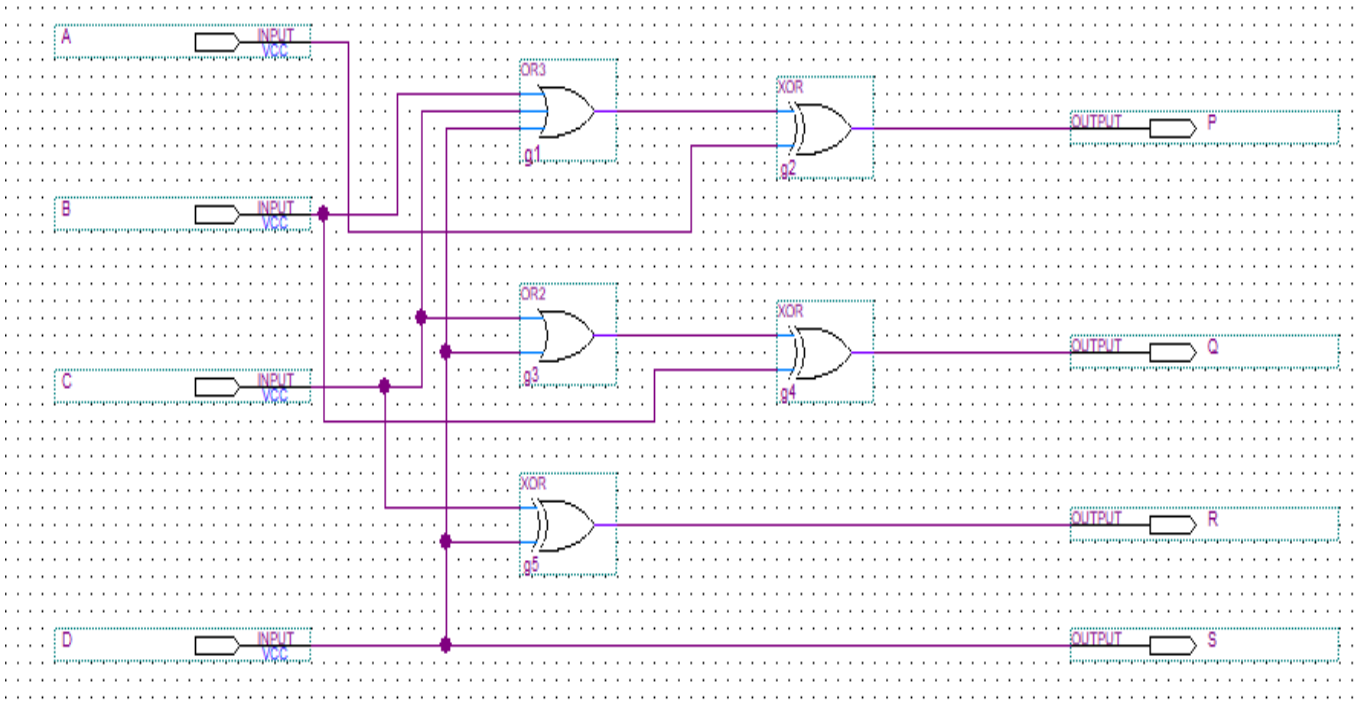

Figure 1: Schematic circuit.

❖ **Behavioral Verilog Code:**

```
1  module code(input A,B,C,D,output P,Q,R,S);
2  assign P=A ^ (B | C | D);
3  assign Q=B ^ (C | D);
4  assign R=C ^ D;
5  assign S=D;
6  endmodule
```

Figure 2: Behavioral Verilog code using Continuous assign statement.

```
1  module code(input A,B,C,D, output reg P,Q,R,S);
2  always@(A,B,C,D)begin
3    P=0;
4    Q=0;
5    R=0;
6    S=D;
7    if(A ^ (B | C | D)) P = 1;
8    if(B ^ ( C | D )) Q = 1;
9    if(C^D) R = 1;
10   end
11   endmodule
12
```

Figure 3: Behavioral Verilog code using procedural model.

❖ Simulation Result:

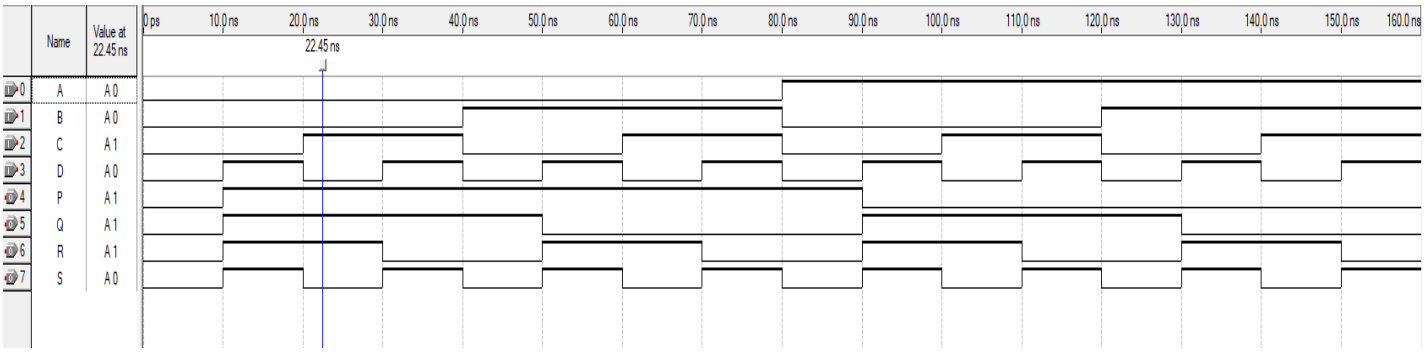

Figure 4: Simulation output.