Bangabandhu Sheikh Mujibur Rahman Science & Technology University
Department of Computer Science and Engineering
3rd Year 1st Semester B.Sc. (Engg.) Final Examination-2019

Course No.: CSE307 **Course Title: Compiler Design**
Full Marks: 60 **Time: 03 hours**
N.B.
i) Answer any **SIX** questions, out of the following **Eight** questions.
ii) All questions are of equal values.

1. a) Explain the phases of a compiler for the following assignment statement: (position:= initial + rate * 60) 4
   b) Consider the CFG with the following production rules: 4

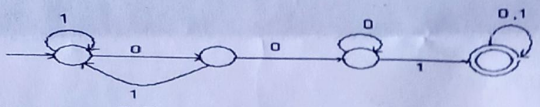
S → aB/ bA
A → bAA / aS/ a
B → aBB / bS/ b

Give the right most derivation and draw derivation tree for the string ***abbaab***.

   c) What is the purpose of semantic analysis in a compiler? 2
2. a) Construct a DFA equivalence to the regular expression (0+1)*(00+11)(0+1)*? 2
   b) Convert the following DFA to Regular Expression. 4

	0	1
p	p	q
q	q	r
r	p	r

   c) Figure shows deterministic finite state automaton M. Let the set of seven bit binary strings whose 1st, 4th and the last bits are 1 is denoted by S. How many strings in S is accepted by M? 4



3. a) Explain ambiguous grammar G: E ⟶ E + E | E * E | (E) | - E | id for the sentence id + id * id. 3
   b) Construct parse tree for the input string w = cad using top down parser. 4
   S ⟶ cAd
   A ⟶ ab | a
   c) What is the minimum number of states in any DFA accepting the regular language L = (111+11111)*? Explain. 3

4. a) Describe the languages denoted by the following regular expressions: 5
   i. a(a|b)*a ii. ((ε|a)b*)*
   b) Construct a syntax directed definition for constructing a syntax tree for assignment statements. 5
   S ⟶ id : = E
   E ⟶ E1 + E2
   E ⟶ E1 * E2
   E ⟶ E1
   E ⟶ (E1)
   E ⟶ id

5. a) Consider the context-free grammar: 6
   S -> S S + | S S * | a
   and the string aa + a*.
   i. Give the rightmost derivation for the string.
   ii. Give a parse tree for the string.
   iii. Is the grammar ambiguous or not? Justify your answer.
   b) Show that the following grammar 4
   S ⟶ Aa | bAc | dc | bda
   A ⟶ a
   is LR (1) but not SLR (1)
6. a) Check whether the following two DFA's are equal or not. 4

	0	1
→ q1	q1	q2
q2	q3	q1
* q3	q2	q3

	0	1
→ q4	q4	q5
q5	q6	q4
q6	q7	q6
* q7	q6	q4

b) Construct parsing table for the grammar and find moves made by predictive parser on input id + id * id and find FIRST and FOLLOW. 6

E ⟶ E + T
E ⟶ T
T ⟶ T * F
T ⟶ F
F ⟶ (E)/id

7. a) Given the following code segment: 4

```
for i:=1 to 20 do
  if i>a+5
    then x:=x+2
  else y:=y-1;
```

Translate the code segment into abstract syntax trees, quadruples, and postfix code.

b) Consider the following grammar: 4

$$S \rightarrow A$$

$$A \rightarrow A+A \mid B{+}{+}$$

$$B \rightarrow y$$

i) Draw the parse tree for the input "$y + + + y + +$"
ii) Show a leftmost derivation of "y + + + y + +"

c) Find the instruction cost for the following instructions. 2

(i) MOV R0, R1

ADD c, R0

MOV R0, a

(ii) MOV 4(R0), M

MOV b, a(R)

8. a) Draw the DAG for the statement **a=(a*b+c)-(a*b+c).** 3

b) For the following three address code identify the basic blocks and draw the flow graph. 5

(1) PROD = 0
(2) I = 1
(3) T2 = addr(A) – 4
(4) T4 = addr(B) – 4
(5) T1 = 4 x I
(6) T3 = T2[T1]
(7) T5 = T4[T1]
(8) T6 = T3 x T5
(9) PROD = PROD + T6
(10) I = I + 1
(11) IF I <=20 GOTO (5)

c) Optimized the following code: 2

```
while(i<100)
{
 a = Sin(x)/Cos(x) + i;
 i++;
}
```

Bangabandhu Sheikh Mujibur Rahman Science and Technology University

Department of Computer Science and Engineering

3rd Year 1st Semester B.Sc. Engineering Final Examination 2019

Course Title: Computer Architecture and Organization **Course Code: CSE 305**

Total Marks: 60 **Time: 3 (Three) Hours**

N.B.

i. Answer **SIX** questions taking any **EIGHT**.

ii. All questions are of equal values.

1. a) Show the binary representation of -0.125_{ten} in single and double precision. 2

   b) Draw the block diagram of a four-way set associative cache. 3

   c) Write down the control steps including control signals in a multi (three) bus organization for the following instruction- ADD R_4, R_5, R6. 3

   d) Write short note on (i) Control word (ii) μinstructions (ii) μPC. 2

2. a) What is instruction pipeline? How does it improve the performance of computer system? Explain with diagram. 3

   b) Explain user visible and status register with example. 3

   c) What is memory hierarchy? Explain. 2

   d) What is meant by branch penalty? Discuss the various approaches for dealing with branches. 2

3. a) Assume (i) 1 memory bus clock cycles to send the address (ii) 10 memory bus clock cycles each DRAM access initiated (iii) 2 memory bus clock cycles to send a word of data. Now analyze miss penalty for the following memory organizations- (i) One-word-wide memory (ii) Wide memory (iii) Interleaved memory organization. 3

   b) Describe following block placement mechanism in cache and analyze performance in terms of number of misses- (i) Fully associative (ii) Set-associative (iii) Direct-mapped. 3

   c) Draw the improved version of multiplication hardware. 2

   d) Define main memory. How many semiconductor cells are in a 4GB RAM? 2

4. a) Describe how virtual memory, TLB and cache work together with necessary figures. 3

   b) A program runs in 8 seconds on computer A, which has a 4GHz clock. You want to help a computer designer build a computer B that will run this program in 6 seconds. The designer has determined that a substantial increase in the clock rate is possible, but this increase will affect the rest of CPU design, causing B to require 1.2 times clock cycles as computer A for this program. What clock rate should you tell the designer to target? 2

   c) Describe following methods of handling instruction hazard due to conditional branch- (i) Delayed Branch (ii) Branch Prediction 3

   d) What is swapping? How virtual page number is mapped to secondary memory when page fault occurs? 2

5. a) Draw a flow chart of processing a read or write through in TLB and cache. 3

b) A complier designer is trying to decide between two code sequences for a particular computer. The hardware designers have supplied the fact in fiq-1(a).For a particular high-level-language statement, the compiler writer is considered two code sequences that require the instructions counts in fiq-1(b). Which code sequence executes the most instructions? Which will be faster? What is the CPI for each sequence? 3

c) Write down the division algorithm and draw the division hardware. 2

d) Write short note on (i) hit (ii) miss (iii) hit time (iv) miss penalty. 2

6. a) Draw the block diagram of single bus organization with in processor. 2

b) What is interrupt? Briefly describe interrupt hardware. 2

c) What is virtual memory? Why virtual memory is so important? How virtual address is translated to physical address? 3

d) What is page table? Describe how page table is indexed with the virtual page number to obtain corresponding physical page number with necessary figures. 3

7. a) What is TLB? How TLB makes virtual memory translation fast? 3

b) Verify the following statement with necessary reasoning- Increase in performance resulting from pipelining is proportional to the number of pipelining stages 3

c) What is Computer Architecture? Describe overall operation of a computer. 2

d) Write short note on (i) Throughput (ii) Response time (iii) Performance. 2

8. a) What is DMA? Explain DMA data transfer procedure using appropriate figure. 3

b) Explain operating principle of a static RAM with necessary figure. 4

c) What is cache memory? How does it minimize gap between CPU and RAM? 3

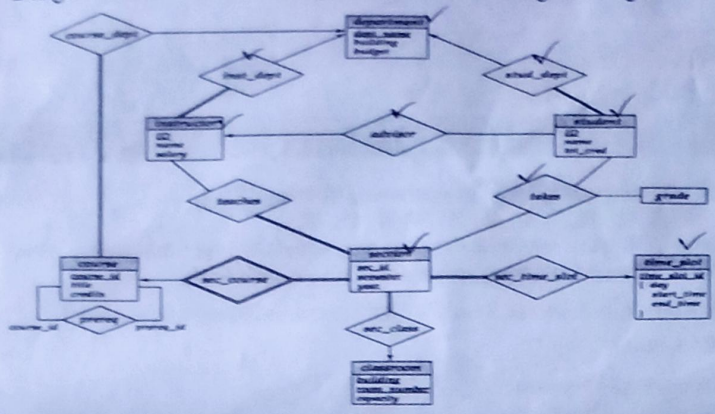
Bangabandhu Sheikh Mujibur Rahman Science and Technology University, Gopalganj
Department of computer Science & Engineering
3rd Year 1st Semester B.Sc. Engg. Examination-2019
Course Code: CSE309 Course Name: Database Management System

Full Marks: 60 **Times: 3 Hours**

N.B.:
i. Answer any SIX questions.
ii. All questions are of equal values

1. a) Distinguish between the DDL and DML with example. 3
   b) Who is database administrator? Write down the function of database administrator. 3
   c) Explain in detail about Database Management System advantages over file management system. 4

2. a) Design a relation database corresponding to the following E-R diagram. 5



   b) Construct an ER diagram for university registrar's office. The office maintains data about each class, including the instructor, the enrollment and the time and place of the class meetings. For each student class pair a grade is recorded. 5
   Determine the entities and relationships.

3. a) Discuss various types of fundamental relational algebra operations in binary operations. 5
   b) Suppose you are given the following requirements for a simple database for the National Hockey League (NHL): 5
   - the NHL has many teams,
   - each team has a name, a city, a coach, a captain, and a set of players,
   - each player belongs to only one team,
   - each player has a name, a position (such as left wing or goalie), a skill level, and a set of injury records,
   - a team captain is also a player,
   - a game is played between two teams (referred to as host_team and guest_team) and has a date (such as May 25th, 2018) and a score (such as 4 to 2).

   Construct a clean and concise ER diagram for the NHL database.

4. a) Illustrate the usage with example of SQL GROUP BY, ORDER BY and HAVING clauses. 5
   b) Consider the relational database of **Figure-4**, where the primary keys are underlined. 5

TRAIN (Name, Start, Destination)
TICKET (PNR_NO, Start, Destination, Fare)
PASSENGER (Name, Address, PNR_NO)

Figure-4: Database schemas.

   Write SQL expressions for the following queries:

   i) List the names of passengers who are travelling from the start to the destination station of the train.
   ii) Change the destination address of "ABC Express" to "Rangpur".
   iii) Find the name of all passengers whose address includes the substring "Rangpur".

5. a) What is Database Normalization? Explain its role in database design. 3

b) What do you know about functional dependency and data redundancy? 2

c) The following figure 5

i) What Normal Form did it violate?

ii) How should we normalized the above table?

EmployeeID	Lastname	Firstname	DepartmentCode
1001	Mills	Karen	SAL01
1002	Courtney	Francis	SAL02
1003	Smith	Phillip	ENG01
1005	Xavier	Duran	ENG02
1004	Morrison	John	SAL02

6. a) The following set of key values are given for constructing B^+-tree: 4

(3, 10, 17, 23, 28, 31, 41, 45, 51, 59, 61, 65, 70)

Assume that the tree is initially empty and values are added in ascending order. Now construct B^+ -tree such that maximum three pointers are fitted in each node.

b) What is Redundant Array of Independent Disks(RAID)? Discuss different levels of RAID. 6

7. a) What is Thomas' Write Rule? 2

b) Explain the Timestamp-Based Protocols. 5

c) Differentiate between homogeneous and heterogeneous database system. 3

8. a) During the execution, a transaction passes through several states. Draw the state diagram of transaction and define each of them briefly. 4

b) Describe several architectural models for parallel machines. 6