Bangabandhu Sheikh Mujibur Rahman Science and Technology University

Department of Computer Science and Engineering

3rd Year 1st Semester B.Sc. Engineering Examination-2015

Course No: CSE 310 Course Title: Computer Architecture and Organization

Total marks: 70 Time: 4 hours.

N.B.

i. Answer **SIX** questions, taking any **THREE** from each section.
ii. All questions are of equal values
iii. Use separate answer script for each section

SECTION - A

1. (a) Briefly explain the organization of ISA computer. 3

   (b) What do you mean by performance balance? Describe various ways of maintaining performance balance? 4

   (c) When does multiple interrupt occur? What are the two approaches to dealing with multiple interrupt? Explain. $4\frac{2}{3}$

2. (a) What is the benefit of using multiple-bus architecture compared to single-bus architecture? Discuss the method of bus arbitration. 4

   (b) Explain the direct mapping cache organization. Define cache hit and cache miss. 4

   (c) What is the benefit of using cache memory? Show the flowchart of cache memory read operation. $3\frac{2}{3}$

3. (a) What are key properties of semiconductor memory? $2\frac{2}{3}$

   (b) What do you mean by memory hierarchy? Briefly discuss. 3

   (c) What are the differences between DRAM and SRAM in terms of characteristics such as speed, size, cost and application? 3

   (d) Describe the interaction between hardware and software in a computer system. 3

4. (a) What are the major functions of an I/O module? Draw the block diagram of it. 2+2

   (b) Briefly define and compare three techniques for performing I/O? 4

   (c) What is DMA controller? Explain DMA driven data transfer technique. $3\frac{2}{3}$

SECTION-B

5. (a) What is the advantage of using twos complement representation? Perform the following calculation - 6 + 13 using in 8-bit twos complement representation? $2\frac{2}{3}$

   (b) How can an instruction be represented? Classify different types of instructions. 3

   (c) Why are transfer-of-control operations required? Discuss the branch instruction operation. 4

(d) Write the two-address machine instructions to compute the following state... (A-B)/(C+D×E)

6. (a) What are the key attributes of stack implementation? Describe basic stack operation with an example.
   (b) Describe different kinds of addressing modes with an example of each. 4
   (c) What are the roles of using registers? List the registers of 8086 processor. 2+2

7. (a) Sketch the control flow diagram of instruction pipelining. 3
   (b) What are the advantages of using pipelining? Derive the formula of speed-up factor of instruction pipelining. 2+3
   (c) What is pipelining hazard? Describe data hazard briefly. $3\frac{2}{3}$

8. (a) Draw the block diagram of control unit organization. What functions does it perform in a processor? $3\frac{2}{3}$
   (b) Explain the internal control structure of the control unit using i) Hardwired Control ii) Micro programmed control 4
   (c) Show the block diagram of micro-programmed control unit with its functioning. 4

Bangabandhu Sheikh Mujibur Rahman Science and Technology University

Department of Computer Science and Engineering

3rd Year 1st Semester B.Sc. Engineering Examination-2014

Course No: CSE-310 Course Title: Computer Architecture and Organization

Total marks: 70 Time: 4 hours.

N.B.

i. Answer **SIX** questions, taking any **THREE** from each section.
ii. All questions are of equal values
iii. Use separate answer script for each section

SECTION - A

1. (a) What, in general terms, is the distinction between computer architecture and organization? Draw the top-level structural view of a computer. 4

(b) Define Moore's law. Explain the consequences of Moore's law. 3

(c) When does multiple interrupt occur? What are the two approaches to dealing with multiple interrupt? Explain. $4\frac{2}{3}$

2. (a) What is the benefit of using multiple-bus architecture compared to single-bus architecture? Discuss the method of bus arbitration. $3\frac{2}{3}$

(b) What is the benefit of using cache memory? Show the flowchart of cache memory read operation. 4

(c) What is the problem of direct-mapping cache organization? How can it be eliminated in associative mapping? Explain. 4

3. (a) What are key properties of semiconductor memory? 2

(b) What are the differences between DRAM and SRAM in terms of characteristics such as speed, size, cost and application? 3

(c) Define EPROM, EEPROM and flash memory. 3

(d) What is magnetic disk? How are data read from a magnetic disk? $3\frac{2}{3}$

4. (a) What are the major functions of an I/O module? Draw the block diagram of it. 3

(b) Briefly define and compare three techniques for performing I/O. 3

(c) Distinguish between memory mapped I/O and isolated I/O. 2

(d) What is DMA controller? How DMA transfer is performed from memory to disk? $3\frac{2}{3}$

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SECTION-B

5. (a) Explain how to determine if a number is negative in the following representations: sign magnitude, twos complement with an example, Assume the negative number is -14. 3

   (b) How can an instruction be represented? Classify different types of instructions 3

   (c) Explain procedure call transfer-of-control operation. What is the best place for storing the return address and why? 4

   (d) Write the two-address machine instructions to compute the following statement: (A-B)/(C+D×E) $1\frac{2}{3}$

6. (a) What is stack? Describe typical stack implementation as a part of processor. 3

   (b) List and briefly explain basic addressing modes with an example of each respectively? 3

   (c) Draw the PDP-10 instruction format? What are the advantages and disadvantages of variable-length instruction format? 4

   (d) Define big endian and little endian of byte ordering. $1\frac{2}{3}$

7. (a) Draw the internal structure of the CPU. $2\frac{2}{3}$

   (b) Explain the pipelining strategy. What are the advantages of using pipelining? 4

   (c) How do number of instructions and number of stages relate to pipelining performance? 2

   (d) When does pipelining hazard occur? Describe data hazard briefly? 3

8. (a) Provide a brief description of the inputs and outputs of a control unit with a block diagram. $3\frac{2}{3}$

   (b) What do you mean by a hardwired implementation of a control unit? Explain. 3

   (c) Show the block diagram of micro-programmed control unit with its functioning. 3

   (d) What is the relationship between instructions and microinstructions? 2

Bangabandhu Sheikh Mujibur Rahman Science and Technology University
Department of Computer Science & Engineering
3rd Year 1st Semester B.Sc. Engineering Examination-2017

Course Title: Computer Architecture and Organization **Course Code: CSE 310**
Full Marks: 60 **Time: 3(Three) Hours**

N.B.
i) Answer **SIX** questions, taking any **THREE** from each section.
ii) All questions are of equal values.
iii) Use separate answer script for each section.

SECTION-A

Q.1 (a) What Moore's law states and what is the corresponding reality? 3

(b) With necessary illustration briefly explain the inter-relation between High-level language, Assembly language and Machine language. 3

(c) Explain in detail the Von Neumann machine model. 4

Q.2 (a) Describe why assessing the performance is challenging? 2

(b) The hardware designer supplied the instruction class and average clock cycles per instruction (CPI) (see table-1) and two code sequences and instruction counts for instruction class(see table-2). 6

Table-1

Instruction class	CPI for this class
A	1
B	2
C	3

Table-2

Code Sequence	Instruction counts for instruction class		
	A	B	C
1	3	2	1
2	4	1	2

Your task is to find out

I. Which code sequence executes the most instructions?
II. Which will be faster?
III. What is the CPI for each sequence?

(c) If machine A runs a program in 10 seconds and machine B runs the same program in 15 seconds, how faster is A than B? 2

Q.3 (a) With the help of a diagram show the relation between execution-time, CPU-time, user CPU-time and system CPU-time. 3

(b) Define alignment restriction and spilling register. Write down the principles of hardware design. 3

(c) Finds the MIPS machine language codes for the following instructions. 4

I. add $s1,$s2,$s3
II. lw $t1, 100($t2)

Q.4 (a) Find the corresponding MIPS assembly-codes for the following machine codes. 4

I. 0000 0000 1010 1111 1000 0000 0010 0010
II. 1000 1101 0010 1000 0000 0000 0000 1010

(b) Write the MIPS assembly code for the following instructions. 4

I. g=h+A[i]
II. while(save[i]==k)
i=i+j;

(c) What do you mean by cache memory and virtual memory? Sketch the memory hierarchy. 2

SECTION-B

Q.5 (a) Write down the 16-bit binary version of 6 then negate the binary number also convert the 16-bit binary versions of 6 and -6 to 32-bit binary numbers. 3

(b) Draw a 32 bit ALU that can perform **AND**,**OR**,**add**, **sub**, **slt** and **beq** operations. 3

(c) Define propagate (p_i) and generate (g_i) and explain why they are named so. 4

Determine the C_4values of these two 16 bit numbers:

a: 0001 1010 0011 0011

b: 1110 0101 1110 1011

Q.6 (a) Using Booth's algorithm multiply 2_{ten} by $-5_{ten.}$ 5

(b) Divide 7 by 2 using first version of division algorithm. 5

Q.7 (a) What is meant by bus control? 1

(b) List the methods of processor control. Draw and explain the PLA control organization. 3

(c) Classify the pipelining hazard. 2

(d) Describe the microprogram control logic with appropriate diagram. 4

Q.8 (a) What are the major characteristics of a pipeline? 2

(b) Discuss the various hazards that might arise in a pipeline? What are the remedies commonly adopted to overcome these hazards. 4

(c) Draw the block diagram of a DMA controller. What are the main functions of a typical DMA controller? 4