Bangladesh University of Business & Technology (BUBT)

Department of Computer Science and Engineering

Final Examination: Summer 2021

CSE 205 | Course Title: Digital Logic Design

Intake: 37th, Program: B.Sc. in CSE (Diploma Holders)

Marks-40

[Answer all the questions]

1. a) How do combinational circuits differ from sequential logic circuit? Explain with an example. **[05]**

b) **Design** a 3×8 decoder using only NAND logic gates and verify the circuit an example. **[05]**

2. a) **Implement** the following Boolean function using a multiplexer (MUX). **[05]**

$$F1 = \sum(0, D+1, D+2, D+3, 11, 12, 14, 15)$$

Here, ***D = (X1X2X3+5) mod 7*** where $X_1X_2X_3$ denotes the last 3 digits of your ID.

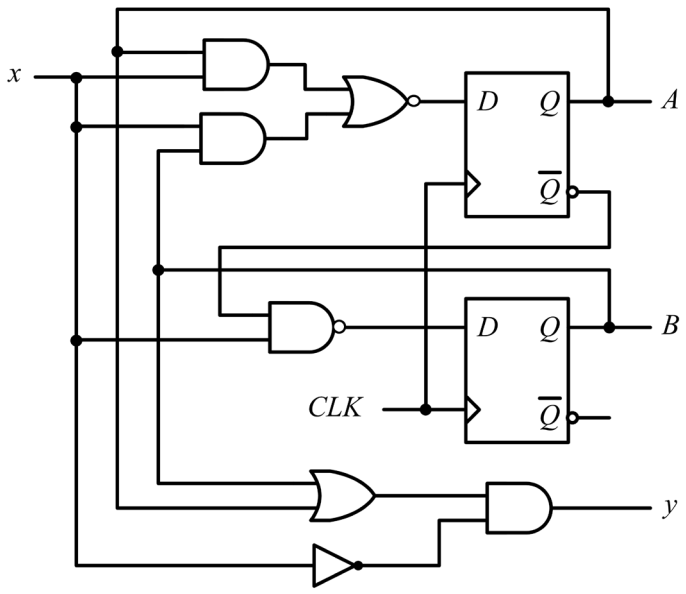
b) A combination circuit is defined by the following function F1: **Implement** the combinational circuit using a suitable decoder. **[05]**

$$F1 = \sum(N, N+1, N+3, N+4, N+7, N+8, N+10)$$

Here, ***N = (X1X2X3+5) mod 11*** where $X_1X_2X_3$ denotes the last 3 digits of your ID.

3. a) Analyze R-S flip-flop to find out the limitations and **characterize** a solution to overcome the limitation. **[05]**

b) **Derive** the state table and state diagram for the sequential circuit given below. **[05]**



4. a) **Explain** briefly the implementation of BCD ripple counter with J-K flip flop. **[05]**

b) Consider the following operating mode and **design** a shift register using MUX to perform all the operations. **[05]**

S0	S1	Operating Mode
0	0	Locked
1	0	Shift-Right
0	1	Shift-Left
1	1	Parallel Loading