07/26 Xknow diff. Ltun lea VS mov Intel Load Effective Address: + mov instruction Putting the address into the register. · Leal Src, DST X Src has to be addr. · Lead Src, DST X DST has to be register! ( ) mans so to memory But this · Leat ("(reax), \*lebx = mort "lolax, "lock Does not go to memory 4 : Lebx sets contents of hear register · mort blocax), "Lebx Is " elox get I byte long from memory at addr in " eax · leal to (cloeax), clobx 4. Webx gets 40 + contents of beax · Leal (% eax, % edx), % ebx 4 % elox gets sum of "leax, "locax contents \* Registers = numbers int sum (int A, int B) return A+B; nemory = addr.

\*think of it as being similar Leal ("loedi, "loesi), "lo eax to pointers Ret. get addr. of local var? int ren (inti) { VaQ -4(°6006), °6000x 'm+ \*p; < move \$3, (%.rbx) p=&ii xp=z t pointer deretenence xy=3; return 0; Lea not access memory

Overflow. · occurs when you try to represent a number that does not for \* LSB gets stored and MSb gets lost 00000000 FREFFRE € -1 80000000 80000000 - Smallest negative 32 bit signed int = 2 TEFFEFF - max 32 bit signed integer JELEELEE 0000000 · Register size of processor determines range of values that can be represented. -Unsigned examples: ·32 bit' 0 ... 232-1 · 8 bit : 0 ... 28 -1 · 64 6.4: 0 . . . 264 - 1 · 16 bit i 0 . . . 2 10-1 · An arithmetic result produces a result larger than N bits. · Overflow reduces result to modulo N, retaining only the least significant N bits, causing a Grap around. addl src, dst Dst += sre JEFFFFF (Src >0 &k dst >0 kk sum <0) 11 (Srcco kl Stco kksum >0) 8000 0 000 OVERFLOW

Subl src, dst DST -= src			
(STC <0 D& LSt >0 K& difference <0)			
11 (src >0 kg lst co kk difference >0)			
- 9nt orman - 9nt			
Port eller			
2006			
- 1044			
mull Src, dst DST X= Src Svc-05t			
(Src >0 && dat >0 && product <0)			
11 (src < 0 kg lst co kk product < 0)			
11 (Src < O Dh dot >0 kk product 70)			
11 (src > 0 k& lst co kk p volucto)			
+ 'int			
& tint & X -int & X + int & X -int &			
- cont + int			
B'it Ordering: A convention independent of byte ordering (Endianness)			
A convention independent of byte ordering			
(Endianness)			
86H Lbbit			
Target Target			
31 0 63 6461+			
31 0 05			

À			
Bitwise operations: (And, or, Xor)			
BITWISE AND (Coper	rector; k)		
int a,b,c;	31 ° 6	1100	
C= A LB;	B	L (010	
tu. opnis	31 0	1000	
De 1 \$50	- (   )		
BITWISE Or (Cope	rector; ()	1100	
int 0,6,0; C=A/B; Retus opnus		1 (010	
CEAIDI Ke tuo opnus	B	(110	
	31 6	(     0	
Bitwise Xor (cope	rector; ^)		
int ab.ci	_	1100	
C= ANB;	31 0	~ ( 0 ( 0	
int a,b,c; C=A,B; Re-tu. opn&	B	0110	
	31 0		
Bitwise Not (cope	rector; ~)		
· Clip the bits	$\sim$ 8		
int albi	31 0	~ 0 \	
a=~b;	SI S	10	
	\$1 6 		
<b>\$</b>			
Logical operations: (And, or)			
Logical And (operator: IS)			
result is 0 or 1			
if (fc) ke ge) rot reached			
Cogleal Or Coperator: 11)			
if (fc) 11 go) relect is 1, then right is			
if (fc) 11 gc) not reached			