

Ex)



```

VOID CALLED_FCN(CHAR * BUFFER)
{
    strcpy(BUFFER, "OUTPUT STRING");
}

VOID CALLER()
{
    CHAR STRING[200];
    * THIS LIVES LONGER
    AND IS REUSABLE
    CALLED_FCN(STRING);
}

```

```

CHAR *
CALLED_FCN()
{
    CHAR * S,
    * S = malloc(200), * DOES NOT LIVE THAT LONG
    strcpy(S, "OUTPUT STRING"),
    RETURN S;
}

VOID CALLER()
{
    CHAR * S,
    S = CALLED_FCN();
    FREE(S);
}

```

08/07

`char * strdup(const char *);`

`//malloc()` Space for a copy of the org String and copies the NUL-terminated org string to the copy. Call is responsible for `free()`

`Strncpy (char * DST, const char * Src)`

`//Copy to DST NUL-terminated Src`

`#include <STDIO.H>`

`FILE * fopen(const char * pathname, const char * mode);`

`SIZE_T fread(void *ptr, SIZE_T nelems, SIZE_T elemSize, FILE *f)`

`\ number of elements read nelems * elemSize`

`\ end file`

`EOF and Error => return 0`

`int feof(FILE *f);`

`\ 1 if eof 0 otherwise`

`int ferror(FILE *f);`

`\ 1 if error 0 otherwise`

`"r"` reading. Positioned at Start of file.
`"r+"` reading & writing. Also pos. at Start of file.
`"w"` Create new file or truncate existing file for writing
`"w+"` open for reading or writing. Create new file or truncate existing file
`"a"` append. Create newfile or at end of existing file.
`"a+"` open for writing or reading. Create new file or at end of existing file.

`const
Size_T fwrite (void *ptr, Size_T nitems, Size_T elemsize, file *)`

↳ number of elements written $nitems \times elemsize$

`int fseek (file *, long offset, int whence)`

↳ offset from start of file or -1 for error ↳ seek_set
 seek_cur
 seek_end

// move around inside a file + rearrange position within the file

`int fclose (file *); // flush output, close file`

↳ 0 success
1 error

`int fflush (file *);`

// force all buffered output to the disk. If arg is 0, flush all open output streams



Transistors: Semiconductor device that amplifies and switches electronic signals

Semiconductor $\xrightarrow{\text{heat}}$ increase conductivity
Super conductor $\xrightarrow{\text{cool}}$ increase conductivity] *

- An electrical switch without moving parts
- Many transistors can be embedded in integrated circuits

* microprocessors contain millions of transistors

* Logically, each transistor acts as a switch.



MOS (Metal Oxide Semiconductor) Transistor has 4 terminals.

- ① Source - current flows from
- ② Drain - current flows toward
- ③ Gate - has 0 or positive voltage
- ④ Body - substrate (underlying material)

"0"

Analog value

Illegal

"1"

$2.4 - 2.9 \text{ V}$

BASIC Logic Gate Symbol:

$A \rightarrow D = \bar{A}$
NOT

, $A \rightarrow D = A + B$
OR

$A \rightarrow D = AB$
AND

, $A \rightarrow D = \overline{AB}$
NAND

$A \rightarrow D = \overline{A + B}$
NOR

like
addition

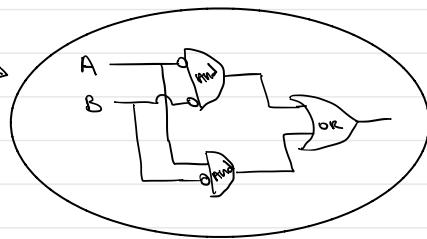
like
multiplication



Inputs		Output
A	B	
0	0	1
0	1	0
1	0	1
1	1	0

$$\bar{A}\bar{B} + A\bar{B} = 1$$

OR'd together all
expressions with output 1.



DeMorgan's Law:

To convert AND to OR (vice versa), invert inputs and output

Circuit Design & Logic Expressions

- Logical AND looks like multiplication.

- Logical OR looks like addition $A+B+C$

- Logical Negation : \bar{A}

- For N inputs, build a truth table with 2^N lines to account for all input possibilities

Truth Table:

A	B	C	F_1	F_2
0	0	0	1	1
0	0	1	1	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	0

Logic Expression

$$F_1 = \bar{A}\bar{B}C + \bar{A}BC + \bar{A}BC + ABC$$

$$F_2 = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C$$

Sum of products logic expression

Algebraic Rules for logic expressions

$$\text{Commutative: } w+y = y+w ; wy = yw$$

$$\text{Associative: } (w+y)+z = w+(y+z) ; (wy)z = w(yz)$$

$$\text{Distributive: } w+yz = (w+y)(w+z) ; w(y+z) = wy + wz$$

$$\text{Idempotent: } w+w = w ; ww = w$$

$$\text{Involution: } \overline{\overline{w}} = w$$

$$\text{Complement: } w+\overline{w} = 1 ; w\overline{w} = 0$$

$$\text{DeMorgan's Laws: } \overline{w+y} = \overline{w}\overline{y} ; \overline{wy} = \overline{w}+\overline{y}$$

$$\text{Identities: } 1+w = 1 ; 0w = 0$$

$$0+w = w ; 1w = w$$

$$w+\overline{w}y = w+y$$



DeMorgan's Law:

A pair of transformation rules that allow the expression of conjunctions (ANDs) and disjunctions (ORs) in terms of each other

1. The negation of a conjunction is the disjunction of the negations.

$$\sim(P \wedge Q) \Leftrightarrow (\sim P) \vee (\sim Q)$$

$\overset{\text{Negation}}{\nwarrow}$ $\overset{\text{equivalent to}}{\uparrow}$ $\overset{\text{Disjunction}}{\nearrow}$
 Conjunction AND

2. The negation of a disjunction is the conjunction of the negations.

$$\sim(P \vee Q) \Leftrightarrow (\sim P) \wedge (\sim Q)$$

$$\left\{ \begin{array}{l} (P \wedge Q) \Leftrightarrow \sim(\sim P \vee \sim Q) \\ (P \vee Q) \Leftrightarrow \sim(\sim P \wedge \sim Q) \end{array} \right.$$